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Supplementary materials for

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Table S1 Bit definitions of user input interface configuration

Bit	Meaning	Type	Definition
63 downto 60	Source ID	read only	Code defined by user, such as 0001b = user0
59	Source Mode	read only	0 = periodic signal, 1= burst signal
58 downto 50	Source Frequency	read only	$1/T_k$ = 0 to 511 Hz
49 downto 34	Source Rate	read only	v_k = 0 to 65535 Mbps
33 downto 30	FIFO Capacity	read only	q_{max} = 0 to 2^N
29 downto 15	Start Address	read only	Start Address << 15
14 downto 0	End Address	read only	End Address << 15

Table S2 Bit definitions of user input status

Bit	Meaning	Type	Definition
63 downto 60	Source ID	read only	Code defined by user, such as 0001b = user0
59 downto 58	Priority	read/write	00 = highest priority, 11 = lowest priority
57 downto 56	Max Amount	read/write	Maximum amount when priority = 00
55 downto 52	Error Status	read/write	Code defined by user
51 downto 49	Power	read/write	0 = power down, 1 = power on TMR
48 downto 46	Use	read/write	0 = disable, 1 = enable TMR
45 downto 32	FIFO Counter	read only	FIFO Counter $q(k, t)$
31 downto 0	Remaining Time	read/write	Remaining time $t_{re}(k, t)$ = N/75000000 s

Table S3 Bit definitions of queue scheduling instruction

Bit	Meaning	Definition
31 downto 24	INS HEAD	BCh
23 downto 22	Priority	00 = highest priority, 11 = lowest priority
21 downto 19	Priority Self Adjusting	0 = disable, 1 = enable TMR
18 downto 8	Channel Bitmap	A bit = a channel, 0 = not use,1 = use
7 downto 0	INS TAIL	EFh

Table S4 Hamming code codec process

Write
Step1: When the task scheduling module detects that it needs to jump to the write task, the Hamming ECC module enters the initialization state and completes the parameter setting according to the user configuration of this partition. Step2: When data are written to NAND Flash from the pre-write cache, the *RP* and *CP* are computed synchronously along with the data stream according to the rules of the formula. Step3: When the entire check segment is stored in NAND Flash, the corresponding Hamming code is computed and stored in pre-write code0. Step4: When the entire page of data has been stored in NAND Flash, the ECC code is subsequently stored in the OOB section of the page. Meanwhile, the external data are stored in pre-write cache1.
Read
Step1: When data are read from NAND Flash to the pre-read cache based on the mapping rules in Fig. 5, the new checksum code is computed in sync with the data stream. Step2: When the entire check segment of the data has been stored in the pre-read cache and the old ECC is obtained, the codex XORs the old and new ECC codes to compute the error correction operators *S0*, *S1* and *S2*. If they are all 0, the data are correct. If *S0*, *S1* and *S2* have a total of (m+n+3) bits of "1," it indicates that a bit flip has occurred, and the error position is (P_{row}, P_{column}). Otherwise, it indicates that an unrepairable error has occurred, and the module reports an anomaly to the upper computer. Step3: Data errors are corrected synchronously with the data stream when the external module reads data from the pre-read cache.

The parameters of step 2 are as follows:

$$\begin{aligned} S &= \{S2, S1, S0\}, \\ P_{column} &= \{S(2m+5), ..., S(3), S(1)\}, \\ P_{row} &= \{S(2n+2m+5), ..., S(2m+1), S(2m+7)\}. \end{aligned} \tag{S1}$$

Table S5 Payload matrix and parameters of different microsatellites

Model	payload	Frequency /Hz	Rate /Mbps	Packet size /Mb
A	Camera1	burst	6400	998
	Camera2	30	1800	4.7
B	Camera3	burst	6720	990
	Camera4	25	1920	4.7
C	Camera5	0.1	5460	2387
	Payload1	2	300	85.3
D	Camera6	3	1560	0.29
	Payload2	5	300	24
A&B	Processor1	2	12000	176
&C	Processor2	2	300	176
&D	Processor3	2	1000	176

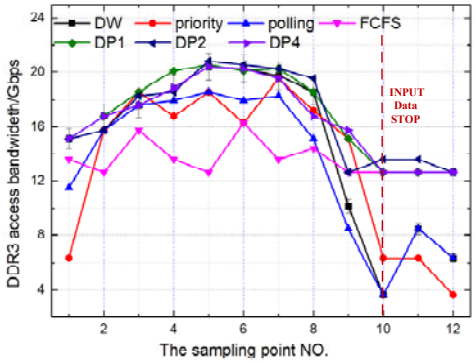

Fig. S1 Measured DDR3 access bandwidth

Fig. S2 Images used in the experiments

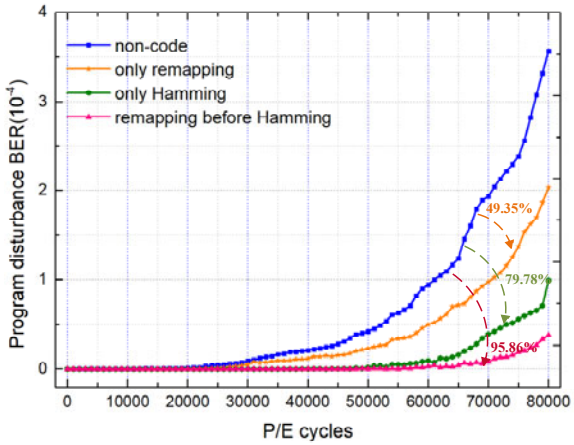

Fig. S3 Program disturbance BER at the room temperature

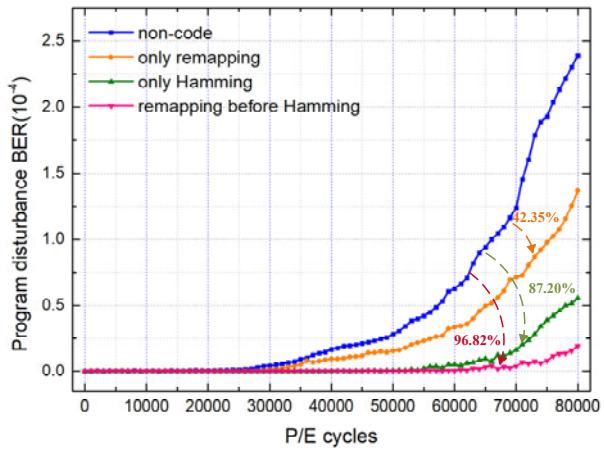

Fig. S4 Program disturbance BER at -30 ℃

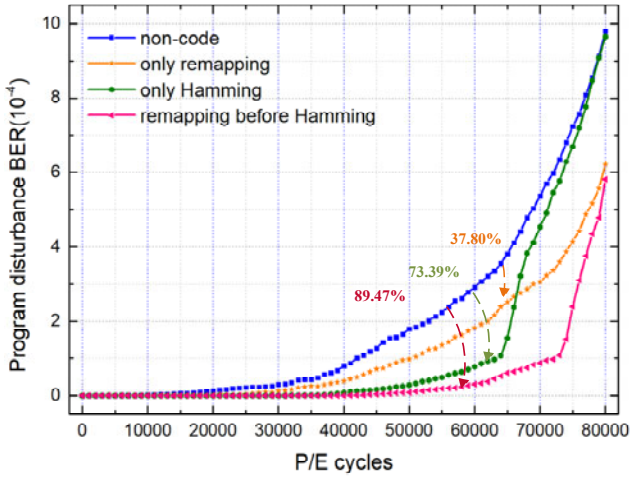

Fig. S5 Program disturbance BER at 60 ℃

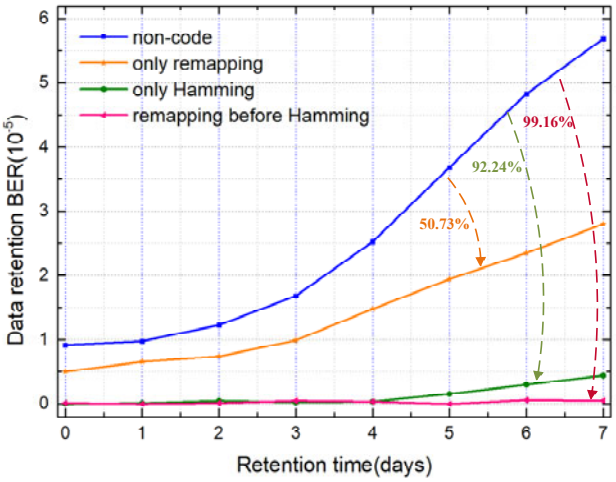

Fig. S6 Data retention BER at the room temperature

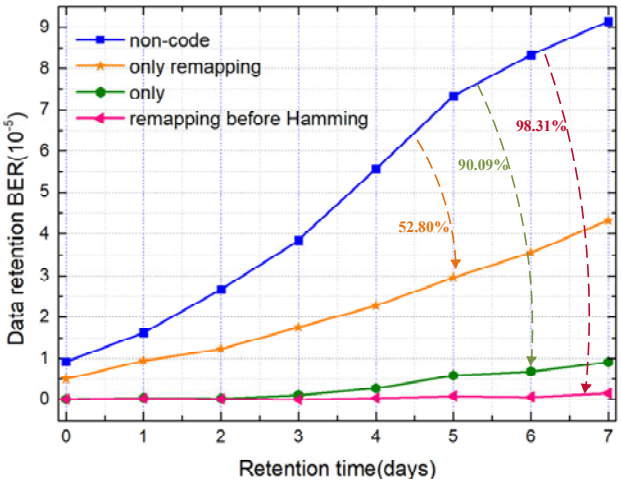

Fig. S7 Data retention BER during temperature cycling