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An analog front-end circuit for ISO/IEC 15693-compatible RFID transponder IC

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Abstract: The 13.56 MHz analog front-end circuit for ISO/IEC 15693-compatible radio frequency identification (RFID) transponder IC presented in this paper converts RF power to DC and extracts clock and data from the interrogator by 10% or 100% ASK modulation. The transponder sends data back to the interrogator by load modulation technology. The electrostatic discharge (ESD) protection circuits function to limit RF voltage to a safe level. An inductive coupling simulation modelling for 13.56 MHz RFID system is presented, with simulation results showing that the transponder operates over a wide range of electromagnetic field strength from H_{min} (150 mA/m) to H_{max} (5 A/m). The transponder IC is implemented in SMIC 0.35-μm three-metal two-poly mixed signal CMOS technology with embedded EEPROM.

Key words: Radio frequency identification (RFID), ISO/IEC 15693, Transponder IC, Analog front-end
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INTRODUCTION

The rapidly increasing application of radio frequency identification (RFID) includes supply chain management, access control to buildings, public transportation, airport baggage, and express parcel logistics (Karthaus and Fischer, 2003; Feldhofer, 2004; Glidden *et al*., 2004). Using an RFID system is a good approach for automated identification of products.

RFID system consists of two major components, an interrogator (reader) and a transponder (tag), composed of an antenna coil and a silicon chip (Feldhofer, 2004). Typical carrier frequencies (interrogator's transmitting frequency) in today's applications range from 125 kHz to 5.8 GHz. Each frequency band has advantages and disadvantages. The 13.56 MHz frequency bands offer the advantages of low frequency (125 kHz), ultra high frequency (860~960 MHz) and microwave (2.4 GHz) bands. RFID tags are often classified as passive or active. The passive tag is energized by a time-varying electromagnetic radio frequency (RF) wave transmitted by the reader, while the active tag is energized by battery. Passive tags have the virtues of low cost and long life. Therefore, this frequency band becomes the most dominant frequency band in passive RFID applications (Lee and Sorrells, 2004).

The international standards for 13.56 MHz RFID system are ISO/IEC 14443 type A/type B, ISO/IEC 15693 and ISO 18000-3 (Min *et al*., 2005; ISO/IEC FCD 15693, 2003; ISO/IEC FCD 14443, 2003; ISO/IEC FDIS 18000-3, 2003). ISO/IEC 14443 is a standard operating in proximity, with communicating distance of less than 10 cm. ISO/IEC 15693 is a standard for vicinity cards, with operating range of up to 1 m. ISO/IEC 18000-3 is a new standard for item management. The physical layer of the air interface for ISO/IEC 18000-3 Mode 1 is compatible with ISO/IEC 15693.

Communications between the interrogator and the transponder IC takes place using the modulation principle of ASK in the ISO/IEC 15693. Two modulation indexes are used: 10% and 100%. Data coding is possible using 1 out of 256 or 1 out of 4 data coding mode which leads to a downlink rate up to 26.48 kbps.

The transponder uses load modulation to send its response. Depending on the mode, uplink rates of up to 26.69 kbps are achievable. The configuration is done via the application protocol.

There were many publications on the design of a chip for RFID (Cho *et al*., 2005; de Vita and Iannaccone, 2005a; 2005b; Feldhofer, 2004; Finkenzeller, 2002; Fukumizu *et al*., 2004; Glidden *et al*., 2004; Henrici and Mäuller, 2004; Karthaus and Fischer, 2003; Lee and Sorrells, 2004; Li and Liu, 2005; Min *et al*., 2005; Ye and Chan, 2005; Zhu *et al*., 2005); however, there are almost no technical papers regarding the design of ISO/IEC 15693-compatible RFID transponder IC. This project was aimed at designing a new transponder IC analog front-end for magnetic power and data transmission to conform with the transfer protocol of ISO/IEC 15693. The circuits have been applied to the transponder IC with a very well-suited technology and the simulation results have also been approved by Cadence environment. The technology is SMIC 0.35-μm three-metal two-poly mixed signal CMOS process with embedded EEPROM.

Sections 2 and 3 describe the system architecture of the transponder IC and the operation of the different building blocks, respectively. Section 4 presents an inductive coupling simulation modelling for 13.56 MHz RFID system and shows the simulation results, and conclusions are provided in Section 5.

ARCHITECTURE OF THE TRANSPONDER IC

Fig.1 shows the system architecture of the transponder IC and the block diagram of the analog front-end. The chip operates based on the inductive coupling RFID principle, and includes analog front-end, EEPROM, and digital controller. Antenna 1 and Antenna 2 are connected to the antenna which is the only external component of the transponder IC. An RF voltage is induced by the electromagnetic field strength and boosted by the resonant circuit to a level that can power up the chip after rectification. The rectifier (RECT) converts a part of the incoming RF signal power to DC voltage. In strong field case, both the RF and DC voltages are too high, causing potential damage to the circuit (Li and Liu, 2005). To avoid this situation, ESD protection circuits limit the chip operation voltage to a safe level. The CLOCK block is the source of the system clock and the ASK/FSK reverse link frequencies. ASK demodulator (DEMOD) is designed to restore the data from the mixed RF signal coupled from the interrogator. Load modulation technology is utilized to send data back to the interrogator.

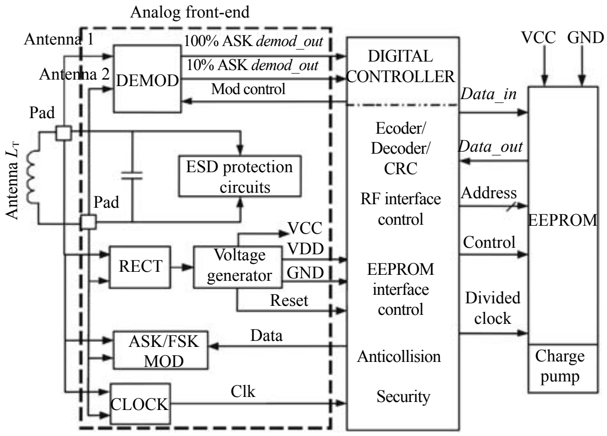

Fig.1 Block diagram of transponder IC

CIRCUIT DESIGN

RF resonant and ESD protection circuits

Fig.2 shows the RF resonant and electrostatic discharge (ESD) protection circuits. *L* and *C*3 form an RF tank circuit with resonant frequency *f* and quality factor *Q* as

$$f = \frac{1}{2\pi\sqrt{LC_3}}, \tag{1}$$

$$Q = \frac{R_L}{2\pi fL} = 2\pi f R_L C_3, \tag{2}$$

where R_L is the equivalent load resistance of the transponder IC. In Eqs.(1) and (2), *C*3 is written as C_3. The read range increases with *Q* of the antenna circuit. This is because the induced voltage is directly proportional to *Q* of the circuit. The recommended *Q* for long-range applications is greater than 40 (Lee and Sorrells, 2004). The clamping circuit consists of devices *M*3~*M*6. The clamping circuit is on when the electromagnetic field strength is strong. Meanwhile, the devices *M*1 and *M*2 are on to limit the RF voltage to a safe level. The devices *M*1 and *M*2 are also on to protect the chip when a high frequency voltage signal is fed to RC filter (*R*3, *C*2).

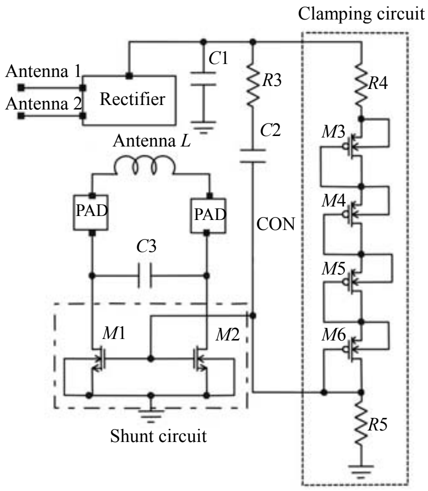

Fig.2 RF resonant and ESD protection circuits

Rectifier (RECT) and voltage generator

The rectifier converts a part of the incoming RF signal power to DC for voltage generator, supplying power (VDD and VCC) for all active circuits on the transponder IC. The circuit is based on the NMOS gate cross-connected bridge rectifier structure shown in Fig.3. The two NMOS transistors connected to the chip ground serve as switches. This configuration can decrease the minimum input working level for an expected output voltage level (Zhu *et al.*, 2005). Our devices have their gates dynamically biased near the threshold in order to respond to small amplitude input signals.

$$VHD \approx V_m / \sqrt{2} - V_{th}, \tag{3}$$

where V_m is the peak-to-peak amplitude of Antenna Voltage, V_{th} is the value of threshold voltage for NMOS.

Voltage generator block serves to provide regulated currents and voltages for other blocks on the chip, such as digital controller and EEPROM. This block provides high power supply rejection in spite of the extreme variability from the input RF power. For different blocks with different voltage levels, the voltage level translation is implemented by the voltage generator. Moreover, this block also senses when the chip is put into a reset condition and detects when insufficient power exists for performing write operations.

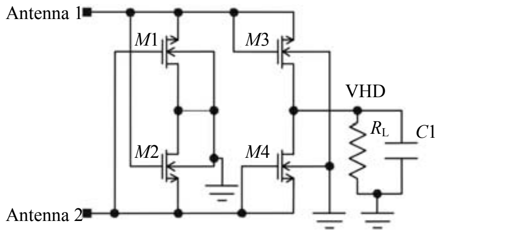

Fig.3 Schematic of NMOS bridge rectifier structure

Clock recovery

The CLOCK block is the source of the system clock and the ASK/FSK reverse link frequencies. The circuit is shown in Fig.4. The CLOCK block consists of NMOS devices $M1$ and $M8$, a latch, an inverter. Part of the high frequency antenna voltage (13.56 MHz) travels to the CLOCK block to generate an internal clocking signal Clk (13.56 MHz) sent to the divider of the digital controller. After division by 32, a clocking signal of 423.75 kHz is available for one sub-carrier reverse link. After division by 28, another clocking signal of 484.28 kHz and the clocking signal of 423.75 kHz are used for two sub-carriers reverse link. The inputs Antenna 1 and Antenna 2 sent to half wave rectifier are two opposite signals. When Antenna 1 is high and Antenna 2 is low, NMOS $M1$ controlled by Antenna 1 will be on and NMOS $M8$ controlled by Antenna 2 will be off, which make the inputs of the first inverter to be low and the second one to be high. As a result, the output Clk will be high. Contrarily, the Clk will be low.

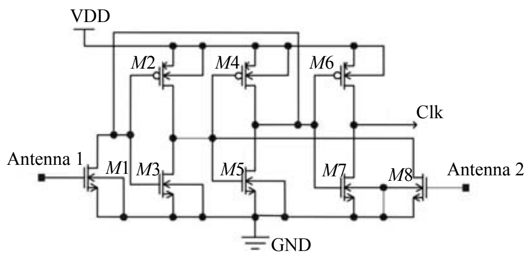

Fig.4 Schematic of clock recovery structure

ASK demodulator

The demodulator serves to detect the two modulation indexes of ASK and output a digital representation of the envelope. The transponder IC uses an envelope detector, amplifier, and latch for the demodulation. The degree of 10% modulation indexes of ASK is lower than the 100%, so the signals of 10% ASK modulation are harder to detect than that of 100% ASK modulation. The 10% ASK demodulation circuits are shown in Fig.5. The envelope detector detects the changes in the voltage amplitude and passes it into RC filter (*R*2, *C*2). The analog signal passing through the shaping amplifier is converted by the latch into data signal. The inverter formed by *M*26 and *M*27 ensures that 10% ASK *demo_out* data is logically compatible with the transition protocol of ISO/IEC 15693. The digital output pulses from the demodulator are passed to the pulse position modulation (PPM) decoder of the digital controller.

Modulator

Due to the weak coupling between the interrogator antenna and the transponder IC antenna, the voltage fluctuations at the interrogator antenna are very slight. In practice, for a 13.56 MHz system, given an antenna voltage of approximately 100 V (voltage step-up by resonance), a useful signal of around 10 mV can be expected (=80 dB signal/noise ratio) (Finkenzeller, 2002). Load modulation technology is utilized to generate modulation sidebands as shown in Fig.6. If the load resistors (*R*1, *R*2) in the transponder IC are switched on and off at a very high elementary frequency f_S, then two spectral lines are created at a distance of $\pm f_S$ around the transmission frequency of the interrogator f_{reader} as shown in Fig.7, and these can be easily detected by the interrogator. The new elementary frequency is called a sub-carrier. The transponder IC transfer data by ASK (423.75 kHz is selected for f_S) and FSK (423.75 and 484.28 kHz are selected for f_S) modulations of the sub-carrier.

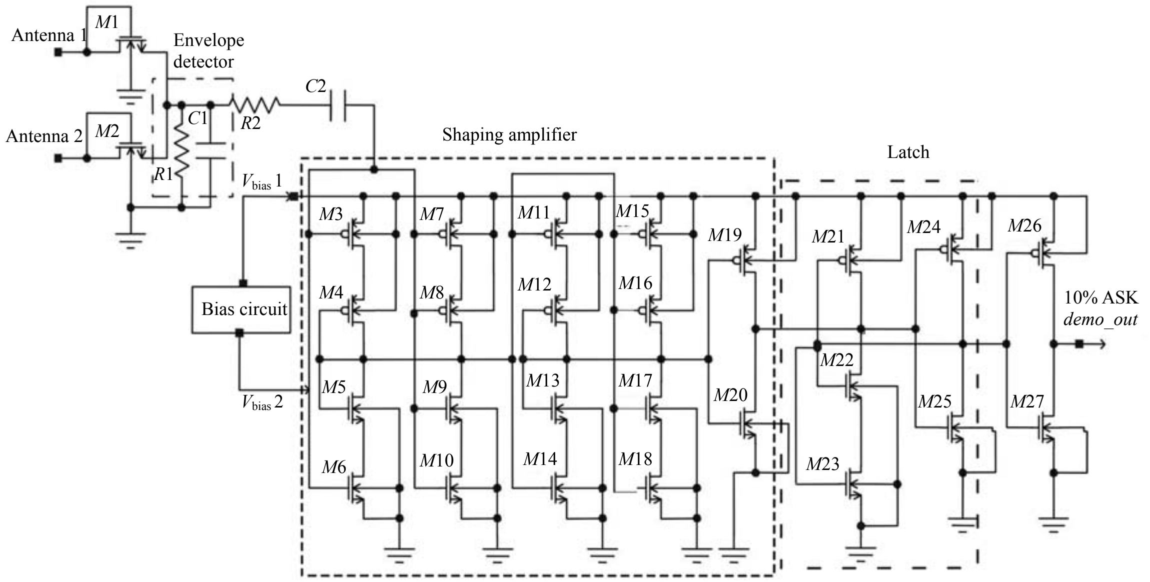

Fig.5 Schematic of 10% ASK demodulation

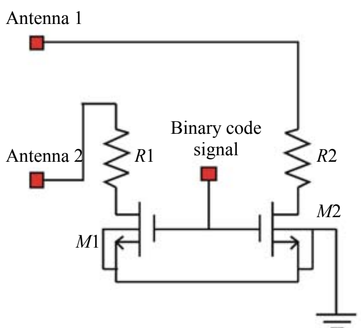

Fig.6 Schematic of generating load modulation

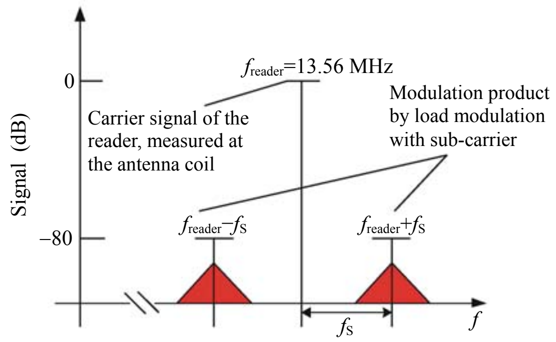

Fig.7 Load modulation creates two sidebands of the sub-carrier frequency around the f_{reader}

SIMULATION

Simulation modelling

The 13.56 MHz RFID system operates based on the inductive coupling principle (Finkenzeller, 2002). A simulation model of the transponder IC is shown in Fig.8. We can calculate the 13.56 MHz equivalent voltage source U_2 induced in the reference VICC (transponder) coil under operating field specified in 6.2 of ISO/IEC 15693-2 (ISO/IEC FCD 15693, 2003):

$$U_2=\mu_0 AHN\omega=1.45H, \quad (4)$$

where μ_0 is permeability of free space, H is the magic field strength, A is the cross section area of the coil, ω is the angular frequency, and N is the turns of the coil (Finkenzeller, 2002). A transponder operates as intended continuously operating field between $H_{\min}$ and $H_{\max}$ in an ISO/IEC 15693-compatible RFID system. $H_{\min}$ is the minimum operating field and has a value of 150 mA/m (rms), which is a typical value for an RFID interrogator at a distance of 1 m. While $H_{\max}$ is the maximum operating field and has a value of 5 A/m (rms). U_2 is calculated to be 0.2175 V (rms) at $H=H_{\min}$=150 mA/m (rms), and the peak voltage V_{pmin}=0.31 V. When $H=H_{\max}$=5 A/m (rms), U_2=7.25 V (rms) and the peak voltage V_{pmax}=10.25 V. The voltage at the transponder IC's input is given by

$$V_{\mathrm{in}}=\frac{\mathrm{j}U_2}{1+\mathrm{j}\omega L_{\mathrm{T}}\cdot\left(\dfrac{1}{R_{\mathrm{L}}}+\mathrm{j}\omega C_3\right)}. \quad (5)$$

The ASK modulator generates 10% and 100% ASK modulated signal, with the EMC filter being a low pass filter composed of inductor and capacitor.

The cut-off frequency of the EMC filter was designed for 14.5 MHz, which is slightly above the carrier frequency (Min *et al*., 2005). The resonance frequency of the LC tank composed by $C3$ and the loop antenna L_{T} is tuned to carrier frequency of 13.56 MHz.

Simulation results

The simulation results showed that the transponder IC can operate between $H_{\min}$ and $H_{\max}$. Fig.9 shows the simulation results of DC voltages (VDD and VCC) and data detection at $H_{\max}$ with 10% ASK modulation, and Fig.10 shows the results at $H_{\min}$ with 100% ASK modulation. The *data_demod_10p* and *data_demod_100p* are the data detection signals. The chip also generates a power on reset (*CLR_*) signal. After the DC voltages are ready, the *CLR_* transits from low to high. The induced voltage of the transponder antenna at $H_{\max}$ is higher than that at $H_{\min}$, so the power on reset time at $H_{\max}$ is shorter. The simulation results of modulating data back are shown in Fig.11. Because the voltage fluctuations at the antenna of the reader that represent the useful signal are smaller by orders of magnitude than the output voltage of the reader, the transponder IC is harder to modulate data back at $H_{\max}$. In Fig.11b, although the amplitude modulation is not obvious from the waveform, it achieved 200 mV peak amplitude change, which is above the minimum 10 mV specification given in (ISO/IEC FCD 15693, 2003; Finkenzeller, 2002; ISO/IEC FDIS 18000-3, 2003).

CONCLUSION

An analog front-end circuit for ISO/IEC 15693-compatible RFID transponder IC was designed by using the SMIC 0.35-μm three-metal two-poly CMOS process. The simulation results demonstrated

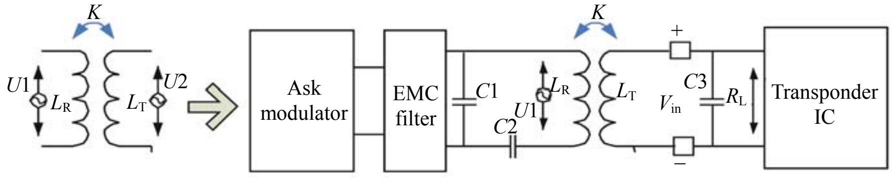

Fig.8 Simulation modelling

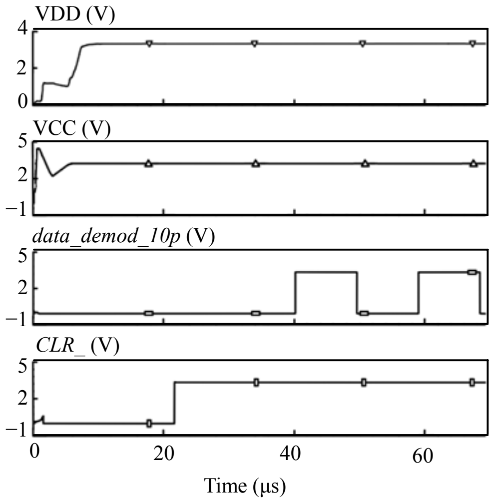

Fig.9 Simulated waveforms of DC voltages and data detection at H_{max} with 10% ASK

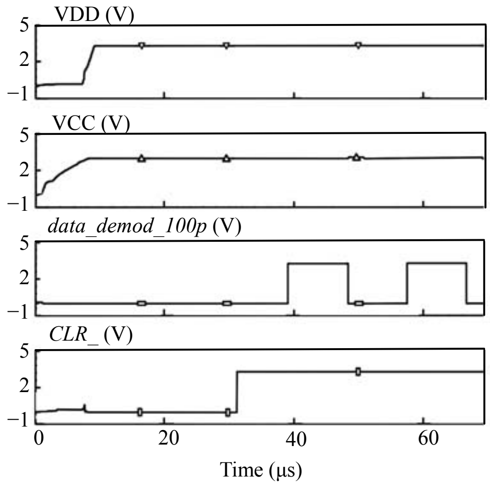

Fig.10 Simulated waveforms of DC voltages and data detection at H_{min} with 100% ASK

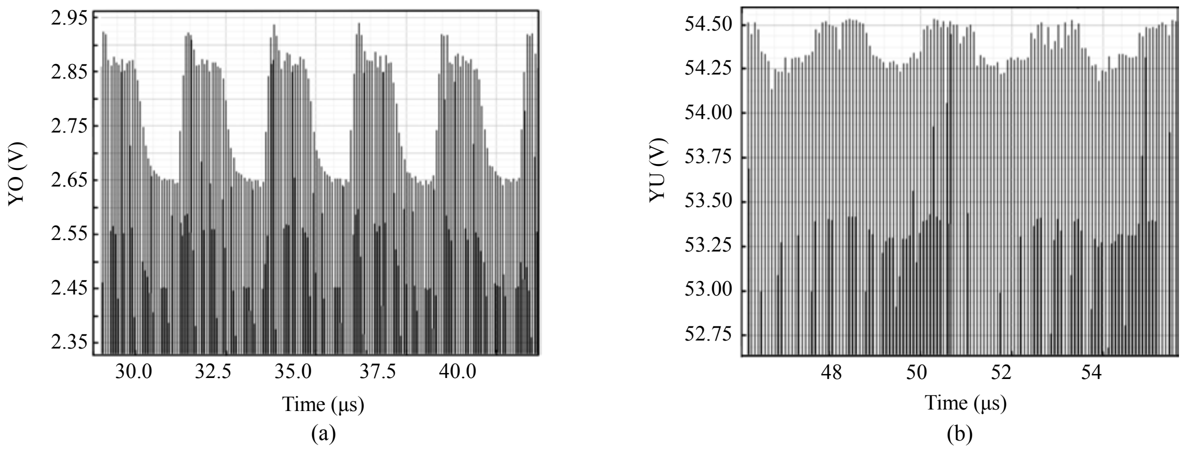

Fig.11 Simulated waveforms of modulating data back for two different RF input powers. (a) Minimum operating field (150 mA/m); (b) Maximum operating field (5 A/m)

that transponder IC effectively converts RF power into DC and extracts clock and data on ASK modulation from the interrogator, and correctly sends data back to the interrogator. The circuits have been applied to the project of the transponder IC. The whole chip layout is shown in Fig.12. The transponder IC, with 1.2 mm×1.2 mm die area, can operate as intended continuously operating field between H_{min} and H_{max}. This is a huge improvement compared with the existing products.

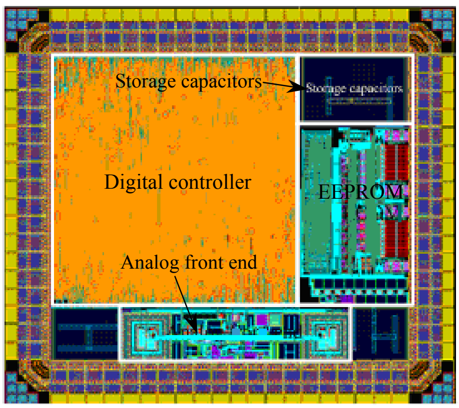

Fig.12 The tag IC die layout

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