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An accurate analytical *I-V* model for sub-90-nm MOSFETs and its application to read static noise margin modeling

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Abstract: We propose an accurate model to describe the *I-V* characteristics of a sub-90-nm metal–oxide–semiconductor field-effect transistor (MOSFET) in the linear and saturation regions for fast analytical calculation of the current. The model is based on the BSIM3v3 model. Instead of using constant threshold voltage and early voltage, as is assumed in the BSIM3v3 model, we define these voltages as functions of the gate-source voltage. The accuracy of the model is verified by comparison with HSPICE for the 90-, 65-, 45-, and 32-nm CMOS technologies. The model shows better accuracy than the *n*th-power and BSIM3v3 models. Then, we use the proposed *I-V* model to calculate the read static noise margin (SNM) of nano-scale conventional 6T static random-access memory (SRAM) cells with high accuracy. We calculate the read SNM by approximating the inverter transfer voltage characteristic of the cell in the regions where vertices of the maximum square of the butterfly curves are placed. The results for the SNM are also in excellent agreement with those of the HSPICE simulation for 90-, 65-, 45-, and 32-nm technologies. Verification in the presence of process variations and negative bias temperature instability (NBTI) shows that the model can accurately predict the minimum supply voltage required for a target yield.

Key words: Modeling, Nano-scale, Process variation, Read static noise margin (SNM), SRAM
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1 Introduction

Analytical *I-V* models are necessary for the design of integrated circuits. In the nano-scale regime, a simple square law model for the *I-V* characteristics of metal–oxide–semiconductor field-effect transistors (MOSFETs) is inaccurate primarily because of velocity saturation and short channel effects. There have been many attempts to accurately model the characteristics of these transistors, including complicated empirical models used for HSPICE simulations. Simple models preserving high accuracy have also been developed for circuit analysis. The *n*th-power model (Sakurai and Newton, 1990; 1991), which assumes a non-integer *n*th-power relation between current and voltage, is an example of these models. The model has been recently modified for sub-65-nm technology (Hiroki *et al.*, 2008). While the model speeds up simulations, obtaining analytical circuit parameters such as stability metrics of SRAM cells requires the use of circuit models with integer powers between current and voltage, in order to provide explicit expressions for these metrics.

Static random-access memory (SRAM) robustness in the hold and read states is measured using static noise margin (SNM) as the figure of merit. The SNM is in turn defined as the DC-voltage disturbance that takes the SRAM cell to the edge of instability (Lohstroh *et al.*, 1983). Lohstroh *et al.* (1983) presented different equivalent criteria for the definition of SNM, including small signal closed-loop gain of cross-coupled inverters of the SRAM cell, and the side length of the maximum square between the normal and mirrored voltage transfer characteristics.

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Seevinck *et al.* (1987) proposed an analytical SNM model based on the square law device current equation. Since the law is not valid for sub-90-nm technology, the model may not be used in this regime. Bhavnagarwala *et al.* (2001) presented an SNM model using the trans-regional drain current model (Bhavnagarwala *et al.*, 2000). The model is implicit and complex, relying on fixed point iterations to obtain self-consistency. Chen *et al.* (2007) estimated the voltage transfer characteristics of the cross-coupled inverters of an SRAM cell as a Butterworth filter. The error of this technique was less than 8%. In this case, however, no closed-form expression was derived for the SNM. In addition, it was assumed that all of the transistor threshold voltages have the same magnitude. Agarwal and Nassif (2008) used the small signal closed-loop gain of cross-coupled inverters of the SRAM cell as a criterion for SNM modeling. This model was based on simulation where process variation effects could not be investigated readily. The SNM modeling for sub-threshold SRAM has also been examined in Calhoun and Chandrakasan (2006) and Hu *et al.* (2009).

This paper has two contributions. First, a model is proposed for the *I-V* characteristics of sub-90-nm technology. The key advantage of the proposed model compared to the existing models is its ability to analytically model the *I-V* characteristics of highly scaled transistors with very good accuracy. The existing analytical models for *I-V* characteristics of highly scaled CMOS technologies are either too complex with too many parameters, which prohibits their use for hand calculations (e.g., numerical models used in HSPICE), or too simplistic with very low accuracies (such as the α-power law or nth-power law). Second, as an example of the effectiveness of the proposed model, we use it to analytically obtain SNM of SRAMs with higher accuracy compared with the previous analytical models.

2 The proposed *I-V* model

To obtain expressions for the SNM parameter of the SRAM cell, we need expressions for the *I-V* characteristics of the transistors in both the linear and saturation regions. In this work, we propose a simple *I-V* model which can be used for SNM calculations.

2.1 Linear region

Our model is based on the BSIM3v3 model for hand calculations. The BSIM3v3 model equation in the linear region ($V_{ds}\leq V_{dsat}$) is given by (Cheng *et al.*, 1995)

$$I_{ds}=\mu_{eff}C_{ox}\frac{W}{L}\frac{1}{1+V_{ds}/(E_{sat}L)}\left(V_{gs}-V_{th}-\frac{V_{ds}}{2}\right)V_{ds}, \quad (1)$$

$$V_{dsat}=\frac{E_{sat}L(V_{gs}-V_{th})}{E_{sat}L+V_{gs}-V_{th}}, \quad (2)$$

where μ_{eff} is the effective mobility, C_{ox} is the gate capacitance per unit area, W is the channel width, L is the channel length, V_{ds} and I_{ds} are the drain-source voltage and current respectively, V_{gs} is the gate-source voltage, V_{th} is the threshold voltage, E_{sat} is the minimum electric field for the onset of velocity saturation, and V_{dsat} is the drain saturation voltage. In the BSIM3v3 model, for V_{th} we use the effective threshold voltage specified by the technology proposed by Morshed *et al.* (2009). In our proposed model, we use the same equations as above except that we replace V_{th} by a fitted threshold voltage, which is a function of V_{gs}. Using this approach, we achieve both simplicity and accuracy in our calculations.

The current-voltage characteristics obtained from the HSPICE simulations, the BSIM3v3 model (Eq. (1)), the nth-power law, and the proposed model for a 45-nm technology are plotted in Fig. 1. We use the BSIM4 technology model for our HSPICE simulations (Morshed *et al.*, 2009). The fitting parameters of the nth-power model are determined by the procedure discussed in Sakurai and Newton (1991). As shown in this figure, the results of the BSIM3v3

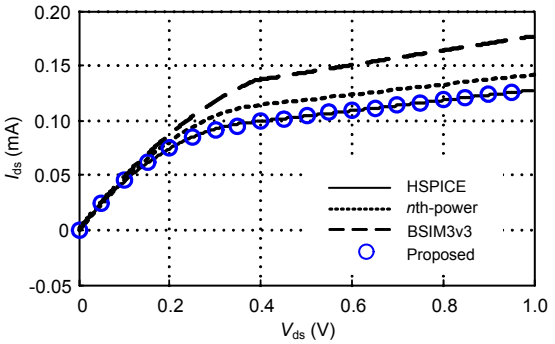

Fig. 1 I_{ds}-V_{ds} characteristics calculated using HSPICE simulations, the BSIM3v3 model, the nth-power law, and the proposed model at V_{gs}=0.9 V for 45-nm technology

model deviate considerably from those of the HSPICE simulations. While the *n*th-power model has good accuracy at the bias points where the fitting parameters are determined, its error becomes non-negligible at other bias points.

We explain how the (fitted) threshold voltage is determined in the proposed model. Fig. 2 depicts the threshold voltage of the model, denoted by V_{th}, versus V_{gs} for the 32-, 45-, 65-, and 90-nm technologies (Morshed *et al.*, 2009). Next, we model V_{th} as a function of V_{gs}. The V_{th} is determined such that the error of the proposed model compared to the HSPICE results is minimized. As seen from the results, we can divide the characteristics into two regions determined by a point (V_{thl}). Based on the observations, we propose the following expressions for modeling the V_{th}-V_{gs} characteristic:

$$V_{th}=\begin{cases}-a_1(V_{gs}-V_{thl})^2+V_{thl0}, & V_{gs}\le V_{thl},\\ -a_2(V_{gs}-V_{thl})^2+V_{thl0}, & V_{gs}>V_{thl},\end{cases} \tag{3}$$

where V_{thl0} is the fitted threshold voltage for V_{gs} equal to V_{thl}, and a_1 and a_2 are two model parameters. Later, we will explain how to compute these parameters. Our results for the four technologies shown in Fig. 2 demonstrate that V_{thl} is the technology threshold voltage (denoted as V_{th0} in HSPICE). For example, in the 45-nm technology, V_{thl} is equal to 0.466 V. To determine whether the modeling remains valid if the technology uses other threshold voltage values, we altered the technology threshold voltage (V_{th0} in HSPICE) between 0.37 V and 0.55 V in the 45-nm technology model. The simulations results again

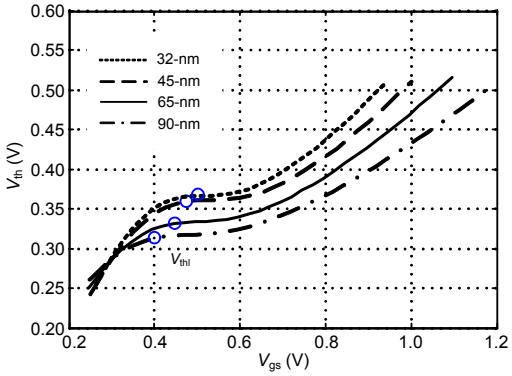

Fig. 2 V_{th}-V_{gs} characteristics for 32-, 45-, 65-, and 90-nm technologies

revealed the same characteristics for V_{th} versus V_{gs} and very good accuracy for the proposed model (Fig. 3). Note that the modeling results for PMOS transistors are similar in terms of their accuracy.

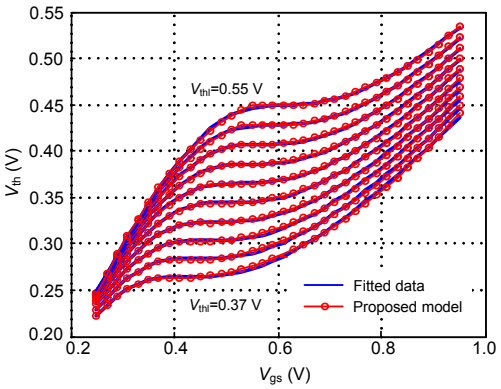

Fig. 3 V_{th}-V_{gs} characteristics for 45-nm technology with the running parameter V_{thl} altered between 0.37 V and 0.55 V

The long channel threshold voltage is given by (Tsividis, 2003)

$$V_{thl}=V_{FB}+2\phi_f+\frac{Q_{dep}}{C_{ox}}+\frac{Q_{im}}{C_{ox}}, \tag{4}$$

where V_{FB} is the flat band voltage, ϕ_f the energy of the Fermi level in the bulk with respect to the intrinsic level, Q_{dep} the depletion charge, Q_{im} the implant dose (1/cm^2), and C_{ox} the oxide capacitance per cm^2.

Using the results shown in Fig. 3, we obtain the V_{thl0}-V_{thl} characteristics (Fig. 4).

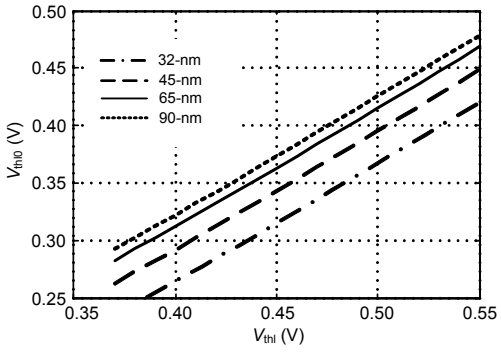

Fig. 4 V_{thl0}-V_{thl} characteristics for 32-, 45-, 65-, and 90-nm technologies

The data reveal a linear relationship between V_{thl0} and V_{thl}:

$$V_{thl}-V_{thl0}=d, \tag{5}$$

where the values of d are 0.13, 0.11, 0.09, and 0.08 for the 32-, 45-, 65-, and 90-nm technologies, respectively. These values suggest that as the channel length increases, V_{thl0} becomes closer to V_{thl}.

As the next step, to find simple expressions for the minimum of V_{gs}, which turns the transistor on, it is necessary to model the $V_{gs\,eff}$ ($=V_{gs}-V_{th}$) versus V_{gs} characteristic. Our proposed expressions for this characteristic are presented for two different cases (V_{gs} smaller or larger than V_{thl}).

Case 1: $V_{gs}\leq V_{thl}$.

$$\begin{aligned} V_{gs\,eff} &= V_{gs}-V_{th} \\ &= a_1\left[V_{gs}-\left(V_{thl}-\frac{1}{2a_1}\right)\right]^2-\frac{1}{4a_1}+V_{thl}-V_{thl0}. \end{aligned} \tag{6}$$

As shown in Fig. 5, $V_{gs\,eff}$ becomes zero when the slope of the curves, $\dfrac{\mathrm{d}V_{gs\,eff}}{\mathrm{d}V_{gs}}$, is zero. Thus, in the above equation, the sum of the last three terms on the right-hand side must be equal to zero. From this, it is possible to write

$$a_1=\frac{1}{4(V_{thl}-V_{thl0})}. \tag{7}$$

And

$$V_{gs\,eff}=a_1(V_{gs}-b_1)^2, \tag{8}$$

where b_1 is the V_{gs} at the onset of transistor conduction, i.e., the effective threshold voltage, and is given by

$$b_1=V_{thl}-\frac{1}{2a_1}=2V_{thl0}-V_{thl}. \tag{9}$$

The values of a_1 obtained from fitting the results of Fig. 5 also verify this analysis. Note that for this case, the transistor conducts when V_{gs} is larger than b_1. As the channel length increases, V_{thl0} approaches V_{thl}, making a_1 very large and b_1 very close to V_{thl}. Therefore, for long channel transistors, the conducting region $b_1<V_{gs}\leq V_{thl}$ vanishes and we have only 'on' current for $V_{gs}>V_{thl}$.

Case 2: $V_{gs}>V_{thl}$.

$$V_{gs\,eff}=a_2(V_{gs}-b_2)^2+c_2, \tag{10}$$

where

$$b_2=V_{thl}-\frac{1}{2a_2}, \tag{11}$$

$$c_2=-\frac{1}{4a_2}+V_{thl}-V_{thl0}. \tag{12}$$

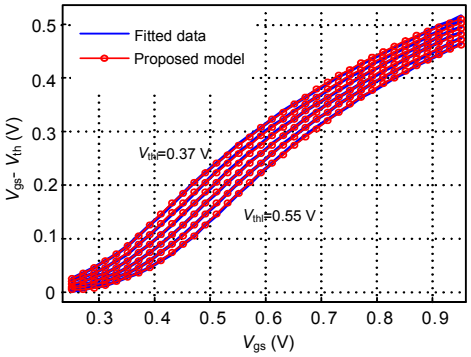

Fig. 5 ($V_{gs}-V_{th}$) versus V_{gs} characteristics for the 45-nm technology with the running parameter V_{thl} altered between 0.37 V and 0.55 V

Our simulations show that a_2 also depends on V_{thl}. By inspecting Fig. 2, we find that the slope of V_{th} versus V_{gs} for $V_{gs}>V_{thl}$ becomes smaller as the channel length increases and a_2 approaches zero, implying a weak dependence of V_{th} on V_{gs}.

2.2 Saturation region

In the saturation region ($V_{ds}>V_{dsat}$), using the BSIM3v3 model, the current-voltage characteristics may be expressed as (Cheng *et al.*, 1995)

$$I_{ds}=I_{dsat}\left(1+\frac{V_{ds}-V_{dsat}}{V_A}\right), \tag{13}$$

where I_{dsat} is the saturation current, V_{dsat} is as defined in Eq. (2), and V_A is the voltage for modeling the drain induced barrier lowering effect in the saturation region. In this work, similar to modeling V_{th} as a function of V_{gs} in the linear region, we model V_A as a function of V_{gs} in the saturation region:

$$V_A=\begin{cases} V_{As1}\left(V_{gs}-V_{th}-\dfrac{V_{dsat}}{2}\right), & V_{gs}\leq V_{thl}, \\ V_{As2}V_{gs}+V_{Ah}, & V_{gs}>V_{thl}, \end{cases} \tag{14}$$

where V_{As1}, V_{As2}, and V_{Ah} are fitting parameters.

Fig. 6 shows a comparison between V_A predicted using our model and the one obtained from the HSPICE simulation results. The comparison shows very high accuracy for the model.

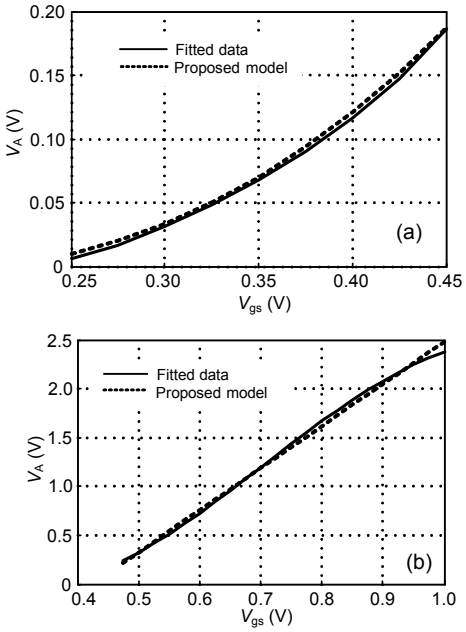

Fig. 6 V_A-V_{gs} characteristics for the 45-nm technology for $V_{gs}\leq V_{thl}$ (a) and $V_{gs}>V_{thl}$ (b)

In Fig. 7, the I_{ds}-V_{ds} characteristics with V_{gs} as the running parameter are depicted for the 45-nm technology. As observed, the results of the proposed model closely match the HSPICE results for wide ranges of V_{gs} and V_{ds}. To quantify this, we use multi-point percent mean absolute deviation (PMAD) between the actual and predicted curves (Chiulli, 1999). For calculating the PMAD values, the absolute value of the difference between the actual and predicted values of data is divided by the actual value for every data point. Then, the results for all data points are added and divided by the number of data points (Chiulli, 1999). The total PMAD for all the regions is 1.8% for the 45-nm technology. As will be seen later, this high accuracy helps us in accurately modeling the read SNM. The PMAD values for different regions are also listed in Table 1, showing that the PMAD values are very low for $V_{gs}>V_{thl}$ but rather high for $V_{gs}\leq V_{thl}$. The reason why they are larger for $V_{gs}\leq V_{thl}$ is that the current amplitude is low in this (narrow) region. This error will not have a major impact on the accuracy of the read SNM modeling.

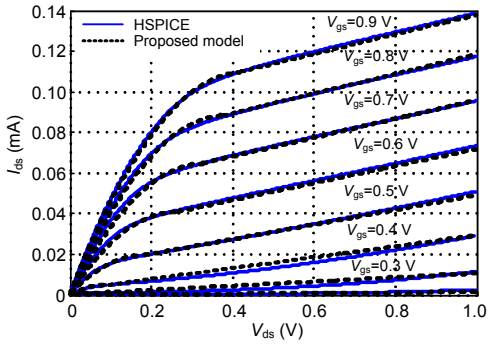

Fig. 7 I_{ds}-V_{ds} characteristic for 45-nm technology using our proposed model

Table 1 PMAD values for different regions of the I_{ds}-V_{ds} characteristic curve for the 45-nm technology

Region	PMAD (%)	Region	PMAD (%)
$V_{gs}\leq V_{thl}$		$V_{gs}>V_{thl}$	
$V_{ds}\leq V_{dsat}$	9.9	$V_{ds}\leq V_{dsat}$	1.7
$V_{ds}>V_{dsat}$	23.6	$V_{ds}>V_{dsat}$	1.2

PMAD: percent mean absolute deviation

Finally, note that the body effect as well as the temperature and process variation effects may be incorporated in the model. For this purpose, existing formulae in the literature which model these effects may be included in the model. Also, note that according to our simulation results, the changes in the model parameters are negligible in the presence of typical variations (see Section 4). By typical variations, we mean that the changes of the parameter are within, typically (e.g., in the case of threshold voltage), 20% of its nominal value. The variations correspond to three times of the standard deviation.

2.3 Parameter extraction

The model parameters may be extracted by choosing the sample points shown on the *I-V* curves in Fig. 8. Substituting the expression for V_{gseff} given by Eq. (8) into Eq. (1) and considering that V_{ds} is the same for points 1, 2, and 3, b_1 can be found as

$$b_1=\frac{\dfrac{V_{gs1}^2-V_{gs2}^2}{I_1-I_2}-\dfrac{V_{gs1}^2-V_{gs3}^2}{I_1-I_3}}{2\left(\dfrac{V_{gs1}-V_{gs2}}{I_1-I_2}-\dfrac{V_{gs1}-V_{gs3}}{I_1-I_3}\right)}. \tag{15}$$

Similarly, by substituting the expression for V_{gs}-V_{th} given by Eq. (10) into Eq. (1) and considering that V_{ds}

is the same for points 1, 4, and 5, b_2 can be obtained as

$$b_2=\frac{\dfrac{V_{gs1}^2-V_{gs4}^2}{I_1-I_4}-\dfrac{V_{gs1}^2-V_{gs5}^2}{I_1-I_5}}{2\left(\dfrac{V_{gs1}-V_{gs4}}{I_1-I_4}-\dfrac{V_{gs1}-V_{gs5}}{I_1-I_5}\right)}. \tag{16}$$

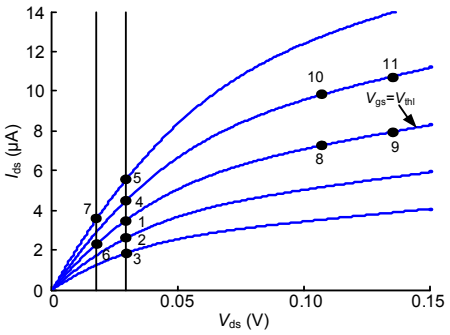

Fig. 8 Sample points on the I_{ds}-V_{ds} characteristic curve for the extraction of parameters

After obtaining b_1 and b_2, we can obtain V_{thl0} and a_2 from Eqs. (9) and (11), respectively. Next, a_1 can be computed from Eq. (7). The parameter values for $\mu_{eff}C_{ox}W/L$ and $E_{sat}L$ can also be obtained from the technology file for the given technology. To increase the accuracy, the values of these parameters may, however, be computed from the *I-V* curves in Fig. 8. Noting that the values of V_{gs} and V_{th} for points 5 and 7 in this figure are the same and using Eq. (1), one may obtain the first parameter as

$$\frac{1}{2}\mu_{eff}C_{ox}\frac{W}{L}=\frac{I_5\left(\dfrac{1}{V_{ds5}}+\dfrac{1}{E_{sat}L}\right)-I_7\left(\dfrac{1}{V_{ds7}}+\dfrac{1}{E_{sat}L}\right)}{V_{ds5}-V_{ds7}}. \tag{17}$$

Similarly, note that the values of V_{gs} and V_{th} for points 5 and 7 as well as 1 and 6 are the same, and that the values of V_{ds} are equal for points 1 and 5 as well as 6 and 7. Using Eq. (1), we determine the second parameter as

$$E_{sat}L=\frac{(I_1-I_5)-(I_6-I_7)}{\dfrac{I_1-I_5}{V_{ds1}}-\dfrac{I_6-I_7}{V_{ds6}}}. \tag{18}$$

To obtain V_{As1}, we choose points 8 and 9, which have the same V_{gs} (V_{gs}=V_{thl}). Using Eqs. (13) and (14), we may write

$$V_{As1}=\mu_{eff}C_{ox}\frac{W}{L}\frac{V_{ds8}-V_{ds9}}{I_8-I_9}\frac{V_{dsat8}}{V_{dsat8}/(E_{sat}L)+1}. \tag{19}$$

For calculating V_{As2}, we consider points 8, 9, 10, and 11. Since the values of V_{gs} and V_{thl} are equal for points 10 and 11 as well as points 8 and 9, the corresponding values of V_{dsat} are also equal. Using Eqs. (13) and (14), and considering the fact that the values of V_{ds} are equal at points 8 and 10 as well as 9 and 11, it is possible to write

$$V_{As2}=\frac{I_{dsat8}\dfrac{V_{ds8}-V_{ds9}}{I_8-I_9}-I_{dsat10}\dfrac{V_{ds10}-V_{ds11}}{I_{10}-I_{11}}}{V_{gs8}-V_{gs10}}. \tag{20}$$

Finally, V_{Ah} may be computed from the continuity condition of V_A defined by Eq. (14) when V_{gs}=V_{thl}.

Note that only b_1, b_2, V_{AS1}, and V_{AS2} are extracted from the *I-V* characteristics for each technology. All other parameters are obtained either from these parameters or from the technology file. Fig. 9 illustrates the flowchart for obtaining the drain current as a function of gate and drain voltages.

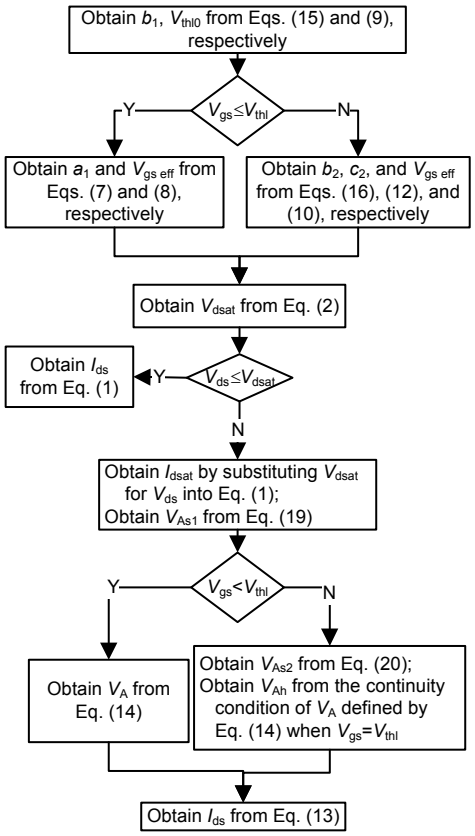

Fig. 9 Flowchart for obtaining I_{ds} for given V_{gs} and V_{ds}

3 Read static noise margin calculation

In this section, we use the analytical model obtained for the *I-V* characteristics of the transistor to derive expressions for the read SNM of a 6T SRAM cell (Fig. 10).

As shown in Fig. 11, for calculating the read SNM, the control signals of WL, BL, and BLC must be set to V_{dd}, and a voltage source should be applied to V_L to obtain the DC transfer characteristics (solid line in Fig. 12). According to Fig. 12, which shows V_R versus V_L, four different regions are specified. In region 1, AR is off and NR is in the saturation region with V_{gs} less than V_{thln} while PR is in the linear region with V_{sg} larger than $|V_{thlp}|$. In regions 3 and 4, NR is in the linear mode with V_{gs} greater than V_{thln}, while AR is in the saturation region with V_{gs} greater than V_{thln}. PR is in the saturation region with V_{sg} less than $|V_{thlp}|$ in region 3 and is off in region 4. We must also have the other DC transfer characteristics, which are the mirror of the main characteristics. This curve (dashed line in Fig. 12) is obtained in the same way except that a voltage source is applied to V_R.

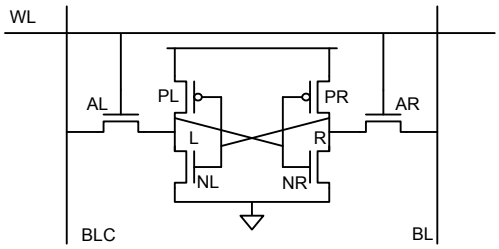

Fig. 10 A conventional 6T SRAM cell

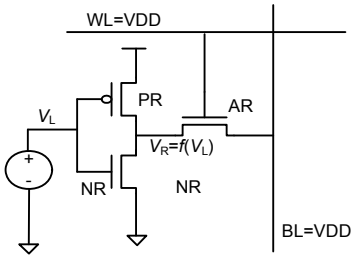

Fig. 11 SRAM cell configuration for calculating forward DC transfer characteristics ($V_R=f(V_L)$) for read SNM calculation

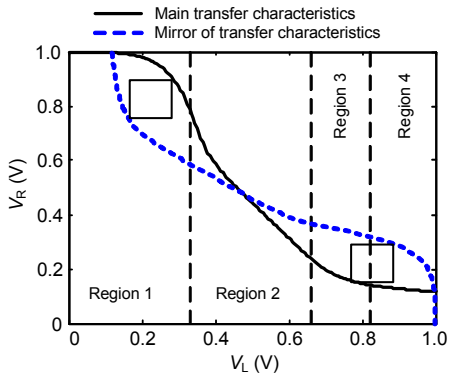

Fig. 12 Butterfly curve in the read mode

SNM may be calculated from the maximum side length of the square whose vertices lie on the curves. As shown in Fig. 12, there are two such squares. For the asymmetric case in which the left and right transistors are not the same, the minimum side length is considered as SNM. Here, we show how to calculate the maximum side length of the left square. The right one can be found easily by exchanging the corresponding right and left values in the final expression of SNM. For the left square, one of the vertices is in region 1 of the main curve and the others are in region 3 or 4 of the mirrored curve (Fig. 12). Thus, to make the calculation easier, it is better to find V_L versus V_R in regions 3 and 4. Also, since none of the vertices of the maximum square encompassed in the butterfly curves is placed in region 2, we are not concerned about the operational modes of the transistors in this region. This assumption holds true in the presence of process variations (Bhavnagarwala *et al.*, 2001; Kang *et al.*, 2007).

In fact, the intersection of the two characteristics forming the butterfly characteristic plot (Fig. 12), which occurs in region 2, is a function of the ratios of the threshold voltages of the left and right NMOS/PMOS transistors. Changes in the ratios due to the variations only partially shift region 2 (including the intersection) to the left or right in the butterfly characteristic plot without changing the regions in which the vertices of the maximum square are located. The shift causes the size of the side length of the square to change. Also, it may change the (left or right) side in which a smaller square occurs. The smaller square is used to determine the SNM.

Next, we calculate SNM using the analytical *I-V* equations in the three regions of interest.

3.1 Calculation of V_L-V_R in region 1

Before applying Kirchhoff's current law (KCL) at node *R*, we use some approximations. For NR, since V_{gs} is less than V_{thln}, V_{dsat} is very small, and hence, we may write

$$1+\frac{V_{\text{dsat NR}}}{E_{\text{sat}}L}\cong 1. \tag{21}$$

V_{R} is also close to V_{dd}, making V_{ds} of PR very small, and hence, we have

$$1+\frac{V_{\text{ds PR}}}{E_{\text{sat}}L}\cong 1. \tag{22}$$

With these approximations, using Eqs. (1) and (13), the current equations for these transistors may be written as

$$\begin{aligned} I_{\text{ds PR}} &= K_{\text{PR}}[a_{\text{2PR}}(V_{\text{dd}}-V_{\text{L}}-b_{\text{2PR}})^2+c_{\text{2PR}} \\ &\quad -\frac{1}{2}(V_{\text{dd}}-V_{\text{R}})](V_{\text{dd}}-V_{\text{R}}), \end{aligned} \tag{23}$$

$$\begin{aligned} I_{\text{ds NR}} &= K_{\text{NR}}a_{\text{1NR}}(V_{\text{L}}-b_{\text{1NR}})^2 \\ &\cdot\left[\left(\frac{1}{2}V_{\text{As1NR}}a_{\text{1NR}}-a_{\text{1NR}}\right)(V_{\text{L}}-b_{\text{1NR}})^2+V_{\text{R}}\right]\Big/V_{\text{As1NR}}. \end{aligned} \tag{24}$$

Since AR is off in this region, we have

$$I_{\text{ds NR}}=I_{\text{ds PR}}. \tag{25}$$

In Eq. (24), as V_{R} is near V_{dd} and V_{L} is small and close to b_{1NR}, V_{L}–b_{1NR} is small. Thus, $I_{\text{ds NR}}$ may be approximated as

$$I_{\text{ds NR}}=K_{\text{NR}}a_{\text{1NR}}(V_{\text{L}}-b_{\text{1NR}})^2V_{\text{R}}/V_{\text{As1NR}}. \tag{26}$$

From Eqs. (23)–(26), we can obtain V_{R} as a function of V_{L}:

$$V_{\text{R}}=f(V_{\text{L}}). \tag{27}$$

After solving the equations and finding the analytical expression for $f(V_{\text{L}})$, we see that $(V_{\text{L}}-b_{\text{1NR}})^2$ is the dominant term and hence we may approximate the function by

$$f(V_{\text{L}})\approx V_{\text{dd}}-m(V_{\text{L}}-b_{\text{1NR}})^2, \tag{28}$$

where m can be found from the above equation by taking its second derivative with respect to V_{L} and evaluating it at any point in region 1. For simplicity, we choose the point of $V_{\text{L}}=b_{\text{1NR}}$, and obtain

$$\begin{aligned} m &= -\frac{1}{2}\frac{\partial^2 f(V_{\text{L}})}{\partial V_{\text{L}}^2}\Big|_{V_{\text{L}}=b_{\text{1NR}}} \\ &= \frac{K_{\text{NR}}a_{\text{1NR}}}{K_{\text{PR}}V_{\text{As1NR}}[a_{\text{2PR}}(V_{\text{dd}}-b_{\text{1NR}}-b_{\text{2PR}})^2+c_{\text{2PR}}]}. \end{aligned} \tag{29}$$

3.2 Calculation of V_{L}-V_{R} in regions 3 and 4

To obtain V_{L}-V_{R} in regions 3 and 4, we need a simple equation for the current of AR in the saturation region. Considering that $V_{\text{ds}}=V_{\text{gs}}$ for AR, we can rewrite the drain current of AR as

$$I_{\text{ds AR}}=\frac{1}{2}k_{\text{AR}}E_{\text{sat}}L\frac{Z_1}{Z_2^2}Z_3, \tag{30}$$

where

$$Z_1=\frac{[a_{\text{2AR}}(V_{\text{gs AR}}-b_{\text{2AR}})^2+c_{\text{2AR}}]^2}{V_{\text{As2AR}}V_{\text{gs AR}}+V_{\text{Ah AR}}}, \tag{31}$$

$$Z_2=E_{\text{sat}}L+a_{\text{2AR}}(V_{\text{gs AR}}-b_{\text{2AR}})^2+c_{\text{2AR}}, \tag{32}$$

$$\begin{aligned} Z_3 &= [(V_{\text{As2AR}}+1)V_{\text{gs AR}}+V_{\text{Ah AR}}]Z_2 \\ &\quad -E_{\text{sat}}L[a_{\text{2AR}}(V_{\text{gs AR}}-b_{\text{2AR}})^2+c_{\text{2AR}}]. \end{aligned} \tag{33}$$

Note that the variation of Z_1 by $V_{\text{gs AR}}$ is negligible, and hence, for our calculations we use its value at $V_{\text{gs AR}}=b_{\text{2AR}}$, which is

$$Z_1=\frac{c_{\text{2AR}}^2}{V_{\text{As2AR}}b_{\text{2AR}}+V_{\text{Ah AR}}}. \tag{34}$$

Z_2 is also approximately constant for $V_{\text{gs AR}}$ between V_{thl} and b_{2AR} and increases slightly by increasing $V_{\text{gs AR}}$ for $V_{\text{gs AR}}>V_{\text{thl}}$. We can also assume Z_2^2 constant, but to increase the accuracy, we may use a geometric average by using the values of Z_2 evaluated at two boundary V_{gs} values as

$$\begin{aligned} Z_2^2 &\approx Z_2\Big|_{V_{\text{gs AR}}=b_{\text{2AR}}}\cdot Z_2\Big|_{V_{\text{gs AR}}=V_{\text{thl}}}=(E_{\text{sat}}L+c_{\text{2AR}}) \\ &\cdot[E_{\text{sat}}L+a_{\text{2AR}}(V_{\text{thl}}-b_{\text{2AR}})^2+c_{\text{2AR}}]. \end{aligned} \tag{35}$$

The simulations also show that $I_{\text{ds AR}}$ has a linear relationship with $V_{\text{gs AR}}$. By substituting the approximate values of Z_1 and Z_2^2 into Eq. (30) and taking the derivative with respect to $V_{\text{gs AR}}$ at a point like b_2, it is possible to obtain the slope of $I_{\text{ds AR}}$ with respect to $V_{\text{gs AR}}$, denoted by s_{AR}, as

$$s_{\mathrm{AR}}=\frac{\partial I_{\mathrm{ds\,AR}}}{\partial V_{\mathrm{gs\,AR}}}\Big|_{V_{\mathrm{gs\,AR}}=b_{\mathrm{2AR}}}=\frac{1}{2}K_{\mathrm{AR}}E_{\mathrm{sat}}L \cdot c_{\mathrm{2AR}}^2(1+V_{\mathrm{As\,2AR}})(V_{\mathrm{As\,2AR}}b_{\mathrm{2AR}}+V_{\mathrm{Ah\,AR}})^{-1} \cdot[E_{\mathrm{sat}}L+a_{\mathrm{2AR}}(V_{\mathrm{thl}}-b_{\mathrm{2AR}})^2+c_{\mathrm{2AR}}]^{-1}. \quad (36)$$

Substituting V_{gs} by V_{thl} in Eq. (10) and noting that V_{thl0} is the threshold voltage for V_{gs} equal to V_{thl},

$$a_2(V_{\mathrm{thl}}-b_2)^2+c_2=V_{\mathrm{thl}}-V_{\mathrm{thl0}}. \quad (37)$$

As discussed before, the right-hand side is very small and approaches zero as the channel length increases. Therefore, we can approximate s_{AR} as

$$s_{\mathrm{AR}}=\frac{1}{2}K_{\mathrm{AR}}\frac{c_{\mathrm{2AR}}^2(1+V_{\mathrm{As\,2AR}})}{V_{\mathrm{As\,2AR}}b_{\mathrm{2AR}}+V_{\mathrm{Ah\,AR}}}. \quad (38)$$

The simulations show that, for the three technologies,

$$b_2+\frac{V_{\mathrm{Ah}}}{V_{\mathrm{As2}}}\approx 1. \quad (39)$$

Thus,

$$s_{\mathrm{AR}}=\frac{1}{2}K_{\mathrm{AR}}c_{\mathrm{2AR}}^2\left(1+\frac{1}{V_{\mathrm{As\,2AR}}}\right). \quad (40)$$

Since Z_1 and Z_2 are almost constant and $I_{\mathrm{ds\,AR}}$ has a linear relationship with V_{gs}, it may be concluded that Z_3 should have a linear dependence on V_{gs}. To find this linear relation, we rewrite Eq. (33) as

$$Z_3=(V_{\mathrm{As\,2AR}}+1)Z_2 \cdot\left(V_{\mathrm{gs\,AR}}+\frac{V_{\mathrm{Ah\,AR}}-E_{\mathrm{sat}}L(Z_2-E_{\mathrm{sat}}L)/Z_2}{V_{\mathrm{As\,2AR}}+1}\right). \quad (41)$$

Using the value of Z_2 evaluated at $V_{\mathrm{gs\,AR}}=b_{\mathrm{2AR}}$ yields

$$Z_3=(V_{\mathrm{As\,2AR}}+1)Z_2 \cdot\left(V_{\mathrm{gs\,AR}}+\frac{V_{\mathrm{Ah\,AR}}-E_{\mathrm{sat}}Lc_{\mathrm{2AR}}/(E_{\mathrm{sat}}L+c_{\mathrm{2AR}})}{V_{\mathrm{As\,2AR}}+1}\right). \quad (42)$$

The value of $I_{\mathrm{ds\,AR}}$ at $V_{\mathrm{gs\,AR}}=0$, denoted by h_{AR}, is obtained from

$$h_{\mathrm{AR}}=s_{\mathrm{AR}}\frac{V_{\mathrm{Ah\,AR}}-E_{\mathrm{sat}}Lc_{\mathrm{2AR}}/(E_{\mathrm{sat}}L+c_{\mathrm{2AR}})}{V_{\mathrm{As\,2AR}}+1}. \quad (43)$$

Finally, $I_{\mathrm{ds\,AR}}$ versus $V_{\mathrm{gs\,AR}}$ can be estimated as a linear function, given by

$$I_{\mathrm{ds\,AR}}=s_{\mathrm{AR}}V_{\mathrm{gs\,AR}}+h_{\mathrm{AR}}. \quad (44)$$

In region 3, PR is in the saturation region with V_{sg} less than $|V_{\mathrm{thlp}}|$ and is off in region 4. In these two regions, the AR and NR currents are large while the PR current is small and can be ignored for simplicity. Here, as discussed in the beginning of this section, it is better to find V_{L} versus V_{R} for the read SNM calculation.

$$I_{\mathrm{ds\,AR}}=I_{\mathrm{ds\,NR}}, \quad (45)$$

$$K_{\mathrm{AR}}E_{\mathrm{sat}}LV_{\mathrm{R}}[a_{\mathrm{2NR}}(V_{\mathrm{L}}-b_{\mathrm{2NR}})^2+c_{\mathrm{2NR}}] =(K_{\mathrm{AR}}E_{\mathrm{sat}}L/2-a_{\mathrm{2AR}})V_{\mathrm{R}}^{\,2}+E_{\mathrm{sat}}L(s_{\mathrm{AR}}V_{\mathrm{dd}}+h_{\mathrm{AR}}) +(s_{\mathrm{AR}}V_{\mathrm{dd}}+h_{\mathrm{AR}}-E_{\mathrm{sat}}Ls_{\mathrm{AR}})V_{\mathrm{R}}. \quad (46)$$

From the above equations, V_{L} may be obtained. To simplify this equation, we note that for high V_{gs}, $V_{\mathrm{gs\,eff}}$ has a linear relationship with V_{gs} (Fig. 5), so $V_{\mathrm{gs\,eff\,NR}}=a_{\mathrm{2NR}}(V_{\mathrm{L}}-b_{\mathrm{2NR}})^2+c_{\mathrm{2NR}}$ can be approximated by a linear relationship as

$$V_{\mathrm{gs\,eff\,NR}}=\alpha V_{\mathrm{L}}+\beta, \quad (47)$$

where α and β may be obtained from evaluating the function at any point denoted by $V_{\mathrm{L}m}$ in these regions (regions 3 and 4):

$$\alpha=2a_{\mathrm{2NR}}(V_{\mathrm{L}m}-b_{\mathrm{2NR}}), \quad (48)$$

$$\beta=a_{\mathrm{2NR}}(b_{\mathrm{2NR}}^2-V_{\mathrm{L}m}^2)+c_{\mathrm{2NR}}. \quad (49)$$

The best point to minimize the approximation error for $V_{\mathrm{L}m}$ is the beginning of region 3. For obtaining $V_{\mathrm{L}m}$, noting V_{R} is small (and hence, $1+V_{\mathrm{R}}/(E_{\mathrm{sat}}L)\approx 1$), we may rewrite Eq. (45) as

$$\left(V_{\mathrm{R}}-V_{\mathrm{gs\,eff\,NR}}-s_{\mathrm{AR}}/K_{\mathrm{NR}}\right)^2=U, \quad (50)$$

where

$$U=\left(V_{\mathrm{gs\,eff\,NR}}+s_{\mathrm{AR}}/K_{\mathrm{NR}}\right)^2-\frac{2}{K_{\mathrm{NR}}}(s_{\mathrm{AR}}V_{\mathrm{dd}}+h_{\mathrm{AR}}). \quad (51)$$

Taking the second derivative of Eq. (50) with respect to V_L, we obtain

$$2[V_R' - 2a_{2NR}(V_L - b_{2NR})]^2 + (V_R'' - 2a_{2NR}) \cdot \left(V_R - V_{gs\,eff\,NR} - s_{AR}/K_{NR}\right) = U''. \quad (52)$$

Here, we need the expression for V_R as a function of V_L. At the beginning of region 3, NR is at the boundary of linear and saturation regions, and hence, $V_{ds\,NR}$ is equal to $V_{dsat\,NR}$.

$$V_{ds\,NR} = V_{dsat\,NR} = V_{gs\,eff\,NR}. \quad (53)$$

Using the approximate equation for $V_{dsat\,NR}$, it is possible to write

$$V_R = a_{2NR}(V_L - b_{2NR})^2 + c_{2NR}. \quad (54)$$

Taking the first and second derivatives of Eq. (54) with respect to V_L, we obtain

$$V_R' = 2a_{2NR}(V_L - b_{2NR}), \quad (55)$$

$$V_R'' = 2a_{2NR}. \quad (56)$$

Substituting Eqs. (55) and (56) into Eq. (52), we have

$$U'' = 0. \quad (57)$$

Thus, V_{Lm} is obtained easily as

$$V_{Lm} = b_{2NR} + \sqrt{-\frac{m_{AR} + K_{NR}c_{2NR}}{3K_{NR}a_{2NR}}}. \quad (58)$$

Having found V_{Lm}, we can obtain α and β from Eqs. (48) and (49), respectively. Finally, substituting $V_{gs\,eff\,NR}$ from Eq. (47) into Eq. (46), the relationship between V_L and V_R can be easily achieved. Finally, note that V_{Lm} could have been obtained by solving Eqs. (50) and (54). Since solving these equations was very difficult, we took the approach explained here.

3.3 Read SNM calculation

As is evident from the butterfly curves of HSPICE simulations and the proposed technique (Fig. 13), the error is very small. The V_L-V_R relationship obtained in the three regions is simple and hence may be used for the read SNM calculation. As shown in Fig. 13, for calculating SNM we can intersect the normal curve and the mirrored one by the line $V_R=V_L+a$ (Bhavnagarwala *et al.*, 2001).

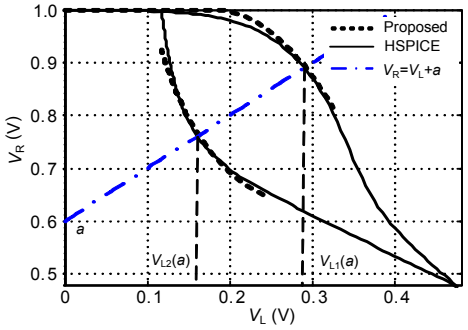

Fig. 13 Butterfly curve in the read mode for calculating read SNM

Note that to obtain the mirrored curve in region 1, we could use the formulae in regions 3 and 4, but we should replace the parameters of the left transistors of AL and NL by those of the right transistors of AR and PR and do mirroring. For each a, this line intersects the normal and mirrored curves at two points, denoted by (V_{L1}, V_{R1}) and (V_{L2}, V_{R2}). The points are determined by intersecting this line by the butterfly curves. The SNM may be found from the maximum separation of the points or side length of the square encompassed in the butterfly curves as

$$\text{SNM}=\max(\text{side length}), \quad (59)$$

where

$$\text{side length}=V_{L1}(a)-V_{L2}(a). \quad (60)$$

Using the expressions obtained in the previous section, an analytical relation for the SNM (side length) is obtained. Fig. 14 illustrates the steps that should be taken for SNM calculation.

1. Obtain m from Eq. (29)
2. Obtain $V_R=f(V_L)$ in region 1 from Eqs. (28) and (29)
3. Obtain V_{L1} by intersecting $V_R=V_L+a$ by the $V_R=f(V_L)$ in region 1
4. Obtain V_{Lm} from Eq. (58)
5. Obtain α and β from Eqs. (48) and (49), respectively
6. Obtain $V_{gs\,eff\,NR}$ from Eq. (47) and insert it into Eq. (46)
7. Obtain $V_L=f(V_R)$ from Eq. (46)
8. Replace the parameters of the left transistors by those of the right transistors and do mirroring to find $V_R=g(V_L)$ in regions 3 and 4
9. Obtain V_{L2} by intersecting $V_R=V_L+a$ by the $V_R=g(V_L)$ in regions 3 and 4
10. Obtain a by setting to zero the differential of V_{L1}- V_{L2} with respect to a
11. Obtain SNM from Eqs. (59) and (60)

Fig. 14 Static noise margin (SNM) calculation steps

4 Results and discussion

In this section, we discuss the results of the analytical SNM model for different technologies. The results also include the study of the effects of process variations, NBTI, and the minimum supply voltage required for a target yield in the presence of the process variations. The read SNMs calculated using the proposed model and the HSPICE simulations as a function of the β ratio (the relative strength of the pull down transistors to access transistors) are compared (Fig. 15). The results are presented for four CMOS technologies of 32-, 45-, 65-, and 90-nm. As shown in this figure, our read SNM model has very high accuracy. The maximum errors were 1.5%, 1.7%, 1.4%, and 1.5% for the 32-, 45-, 65-, and 90-nm technologies, respectively. The errors are much less than those reported in Chen *et al.* (2007) for the 70-nm technology (maximum 8%). In Bhavnagarwala *et al.* (2001), the maximum error of the model was more than 3% for a 0.18-μm process. The model in Bhavnagarwala *et al.* (2001) also suffers from complexity and relies on fixed point iteration to reach self-consistency. This shows higher accuracy for our proposed SNM model. The high level of accuracy makes the model appropriate for practical designs. In fact, using the flowcharts given in Figs. 9 and 14, we can calculate the SNM much faster than with HSPICE, without requiring the type of numerical calculations performed in HSPICE simulations.

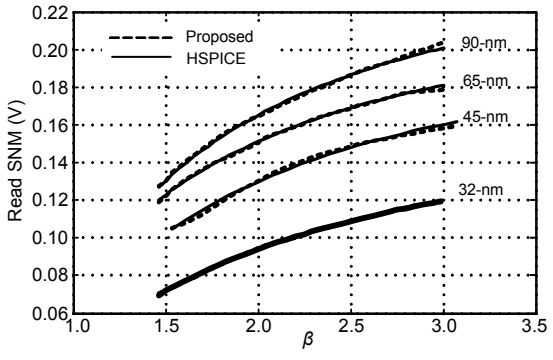

Fig. 15 Read SNM curves with respect to the β ratio for 32-, 45-, 65-, and 90-nm technologies

Next, we study the accuracy of the model in the presence of process variations and negative bias temperature instability (NBTI) effect. We consider threshold voltage variations and assume a Gaussian distribution for the threshold voltage (Agarwal and Nassif, 2008). Note that random dopant fluctuation (RDF) usually dominates the total threshold voltage variation (Orshansky *et al.*, 2008). The standard deviation for this distribution, denoted by $\sigma V_{\text{th,RDF}}$, is given by (Li *et al.*, 2009)

$$\sigma V_{\text{th,RDF}} = 3.19\times10^{-8}\frac{t_{\text{ox}}N_{\text{A}}^{0.401}}{\sqrt{WL}}, \tag{61}$$

where t_{ox} is the oxide thickness and N_{A} is the doping density. For the 32-nm technology, the 3σ value (for the minimum size transistor) becomes slightly more than 10% of the nominal threshold voltage. Other sources of variations may increase this value. To consider the worst case condition, we set 3σ=20% as the nominal value. The variations, which are induced mainly by RDF, are highly uncorrelated (i.e., independent) (Agarwal and Nassif, 2008).

The values obtained from the distributions were applied to V_{thl} of transistors in the proposed model and V_{th0} in the HSPICE simulations. The other fitting parameters were assumed to be constant. Also, we considered the NBTI effect which is responsible for the threshold voltage increase of PMOS transistors over time when a negative bias is applied (Schroder and Babcock, 2003). Previous works have shown that the read SNM was degraded by the NBTI effect (Kang *et al*., 2007). Fig. 16 shows the probability distribution function (PDF) of the read SNM calculated according to the HSPICE simulations and our proposed model under process variations and NBTI in the 32-nm technology. The results obtained from 10000 Monte Carlo simulations showed that our models (SNM and *I*-*V*) had high accuracy in the presence of both process variation and NBTI (aging effect) while it was evaluated in a very short period of time due to its analytical nature. The computer runtime was 0.23 and 48949 s when our analytical model and HSPICE simulations were used, respectively, in the study of the SNM variation in the presence of process variations. The high accuracy of the model makes it a much more efficient technique for calculating the read SNM than HSPICE simulations when we study the impact of process variations and NBTI on the read SNM of the SRAM cell. Note that both the transistor width (*W*) and length (*L*) also have variations in the presence of the process variations. These

variations are highly correlated, giving rise to small impacts on stability metrics such as read SNM (Mukhopadhyay *et al*., 2005), and hence, are ignored in this study.

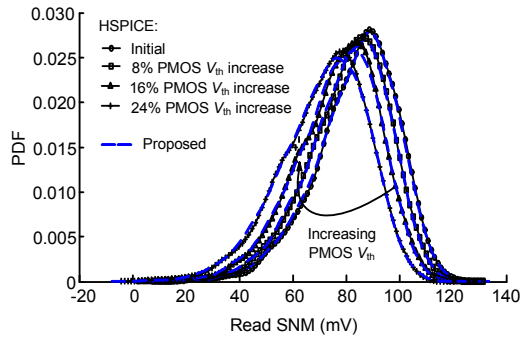

Fig. 16 Probability distribution function (PDF) of read SNM calculated using the HSPICE simulations and our proposed model under process variations and NBTI effect with 8%, 16%, and 24% increase in PMOS threshold voltage in 32-nm technology

One of the applications of the read SNM model is to obtain the minimum supply voltage that satisfies the target yield (for example, 99%) (Park *et al.*, 2010). The voltage is denoted by V_{ddmin}. In a low power design, the supply voltage should be minimized as much as possible. On the other hand, the reduction of the supply voltage may cause deterioration in the yield (Park *et al.*, 2010). We investigated the effect of V_{dd} scaling on the yield in the presence of process variations in the 32-nm technology. The results of this study performed using both the model and HSPICE simulations are shown in Fig. 17. Since for higher V_{dd} failure events rarely occur, 50000 Monte Carlo simulations were needed for the yield calculation. The figure which plots the SNM yield versus the supply voltage again shows very good accuracy for the model. A target read SNM of 27 mV was assumed for this study. For a target yield of 99%, V_{ddmin}'s of 0.809 V and 0.812 V are predicted by the model and simulation, respectively.

5 Conclusions

In this work, an accurate model for *I-V* characteristics of sub-90-nm MOSFET in the linear and saturation regions were proposed. Contrary to the *n*th-power law, in our proposed model, the current

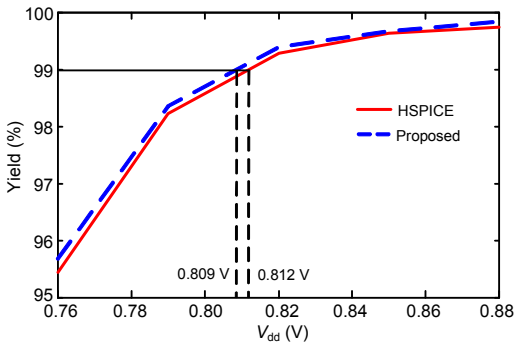

Fig. 17 Yield versus supply voltage for the 32-nm technology (a target read SNM of 27 mV was assumed)

relations with the voltages had integer powers, making it suitable for hand calculations and analysis. The accuracy of the model was verified for the 90-, 65-, 45-, and 32-nm CMOS technologies. The model showed better accuracy than the *n*th-power and BSIM3v3 models. The procedure for extracting the model parameters was also described. Next, the read SNM was calculated using the proposed *I-V* model. We used the criteria of the side length of the maximum square encompassed in the butterfly curves as the SNM. To obtain the read SNM, the voltage transfer characteristic was approximated in the regions where the vertices of the square were laid. The read SNM obtained from the approach had a maximum error of about 1.7% for the four technologies. The accuracy of the model was also verified in the presence of process variations and negative bias temperature instability (NBTI) effect. Moreover, it was shown that the model could accurately predict the minimum supply voltage required for a target yield. Note that the analytical model for the *I-V* characteristic of highly scaled transistors is expected to have wide applications to many other circuit analysis and optimization problems thanks to the integer power relation between current and voltage.

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