Journal of Zhejiang University-SCIENCE C (Computers & Electronics)
ISSN 1869-1951 (Print); ISSN 1869-196X (Online)
www.zju.edu.cn/jzus; www.springerlink.com
E-mail: jzus@zju.edu.cn

Predictive current control of multi-pulse flexible-topology thyristor AC-DC converter*

Da-min ZHANG†1, Shi-tao WANG[2], Hui-pin LIN[1], Zheng-yu LU†1

([1]*School of Electrical Engineering, Zhejiang University, Hangzhou 310027, China*)

([2]*State Grid of China Technology College, Jinan 250002, China*)

†E-mail: hqxmzj@sina.com; eeluzy@cee.zju.edu.cn

Received Oct. 14, 2012; Revision accepted Mar. 11, 2013; Crosschecked Mar. 21, 2013

Abstract: This paper proposes a novel multi-pulse flexible-topology thyristor rectifier (FTTR) that can operate over a large voltage range while maintaining a low total harmonic distortion (THD) in the input current. The proposed multi-pulse FTTR has two operating modes: parallel mode and series mode. Irrespective of the mode in which it operates, the multi-pulse FTTR maintains the same pulses in the load current. To mitigate the harmonic injection into the AC mains, the topology-switching mechanism is then proposed. In addition, predictive current control is employed to achieve fast current response in both the transience and the transitions between modes. To verify the effectiveness of the multi-pulse FTTR as well as the control scheme, performance analysis based on an 18-pulse FTTR is investigated in detail, including fault tolerance evaluation, current THD analysis based on IEEE standard, and potential applications. Finally, a simulation model and the corresponding laboratory setup are developed. The results from both simulation and experiments demonstrate the feasibility of the proposed multi-pulse FTTR as well as the control scheme.

Key words: Flexible-topology operation, Multi-pulse thyristor rectifier, Predictive current control, Fast current response, Fault tolerance evaluation

doi:10.1631/jzus.C1200283 **Document code:** A **CLC number:** TM921

1 Introduction

Owing to the high power capacity and low cost of thyristor AC-DC converters, they are still widely used in industrial applications, such as electrical arc furnace, electro-chemical process, and high-voltage direct current (HVDC) transmission (Wiechmann *et al.*, 2000; Tanaka *et al*., 2001; Rodríguez *et al*., 2005; Rezazadeh *et al*., 2010). However, the poor power factor and the harmonic current injection of the thyristor converter are of primary concern. Particularly, when the converter feeds light loads, the firing angle is very close to 90°, resulting in a heavy phase lag of the input current and more harmonic components in the AC mains. To alleviate these drawbacks of thyristor AC-DC converters, the active and the passive wave-shaping techniques were proposed by Peterson and Singh (2006). The active wave-shaping technique usually employs controlled power converters such as static var compensator (STATCOM) to provide the reactive power and compensation for the harmonics (Peterson and Singh, 2006). The voltage and current waveforms produced by the controlled power converters eliminate the particular harmonics produced by the nonlinear loads. Nevertheless, the active wave-shaping technique suffers from the drawbacks of control complexity, increased cost, and losses. Consequently, the passive wave-shaping technique is an attractive alternative due to its ease of control, low cost, and simplicity. It comprises the application of the harmonic injection method (Saied and Zynal, 2007) and the multi-pulse configuration which is usually accomplished by a special coupling

* Project supported by the National Natural Science Foundation of China (No. 51177148) and the Zhejiang Key Science and Technology Innovation Group Program, China (No. 2010R50021)

transformer. In general, several six-pulse uncontrolled/controlled rectifiers are connected either in series or parallel to form a multi-pulse rectifier (Fukuda *et al*., 2008; Garg *et al*., 2009; Arvindan and Guha, 2011). As the input currents with different phase angles are overlapped, near sinusoidal input current is produced with low total harmonic distortion (THD) and low ripple contents. Zargari *et al*. (1997) proposed an 18-pulse AC-DC converter with three standard 6-pulse thyristor rectifiers connected in series. The upper two 6-pulse thyristor rectifiers are each paralleled by a gate-turn-off (GTO). By changing the multi-pulse configuration with the help of GTOs, the input current THD and the power quality are improved to some extent. However, the output voltage is not controlled 'in a continuous way' but 'in step' when the upper rectifiers are short out. The step change of the output voltage may not be good for the system reliability since large du/dt may cause serious electromagnetic interference (EMI) and activate an overvoltage protection, resulting in an undesirable failure of the rectifiers. Peterson and Singh (2009) proposed an 18-pulse parallel thyristor AC-DC converter for the load current control. Based on the load conditions, a pulse control strategy is presented to disable or enable the rectifier(s) from the high load current. In this way, the input current THD and the power factor as well as the overall system efficiency are improved. However, the same drawbacks exist in the 18-pulse parallel rectifier as in the 18-pulse series rectifier. On one hand, the load current bears step changes when the top and middle rectifiers are bypassed. On the other hand, the phase-shift angle between the secondary windings is 20° when the 18-pulse parallel rectifier operates in the 12-pulse configuration.

To reduce the input current THD and improve the power quality, more-pulse rectifiers were proposed and 18-, 24-, 36-, and 48-pulse configurations are commonly used (Choi *et al*., 2003; Singh and Gairola, 2007; Kocman *et al*., 2010; Young *et al*., 2012). Nevertheless, the aforementioned multi-pulse rectifiers have a narrow operating voltage range for the purpose of reducing the THD. This paper proposes a novel multi-pulse flexible-topology thyristor rectifier (FTTR) that can operate over a large voltage range while keeping low current THD. The topology-switching mechanism is then devised to improve the input current THD as well as the power factor of the system. The proposed multi-pulse FTTR has two operating modes; irrespective of the mode in which it operates, it always maintains the same pulses in the load current. In addition, the predictive current control strategy is proposed to achieve a fast current response. To verify the effectiveness of the proposed multi-pulse FTTR as well as the control scheme, detailed analyses of an 18-pulse FTTR are developed in this paper.

2 Schematic of the proposed 18-pulse flexible-topology thyristor rectifier (FTTR)

In this section, the novel 18-pulse FTTR is proposed (Fig. 1). The detailed performance analysis of the rectifier is carried out, including the description of the predictive current control, the topology-switching mechanism, and the parallel and series modes operations. It consists of a phase-shifted transformer with three isolated secondary windings. The phase-shifted angle among the secondary windings is designed to be 20° for harmonic cancellation. Each of the secondary windings feeds a standard 6-pulse thyristor rectifier, and the three 6-pulse rectifiers are connected with four additional diodes and two GTOs (functioned as switches). Compared to the 18-pulse series thyristor rectifier proposed by Zargari *et al*. (1997), the 18-pulse FTTR in this paper only increases two extra diodes, and thus the overall cost does not increase noticeably.

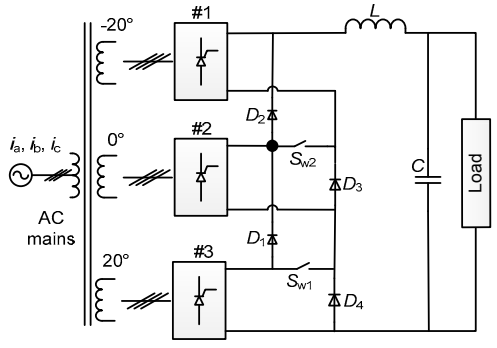

Fig. 1 Schematic of the proposed 18-pulse flexible-topology thyristor rectifier (FTTR)

The corresponding equivalent diagrams of the 18-pulse FTTR which operates in both modes are depicted in Fig. 2.

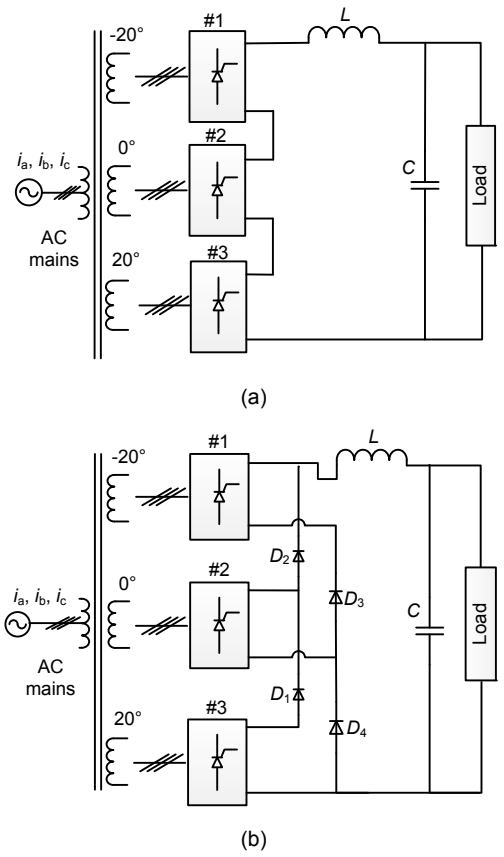

Fig. 2 Equivalent diagrams of the 18-pulse FTTR
(a) Series mode operation; (b) Parallel mode operation

With the auxiliary GTOs, named S_{w1} and S_{w2}, the 18-pulse FTTR is able to operate in either the series mode or the parallel mode. If S_{w1} and S_{w2} are turned on, the 18-pulse FTTR will operate in the series mode. Otherwise, the 18-pulse FTTR will operate in the parallel mode. Both operating modes will be accomplished by the predictive current control.

2.1 Description of the predictive current control

In this section, the principle of the predictive current control with regards to the 18-pulse FTTR is developed. The average current control of the aforementioned multi-pulse rectifiers is usually accomplished by a linear proportional integral (PI) controller (Zargari *et al*., 1997; Hao *et al*., 2007; Wiechmann *et al*., 2008). In this case, the fast dynamic response cannot be achieved since the average load current is usually obtained via a low-pass filter (Fig. 3). The low-pass filter will introduce a time lag and thus affects the response of the controller.

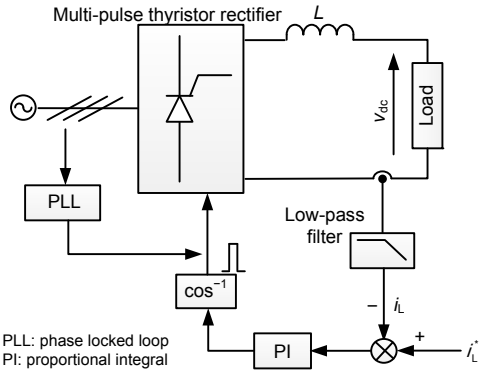

Fig. 3 Block diagram of proportional integral (PI) control of the multi-pulse thyristor rectifier

With the development of fast and powerful microprocessors, the predictive control strategy has been capturing more and more attention (Yang *et al*., 2006; Bao *et al*., 2011). Straightforward concepts, fast response, and powerful ability in coping with nonlinear characteristics all make it suitable for power electronics (Rodríguez *et al*., 2007; Schroder, 2009; Geyer, 2010; Ahmed *et al*., 2011; Yaramasu *et al*., 2012; Lim *et al*., 2013). A conceptually new predictive current control method is presented in Srdic and Nedeljković (2011) where a standard 6-pulse thyristor AC-DC converter is investigated. This paper presents the method introduced in Srdic and Nedeljković (2011) and applies it to the proposed 18-pulse FTTR. A block diagram of the predictive current control strategy applied to the 18-pulse FTTR is shown in Fig. 4, and the current control is performed in the following steps (Rodríguez *et al*., 2007).

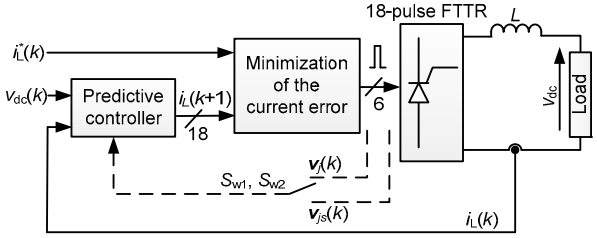

Fig. 4 Block diagram of the predictive current control

1. The operating mode (parallel or series) is selected.

2. The value of the current reference $i_L^*(k)$ is preset or obtained from an outer control loop.

3. The inductor current $i_L(k)$, the output voltage $v_{dc}(k)$, and the input line-to-line voltages are measured.

The input line-to-line voltages are used to calculate the voltage vectors ($\boldsymbol{v}_j(k)$ for the parallel mode and $\boldsymbol{v}_{js}(k)$ for the series mode).

4. The predictive current controller predicts the inductor current in the next sampling instant $i_L(k+1)$ based on the present inductor current $i_L(k)$, the present load voltage $v_{dc}(k)$, and the selected voltage vector.

5. Every voltage vector participates in the prediction of the inductor current $i_L(k+1)$, and the voltage that minimizes the current error is selected. The corresponding thyristors are then fired according to the selected voltage vector.

To achieve the prediction of the inductor current, two calculations about the voltage-time area of the DC-side inductor are required. The first one is about the maximal available inductor current increment ΔI_{Lm}, which is obtained from the voltage-time area between two adjacent crossings of the line-to-line voltages and the load voltage (Fig. 5). Here, the line-to-line voltages denoted by $\boldsymbol{v}_j$ (j=1, 2, …, 18) are defined as the voltage vectors with values being determined according to the operating mode, as can be seen in Section 2.3.

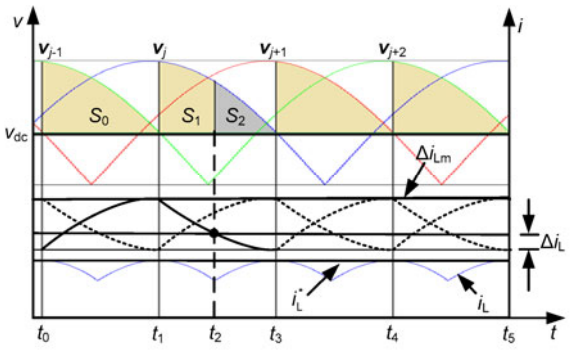

Fig. 5 Principle of the predictive current control

Take the interval [t_0, t_1] as an example. The calculation of the maximal available inductor current increment begins at instant t_0 and ends at instant t_1. Thus,

$$\Delta I_{Lm} = S_0 / L, \tag{1}$$

where $S_0 = \int_{t_0}^{t_1} (v_{j-1} - v_{dc})\mathrm{d}t$.

Upon completion of the first calculation, the second calculation begins. The second calculation is about the available inductor current increment $\Delta i_L(t)$. The available inductor current increment $\Delta i_L(t)$ at any instant within the interval [t_1, t_3] can be determined by the second calculation. Thus, $\Delta i_L(t)$ is determined by the voltage-time area S_2 in Fig. 5:

$$\Delta i_L(t) = S_2 / L, \tag{2}$$

where $S_2 = \int_{t}^{t_3} (v_j - v_{dc})\mathrm{d}t,\ t_1 \le t \le t_3$.

Rather than directly calculating $\Delta i_L(t)$ based on Eq. (2), it is more convenient to calculate it by subtracting S_2 from S_0, as the voltage vectors are assumed to be symmetric.

$$S_2 = S_0 - S_1. \tag{3}$$

Then,

$$\Delta i_L(t) = \Delta I_{Lm} - \frac{1}{L}\int_{t_1}^{t} (v_j - v_{dc})\mathrm{d}t,\quad t_1 \le t \le t_3. \tag{4}$$

Therefore, the available inductor current increment at instant t_2 is given by

$$\Delta i_L(t_2) = \Delta I_{Lm} - \frac{1}{L}\int_{t_1}^{t_2} (v_j - v_{dc})\mathrm{d}t. \tag{5}$$

If the appropriate thyristors are fired at instant t_2, the inductor current will achieve its maximal value at instant t_3 during the conduction of thyristors. The maximal value is equal to the sum of the instantaneous load current $i_L(t_2)$ and the predicted current increment $\Delta i_L(t_2)$. Therefore, for the predictive peak current control, the maximal value of the inductor current should equal the current reference $i_L^*(t_3)$.

$$i_L^*(t_3) = i_L(t_2) + \Delta i_L(t_2). \tag{6}$$

Note that the load voltage is assumed to vary slowly during the calculation of the voltage-time area; otherwise, the control scheme may be ineffective. For this reason, generator-type loads such as battery, DC motors, and inverters are preferable to be fed by the 18-pulse FTTR with the proposed predictive current control (Nedeljković and Stojiljković, 2003).

To achieve the average current control, an approximate transformation of the inductor current between the peak value and the corresponding

average value was adopted in Srdic and Nedeljković (2011). As illustrated in Fig. 6, the current i'_{L} is obtained by subtracting the minimal value of the inductor current i_{Lmin} from the inductor current i_{L}. The average value of the current i'_{L} is then approximated as

$$i'_{\mathrm{Lavg}} \approx 2\Delta I / \pi. \tag{7}$$

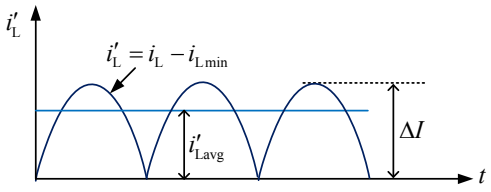

Fig. 6 Control of the average value of the inductor current (Srdic and Nedeljković, 2011)

On the other hand, the average current i'_{Lavg} should equal the current reference $i^*_{\mathrm{L}}(t)$ by subtracting the minimal value of the inductor current i_{Lmin}:

$$i'_{\mathrm{Lavg}} = i^*_{\mathrm{L}}(t) - i_{\mathrm{Lmin}}. \tag{8}$$

Thus, for the predictive average current control, the appropriate thyristors should be fired at the instant when the following equation is satisfied:

$$i^*_{\mathrm{L}}(t) = i_{\mathrm{L}}(t) + \frac{2}{\pi}\Delta I. \tag{9}$$

Consequently, Eq. (6) can be modified to be

$$i^*_{\mathrm{L}}(t_3) = i_{\mathrm{L}}(t_2) + \frac{2}{\pi}\Delta i_{\mathrm{L}}(t_2). \tag{10}$$

The approximation used in Srdic and Nedeljković (2011) is based on the assumption that i'_{L} is sinusoidal. In fact, i'_{L} is non-sinusoidal; thus, the approximation used in Srdic and Nedeljković (2011) causes the steady-state error between the current reference and the actual inductor current. To obtain the average value of i'_{L} with less error, this paper attempts to find the relationship between the peak value and the average value from another perspective. As shown in Fig. 7, i'_{L} starts to rise at instant t_2 and achieves its maximal value at instant t_3, and then begins to decrease until it achieves its minimal value at instant t_4.

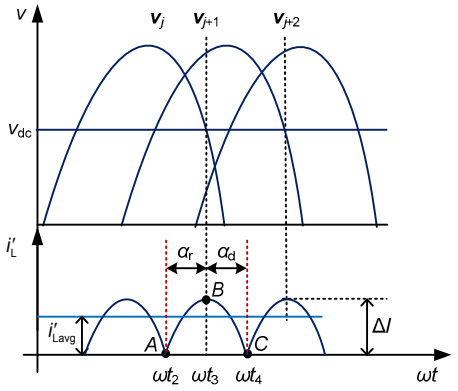

Fig. 7 Illustration of the average current control

As can be seen from Fig. 7, i'_{L} (in one pulse) is composed of two curve segments:

$$\begin{cases} \text{Curve } AB: i'_{\mathrm{L}}(t) = \dfrac{1}{L}\displaystyle\int_{t_2}^{t}(v_j - v_{\mathrm{dc}})\mathrm{d}t, \quad t_2 \le t \le t_3, \\ \text{Curve } BC: i'_{\mathrm{L}}(t) = \Delta I + \dfrac{1}{L}\displaystyle\int_{t_3}^{t}(v_j - v_{\mathrm{dc}})\mathrm{d}t, \quad t_3 \le t \le t_4, \end{cases} \tag{11}$$

where ΔI is the maximal value of i'_{L} and is given by

$$\begin{cases} \Delta I = i'_{\mathrm{L}}(t_3), \\ v_j = \sqrt{2}U_{\mathrm{r}}\sin(\omega t). \end{cases} \tag{12}$$

Based on Eqs. (11) and (12), the average current of i'_{L} is obtained. The relationship between i'_{Lavg} and ΔI is shown in Fig. 8. From Fig. 8, the approximate value of i'_{Lavg} is obtained:

$$i'_{\mathrm{Lavg}} \approx 2\Delta I / 3. \tag{13}$$

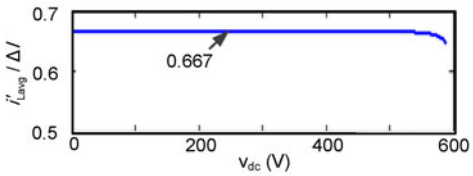

Fig. 8 Relationship between i'_{Lavg} and ΔI

The error comparisons between the approximate values of i'_{Lavg} and the actual average current value are shown in Fig. 9. As can be seen, the approximate value introduced in this paper is closer to the actual value than that introduced in Srdic and Nedeljković

(2011), and the error is practically negligible. Therefore, the modified condition for the predictive average current control is obtained:

$$i_{\mathrm{L}}^{*}=i_{\mathrm{L}}(t)+\frac{2}{3}\Delta i_{\mathrm{L}}(t). \tag{14}$$

If the particular thyristors are fired at which Eq. (14) is satisfied, the average value of each current pulse will equal the current reference i'_{Lavg} (Fig. 6), and thus the average current control is achieved.

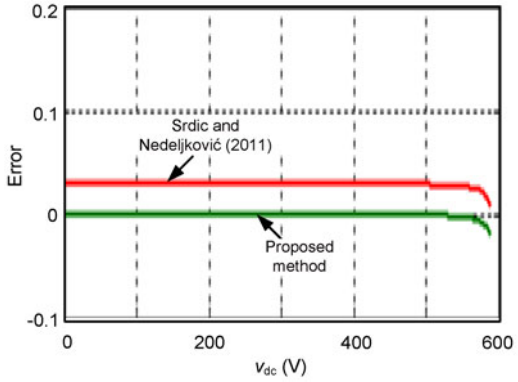

Fig. 9 Error comparisons between the approximate values and the actual value of i'_{Lavg}

Based on the proposed control strategy, the parallel and series operations of the 18-pulse FTTR can be accomplished effortlessly in Section 2.2.

2.2 Parallel and series operations

This section describes the parallel and series operations of the 18-pulse FTTR with the aforementioned control strategy. To apply the predictive current control to the 18-pulse FTTR, the voltage imposed on the DC-side inductor at every instant should be determined. Suppose that the three-phase voltage source from the AC mains is symmetric, i.e.,

$$\begin{cases} v_{AB}=\sqrt{2}U_{\mathrm{r}}\sin(\omega t), \\ v_{BC}=\sqrt{2}U_{\mathrm{r}}\sin(\omega t-2\pi/3), \\ v_{CA}=\sqrt{2}U_{\mathrm{r}}\sin(\omega t+2\pi/3). \end{cases} \tag{15}$$

Accordingly, a complete period (20 ms) is divided into 18 sections in both modes, corresponding to 18 voltage vectors. The values of the voltage vectors are determined based on the line-to-line voltages of the secondary windings of the phase-shifted transformer. The 18 voltage vectors are then applied to the DC-side inductor in sequence to calculate the available inductor current increment. The conducting sequence of the voltage vectors is shown in Fig. 10. For the parallel mode operation, the value of the voltage vectors can be found:

$$v_j=\sqrt{2}U_{\mathrm{r}}\sin\left(\omega t+\frac{(j-2)\pi}{9}\right),\ j=1,2,\cdots,18. \tag{16a}$$

For the series mode operation, the voltage vector $\boldsymbol{v}_{js}$ is obtained by calculating the vector sum of the three adjacent voltage vectors ($\boldsymbol{v}_{j-1}$, $\boldsymbol{v}_{j+1}$) which are defined in the parallel mode. Hence,

$$\begin{aligned}\boldsymbol{v}_{js}&=\boldsymbol{v}_{j-1}+\boldsymbol{v}_{j}+\boldsymbol{v}_{j+1}\\&=\sqrt{2}U_{\mathrm{s}}\sin\left(\omega t+\frac{(j-2)\pi}{9}\right),\ j=1,2,\cdots,18,\end{aligned} \tag{16b}$$

where $U_{\mathrm{s}}=[2\cos(\pi/9)+1]U_{\mathrm{r}}$. Note that $\boldsymbol{v}_0$ should be replaced by $\boldsymbol{v}_{18}$ when calculating the value of $\boldsymbol{v}_{1s}$ based on Eq. (16b). The voltage vectors are transmitted to the predictive controller successively to calculate the current increment, then determining which thyristors should be fired. As can be seen from Eq. (16), values of the voltage vectors in the parallel mode are smaller than those in the series mode, which means that the input voltages are higher in the series mode. Hence, poor current THD will be obtained

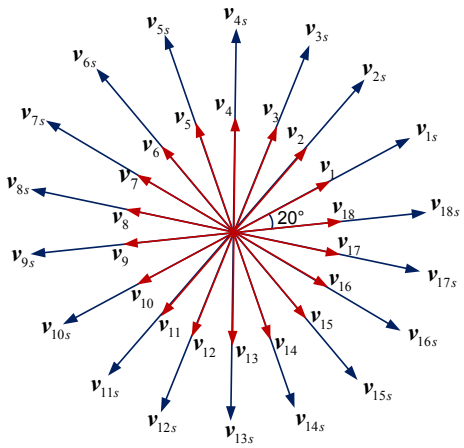

Fig. 10 Voltage vectors defined in the parallel and series modes

Short and long arrows refer to the vectors in the parallel mode operation and the series mode operation, respectively

when the 18-pulse FTTR operates in the series mode for low output voltage. To reduce the input current THD, the operating mode should be selected. In other words, the flexible-topology mechanism of the 18-pulse FTTR should be designed.

2.3 Flexible-topology mechanism of the 18-pulse FTTR

In this section, from the viewpoint of mitigating the input current THD, the topology-switching mechanism is discussed in detail. According to the previous analysis, the load voltage is adopted as the criterion for topology switching. When the load voltage is low enough to be fed by the 18-pulse parallel rectifier, the 18-pulse FTTR is suggested to operate in the parallel mode. In this case, the three 6-pulse rectifiers are connected in parallel to feed the load, and thus the delay angle of thyristors is reduced, as compared to that of the 18-pulse series rectifier feeding the same load. As soon as the load voltage fails to be fed by the 18-pulse parallel rectifier, the 18-pulse FTTR will switch to operate in the series mode. By this way, the three 6-pulse thyristor rectifiers are connected in series to boost the input voltage. Thus, the criterion for topology switching is summarized as follows:

$$\begin{cases} v_{\mathrm{dc}} > v_{\mathrm{h2}}, & \text{series mode,} \\ v_{\mathrm{dc}} < v_{\mathrm{h1}}, & \text{parallel mode,} \end{cases} \tag{17}$$

where v_{h1} and v_{h2} are the low and upper limits of the hysteresis, respectively. A hysteresis is used to make the topology-switching robust (Fig. 11).

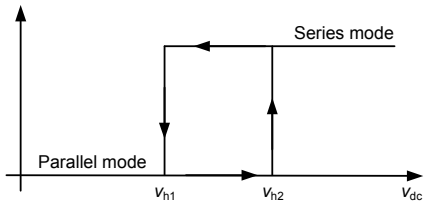

Fig. 11 Illustration of the topology-switching operation

The values of v_{h1}, v_{h2} can be determined by taking into account the available inductor current increment $\Delta i_{\mathrm{L}}(t)$, which characterizes the dynamic performance of the inductor current. As shown in Fig. 7, in the steady state, the performance of $\Delta i_{\mathrm{L}}(t)$ can be characterized by α_{r} and α_{d}, which are subjected to

$$\sin\left(\frac{\pi}{18}\right)\sin\left(\omega t_3 - \alpha_{\mathrm{r}} + \frac{\pi}{18}\right) = \frac{\pi}{18}\left(\frac{v_{\mathrm{dc}}}{\sqrt{2}U_{\mathrm{r}}}\right). \tag{18}$$

Based on Eq. (18), the dynamic performance of α_{r} with the output voltage v_{dc} is illustrated in Fig. 12. As shown in Fig. 12, α_{r} begins to decrease with increasing v_{dc} and experiences a sudden drop when v_{dc} exceeds $1.3U_{\mathrm{r}}$. This is because the voltage-time area is too small to produce the necessary Δi_{Lm} to afford $\Delta i_{\mathrm{L}}(t)$. Thus, to maintain a good dynamic performance, the output voltage of the 18-pulse FTTR should not exceed $1.3U_{\mathrm{r}}$. Accordingly, the certain condition for the 18-pulse FTTR working in the series mode is

$$v_{\mathrm{dc}} > 1.3U_{\mathrm{r}}, \tag{19}$$

and the condition for the 18-pulse FTTR working in the parallel mode is determined with a hysteresis:

$$v_{\mathrm{dc}} > 1.2U_{\mathrm{r}}. \tag{20}$$

Thus, the values of v_{h1} and v_{h2} are obtained:

$$\begin{cases} v_{\mathrm{h1}} = 1.2U_{\mathrm{r}}, \\ v_{\mathrm{h2}} = 1.3U_{\mathrm{r}}. \end{cases} \tag{21}$$

Note that if Eq. (20) is satisfied, the 18-pulse FTTR can operate in either the series or parallel mode, and can easily be switched from one mode to the other.

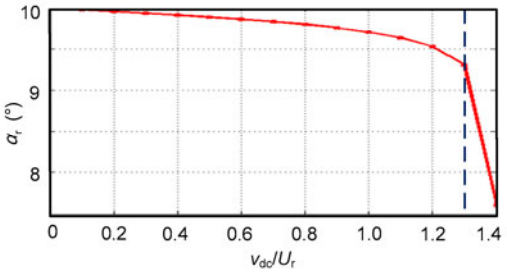

Fig. 12 Relationship between α_{r} and $v_{\mathrm{dc}}/U_{\mathrm{r}}$

Based on the proposed topology-switching mechanism, the input current THD as well as the power quality of the system can be improved. The predictive current control is then applied to the 18-pulse FTTR to obtain fast response, and the control algorithm is illustrated as flow diagrams in Section 2.4.

2.4 Predictive current control algorithm

The predictive current control algorithm is illustrated in Figs. 13 and 14 as flow diagrams. Fig. 13 shows the flexible-topology operation and Fig. 14 illustrates the predictive current control. The operating mode is selected before the implementation of the predictive current control. A FOR cycle is used to evaluate the inductor current with regards to every voltage vector, compare the current error, and store the minimal value as well as the corresponding index value of the voltage vector, and then the corresponding thyristors are fired. The control algorithm is implemented in the following way:

1. Every two adjacent voltage vectors are compared with output voltage for calculating the voltage-time areas.

2. The available inductor current increment with regards to every voltage vector is calculated.

3. The inductor current is predicted and compared with the current reference.

4. The minimal current error is stored and its index value of the related voltage vector is selected.

5. The corresponding thyristors are fired based on the selected voltage vector.

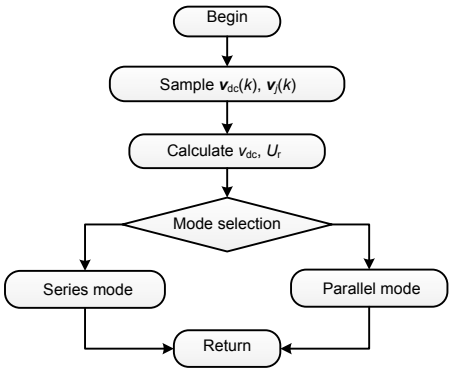

Fig. 13 Flow diagram of the implemented flexible-topology operation

Noted that Fig. 14 shows only the flow diagram of the parallel mode operation. It can be used to show the series mode operation by substituting $\boldsymbol{v}_{(j-1)s}(k)$, $\boldsymbol{v}_{js}(k)$ for $\boldsymbol{v}_{(j-1)}(k)$, $\boldsymbol{v}_j(k)$, respectively. For the sake of brevity, the flow diagram of the series mode is left out.

The control algorithm will be implemented on a digital signal processor (DSP), and six digital outputs of the DSP are used to transmit the firing signals for thyristors. If there is something wrong with any of the digital outputs, the 18-pulse FTTR will malfunction, leading to unexpected results. Even though the digital outputs function normally, any fault of the 18-pulse FTTR will lead to the system operating abnormally. Therefore, the fault tolerance evaluation is necessary.

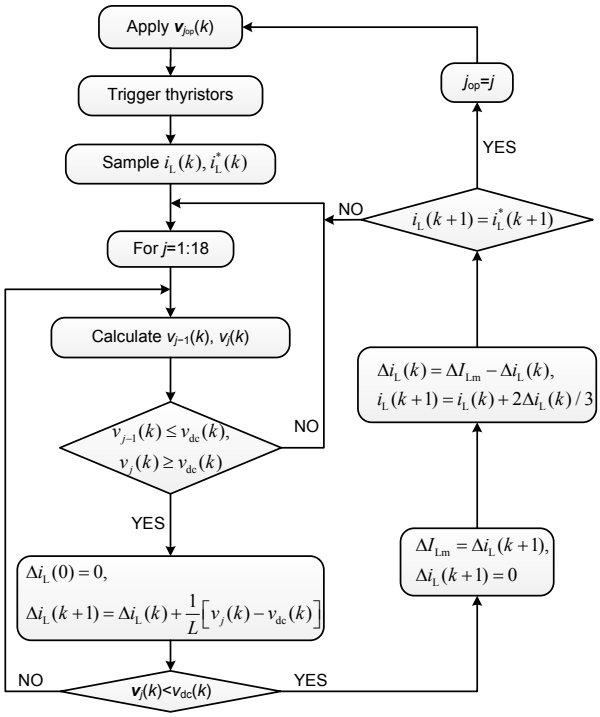

Fig. 14 Flow diagram of the control algorithm in the parallel mode operation

2.5 Fault tolerance evaluation

The 18-pulse FTTR has the fault-tolerant ability in case of rectifier failures. For example, if one of the 6-pulse rectifiers fails, the abnormal inductor current can be detected and the corresponding faulty rectifier is located. Then the main controller shuts down the faulty rectifier and the 18-pulse FTTR is reconfigured into a 12-pulse rectifier. After that, the predictive current controller is modified to control the 12-pulse rectifier, ensuring the current supply for the load. However, in this case, the input current THD as well as the load current ripple will be increased. Fig. 15 shows the simulation results of faulty operations of the 18-pulse FTTR in both operating modes. As a comparison, faulty operations with the PI control are also implemented. It is observed that the current ripple with PI control is larger than that with the

predictive current control. Moreover, the 18-pulse FTTR has the natural ability of short circuit since it is actually a current-source-type converter. This makes it easy to deal with different kinds of short-circuit failures.

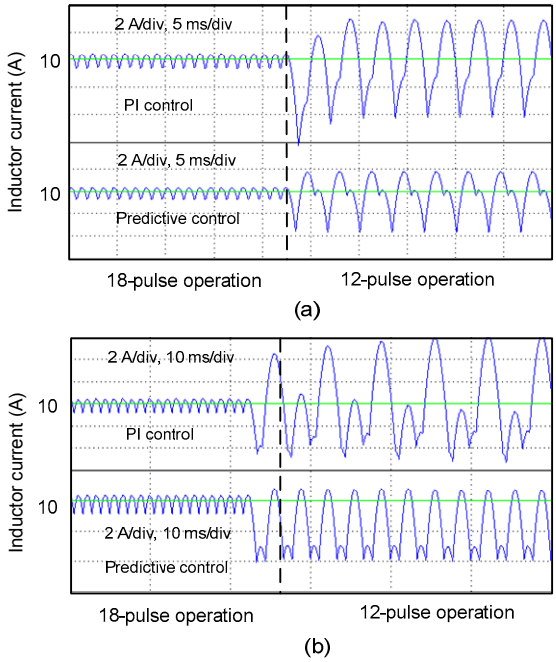

Fig. 15 Faulty operations of the 18-pulse FTTR
(a) Parallel mode operation; (b) Series mode operation

The short-circuit ability is verified when the 18-pulse FTTR operates in the parallel mode (Fig. 16). As can be seen from Fig. 16, when the short circuit occurs (simulated by stepping the output voltage from 20 to 0 V), the inductor current experiences a little overshoot with the PI control. However, it bears great overshoot with the predictive current control. This is because the predictive controller presented in this paper is sensitive to the output voltage variation.

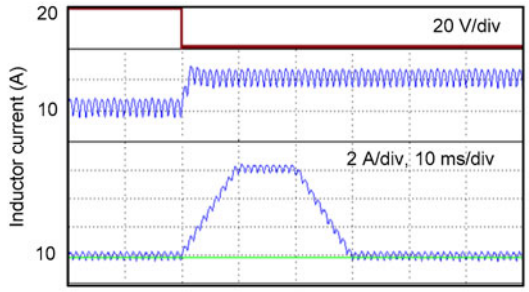

Fig. 16 Short-circuit ability test of the 18-pulse FTTR when operating in the parallel mode

It is also observed that a steady-state error exists in the inductor current when the 18-pulse FTTR is under faulty operation by the PI control. Thus, to eliminate the steady-state error of the inductor current, an adaptive PI controller is more appropriate.

3 Simulation and experimental results

3.1 Simulation results

Simulation of the 18-pulse FTTR controlled by the predictive current control has been carried out with Matlab/Simulink. The simulation results for a step change of the load current from 5 to 10 A and vice versa are shown in Fig. 17.

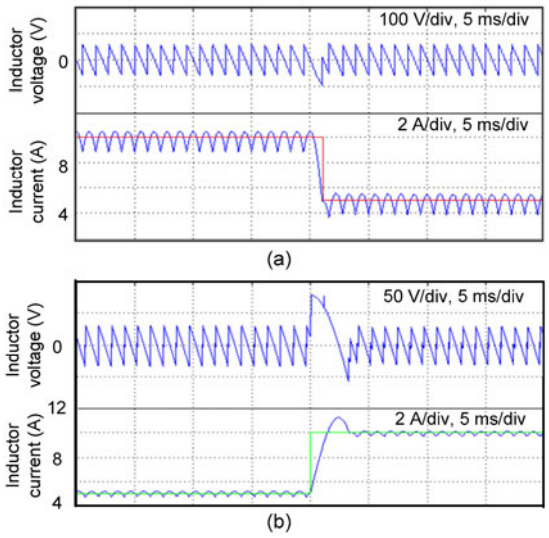

Fig. 17 Simulation results of the series mode (a) and the parallel mode (b) operations

It can be seen from the simulation results that fast transient response is achieved with negligible errors between the current reference and the actual load current. However, a little current overshoot occurs when the load current varies from 5 to 10 A, in both parallel and series operation. The flexible-topology operation is demonstrated in Fig. 18. It is shown that the 18-pulse FTTR can operate in either parallel or series mode by turning on/off the switches.

A performance comparison is carried out between the predictive current control and the conventional PI control (Fig. 19). As can be seen, the settle time of the load current by the predictive control is shorter than that by the PI control in both operating

modes (about 5.5 ms shorter in the parallel mode and 4.5 ms in the series mode). In addition, the performance comparisons of the flexible-topology operation are shown in Fig. 20. It is observed that switching from the series mode to the parallel mode and vice versa by the predictive current control is smooth, without apparent sag or swell in the load current.

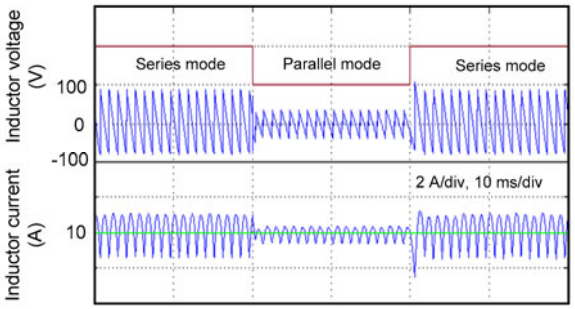

Fig. 18 Simulation results of the flexible-topology operation

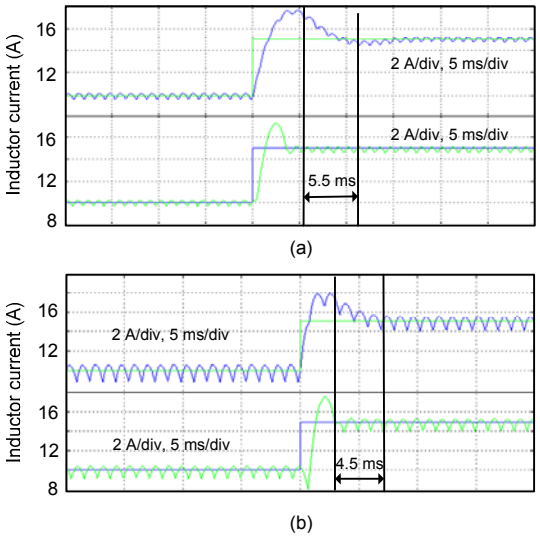

Fig. 19 Comparisons of the predictive controller (bottom) with the PI controller (top) in the parallel mode (a) and the series mode (b)

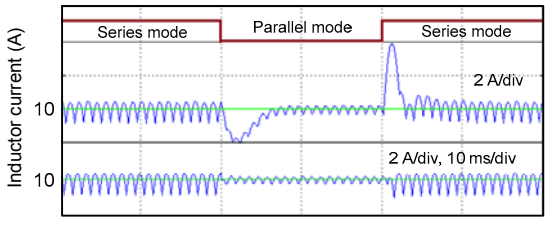

Fig. 20 Comparison between the PI controller (top) and the predictive controller (bottom)

3.2 Experimental results

Based on the simulation results, a laboratory prototype of the proposed 18-pulse FTTR is developed. A part of the prototype is shown in Fig. 21 where the bulky phase-shifted transformer and the generator-type load are excluded. The Chroma programmable AC/DC electronic load (Chroma 63804) is used as the generator-type load. The setup specifications are given in Table 1, and exceptional specifications with regards to some figures are appended to the figures' captions. The control algorithm is implemented on a Texas Instruments TMS320F2812 DSP. The inductor current, input and output voltages are sampled every 25 μs, and each signal is sampled four times to minimize the sampling error. New values of the inductor current, the input and output voltages are updated every 200 μs.

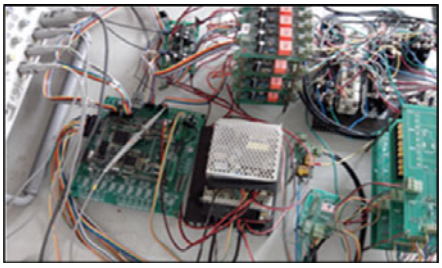

Fig. 21 Experimental setup of the 18-pulse FTTR

Table 1 Experimental setup specifications

Parameter	Value
Input line-to-line voltage, U_r (primary and secondary) (V)	120
Output voltage (load voltage), v_{dc} (V)	80
Transformer ratio (primary:secondary)	1:(1:1:1)
Phase-shift angle (primary:secondary)	0°:(−20°:0°:20°)
Inductance, L (mH)	20.3

The experimental results for a step change of the load current from 5 to 10 A and vice versa are shown in Figs. 22 and 23. Fast current response is achieved in both modes. The flexible-topology operation is verified by the experiment (Fig. 24). As can be seen, the flexible-topology operation is achieved fast and smoothly. The experimental results of the comparison between the predictive control and the PI control are shown in Figs. 25 and 26. These experimental comparisons further demonstrate that the predictive current control is superior to the PI control in coping with sudden current changes.

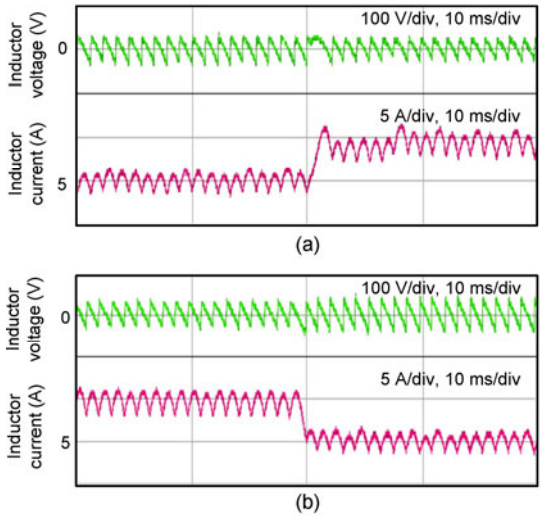

Fig. 22 Experimental results of the 18-pulse FTTR operating in the parallel mode

Current reference varies from 5 to 10 A (a) and from 10 to 5 A (b)

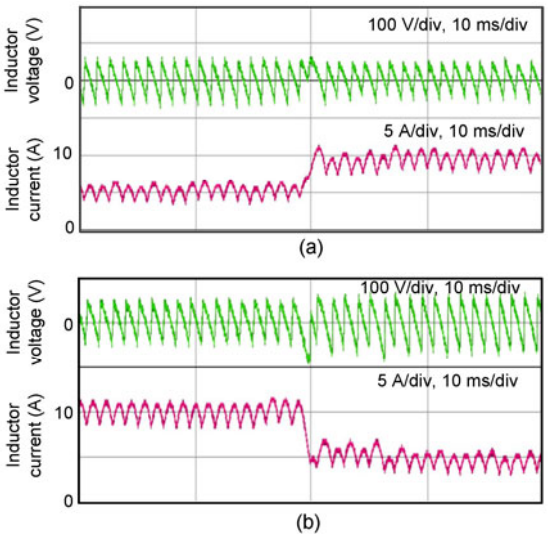

Fig. 23 Experimental results of the 18-pulse FTTR operating in the series mode

Current reference varies from 5 to 10 A (a) and from 10 to 5 A (b)

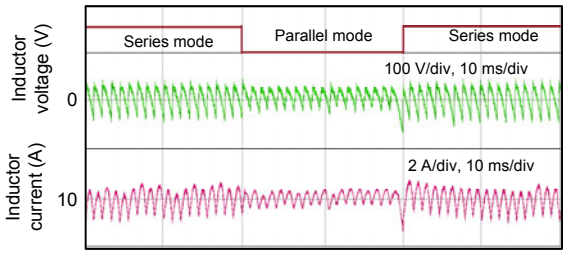

Fig. 24 Experimental result of the flexible-topology operation

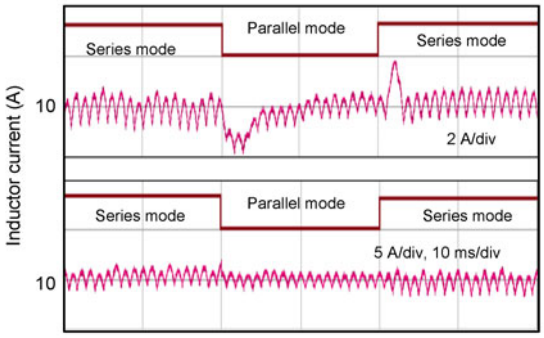

Fig. 25 Comparison between the PI controller (top) and the predictive controller (bottom)

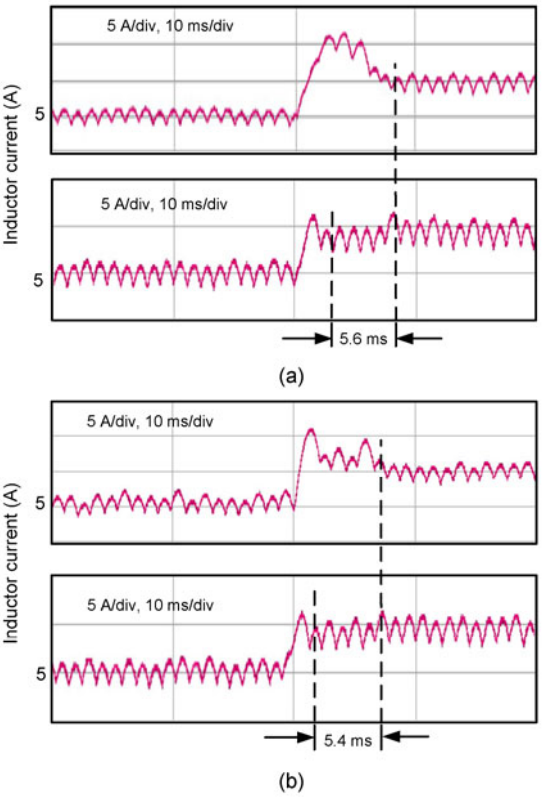

Fig. 26 Comparisons between the PI controller (top) and the predictive controller (bottom) in the parallel mode (a) and the series mode (b) operations

The analyses of the input current THD and the power factor of the system is shown in Figs. 27a and 27b, respectively. The input current waveforms for $v_{dc}/U_r>1$ are shown in Fig. 27c, which indicates that the 18-pulse FTTR can operate in the series mode as a step-up converter. It is observed that the input current THD is lower and the power factor of the system is higher in the parallel mode than that in the series mode when the output voltage is low, and thus the

18-pulse FTTR is capable of improving the input current THD as well as the power factor when feeding the light loads. It is also observed that the input current THD experiences a drastic variation when the output voltage is lower than 360 V. This is because the diodes D_2–D_4 are forced to conduct when the output voltage is low. They bypass part of the load current and thereby deteriorate the input current (Fig. 28). The input current THD comparison between the conventional 18-pulse series rectifier and the 18-pulse FTTR in the series mode is illustrated in Fig. 29. It is shown that the current THD of the 18-pulse FTTR begins to deteriorate when the output voltage is lower than some critical value. Therefore, from the standpoint of improving the current THD, it is suggested that the 18-pulse FTTR operate in the series mode when the output voltage satisfies

$$v_{dc} > 1.75U_r. \quad (22)$$

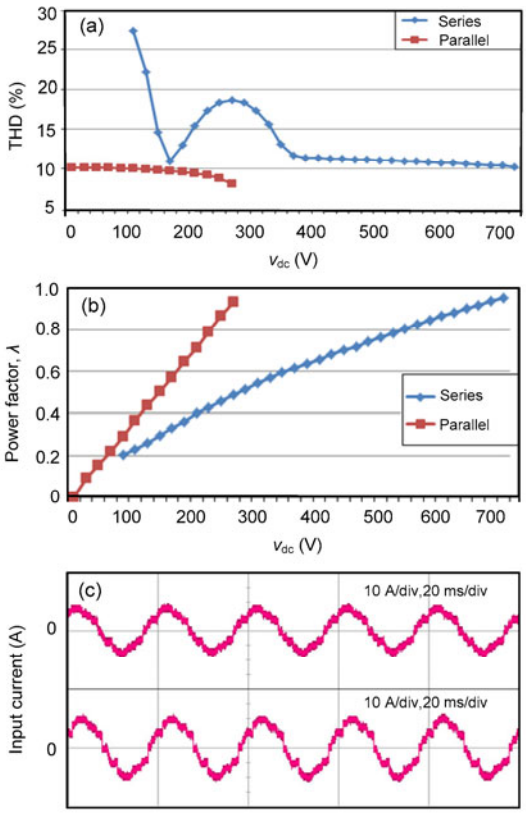

Fig. 27 Analyses of the input current THD and the power factor of the system

(a) Input current THD analysis; (b) Power factor analysis of the 18-pulse FTTR; (c) Input current waveforms for cases with $v_{dc}/U_r>1$ (top: U_r=120 V, v_{dc}=180 V; bottom: U_r=120 V, v_{dc}=140 V)

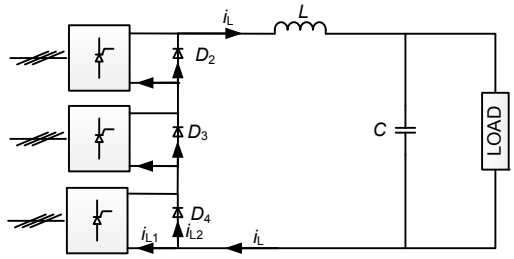

Fig. 28 Flow directions of the load current in the series mode

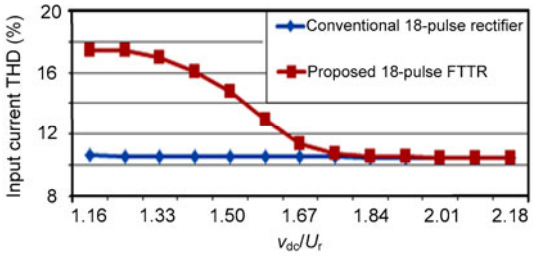

Fig. 29 Comparison of the input current THD

Note that the 18-pulse FTTR can also operate in the series mode even if Eq. (22) does not hold. Thus, Eq. (22) does not contradict Eq. (19) since Eq. (19) is obtained based on the consideration of the dynamic performance of the inductor current, while Eq. (22) is based on the consideration of improving the current THD.

Though the input current THD of the 18-pulse rectifier has been reduced observably as compared to that of the 12- or 6-pulse rectifier, some of the harmonic components are still beyond the limits suggested by IEEE Std. 519-1992 (Table 2). As can be seen from Tables 2 and 3, the low-order harmonic currents (n<17) are far less than the limits while the high-order harmonict currents (n≥17) exceed the limits. Therefore, to meet IEEE Std. 519-1992, additional harmonic mitigation methods (active or passive) should be used in the 18-pulse rectifier. A great amount of work has addressed on this topic (Choi *et al*., 2000; Arrillaga *et al*., 2006; Peterson and Singh, 2007; Fukuda and Ueda, 2010); hence, it is not the focus of this paper.

The input current and voltage waveforms in the worst case of distortion are shown in Fig. 30a; the corresponding current frequency spectrums are displayed in Fig. 30b. The worst case of distortion occurs in the series mode when the output voltage is far less than the input voltage. The figure also shows that

Table 2 Current distortion limits given by IEEE Std. 519-1992

Harmonic order, n	Current distortion limit
<11	≤4%
<17	≤2%
<23	≤1.5%
<35	≤0.6%
≥35	≤0.3%
THD	≤5%

Table 3 Harmonic components

I_{ref} (A)	THD (%)	I_{an}/I_{a1} (%)						
		n=5	n=7	n=9	n=17	n=19	n=35	n=37
10	10.08	0.06	0.07	0.02	7.19	4.39	3.12	2.60
50	6.43	0.23	0.23	0.01	4.87	3.94	0.93	0.78

n: harmonic order; I_{an}: root-mean-square (rms) value of the nth-order harmonic current; I_{a1}: rms value of the fundamental frequency current. The current THD is measured under U_r=200 V, v_{dc}=0 V

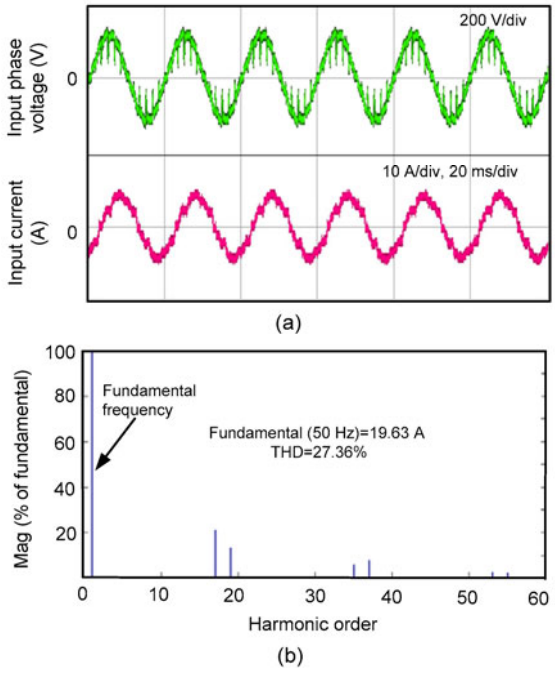

Fig. 30 Input current waveforms and the corresponding frequency spectrum analysis

(a) Input current and voltage (line-to-line value) waveforms in the worst case of distortion (top: input voltage; bottom: input current); (b) Spectrums of the input current

low-order harmonics (n<17) are trivial, and the harmonics are given by

$$n=18K\pm1,\ K=1, 2, \ldots. \quad (23)$$

The efficiency evaluation has been implemented on the experimental setup. It does not take into account the losses of the phase-shifted transformer; thus, the main losses are the conduction losses of the thyristors. The experimental results of the system efficiency in parallel mode are shown in Fig. 31, and the power consumed by the load is listed in Table 4. The results show that as the load voltage increases, the system efficiency increases. This is because when the load voltage increases, the delay angle of the thyristor is reduced and thus the active power increases.

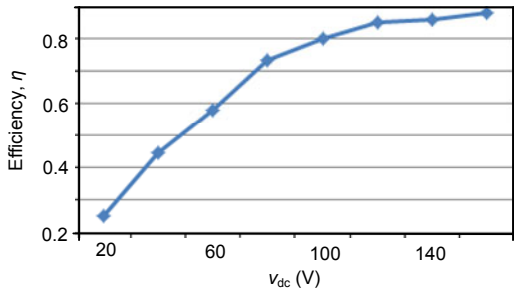

Fig. 31 Experimental results of the system efficiency in the parallel mode

Table 4 Power consumed by the load

v_{dc} (V)	P_{load} (kW)	v_{dc} (V)	P_{load} (kW)
20	0.34	100	1.05
40	0.58	120	1.10
60	0.76	140	1.12
80	0.96	160	1.16

4 Conclusions

This paper proposes a novel multi-pulse FTTR that can operate over a large voltage range while still keeping low current THD. To achieve this aim, the flexible-topology mechanism which determines the operating mode of the multi-pulse FTTR is proposed. Irrespective of the mode in which it operates, the load current maintains the same pulses. Unlike the conventional multi-pulse AC-DC converter that uses the PI controller, this paper proposes the predictive current controller to control the load current. The transient response of both modes and the transitions between parallel mode and series mode are confirmed to be fast and smooth by the performance analyses. Simulation and experimental results show the feasibility of the 18-pulse FTTR and the control method.

Owing to its capability to operate over a large voltage range, the proposed multi-pulse FTTR could be particularly useful in wind generation, to substitute for high-cost pulse-width modulation (PWM) rectifiers in high-power applications. Additionally, because of its better performance under sudden current variation, the proposed multi-pulse FTTR can be applied to aluminium potlines and electrowinning industry.

References

Ahmed, S.K.M., Iqbal, A., Abu-Rub, H., Cortes, P., 2011. Model Predictive Control of a Three-to-Five Phase Matrix Converter. Workshop on Predictive Control of Electrical Drives and Power Electronics, p.36-39. [doi:10.1109/PRECEDE.2011.6078685]

Arrillaga, J., Liu, Y.H., Perera, L.B., Watson, N.R., 2006. A current reinjection scheme that adds self-commutation and pulse multiplication to the thyristor converter. *IEEE Trans. Power Del.*, **21**(3):1593-1599. [doi:10.1109/TPWRD.2005.861324]

Arvindan, A.N., Guha, A., 2011. Novel Topologies of 24-Pulse Rectifier with Conventional Transformers for Phase Shifting. 1st Int. Conf. on Electrical Energy Systems, p.108-114. [doi:10.1109/ICEES.2011.5725312]

Bao, Z., Wu, G., Yan, W., 2011. Control of cascading failures in coupled map lattices based on adaptive predictive pinning control. *J. Zhejiang Univ.-Sci. C (Comput. & Electron.)*, **12**(10):828-835. [doi:10.1631/jzus.C1000369]

Choi, S.W., Oh, J., Cho, J., 2000. Multi-pulse Converters for High Voltage and High Power Applications. Proc. 3rd Int. Power Electronics and Motion Control Conf., p.1019-1024. [doi:10.1109/IPEMC.2000.882963]

Choi, S.W., Won, C., Kim, Y.S., Kim, C.K., 2003. High-pulse conversion techniques for HVDC transmission systems. *IEE Proc.-Gener. Transm. Distr.*, **150**(3):283-290. [doi:10.1049/ip-gtd:20030309]

Fukuda, S., Ueda, S., 2010. Auxiliary Supply Assisted Harmonic Suppression for 12-Pulse Phase-Controlled Rectifiers. Int. Conf. on Power Electronics, p.2310-2317. [doi:10.1109/IPEC.2010.5543685]

Fukuda, S., Ohta, M., Iwaji, Y., 2008. An auxiliary-supply-assisted harmonic reduction scheme for 12-pulse diode rectifiers. *IEEE Trans. Power Electron.*, **23**(3):1270-1277. [doi:10.1109/TPEL.2008.921165]

Garg, V., Singh, B., Bhuvaneswari, G., 2009. 24-pulse AC-DC converter for harmonic mitigation. *IET Power Electron.*, **2**(4):364-374. [doi:10.1049/iet-pel.2008.0039]

Geyer, T., 2010. Model Predictive Direct Current Control for Multi-level Converters. IEEE Energy Conversion Congress and Expo., p.4305-4312. [doi:10.1109/ECCE.2010.5618476]

Hao, R.X., Zheng, T.Q., You, X.J., Guo, W.J., 2007. Development and Experiment Research of High-Power Arc Heater Power Supply Utilizing Thyristor Converter. 2nd IEEE Conf. on Industrial Electronics and Applications, p.1559-1563. [doi:10.1109/ICIEA.2007.4318670]

Kocman, S., Kolar, V., Vo, T.T., 2010. Eighteen-Pulse Rectifiers for Harmonic Mitigation. Proc. 14th Int. Conf. on Harmonics and Quality of Power, p.1-6. [doi:10.1109/ICHQP.2010.5625409]

Lim, C.S., Rahim, N.A., Hew, W.P., Levi, E., 2013. Model predictive control of a two-motor drive with five-leg inverter supply. *IEEE Trans. Ind. Electron.*, **60**(1):54-65. [doi:10.1109/TIE.2012.2186770]

Nedeljković, M., Stojiljković, Z., 2003. Fast current control for thyristor rectifiers. *IEE Proc.-Electr. Power Appl.*, **150**(6):636-638. [doi:10.1049/ip-epa:20030910]

Peterson, M., Singh, B.N., 2006. Modeling and Analysis of Multipulse Uncontrolled/Controlled AC-DC Converters. IEEE Int. Symp. on Industrial Electronics, **2**:1400-1407. [doi:10.1109/ISIE.2006.295677]

Peterson, M., Singh, B.N., 2007. Multipulse AC-DC Thyristor Converter with DC Bus Current Shaper. IEEE Power Engineering Society General Meeting, p.1-8. [doi:10.1109/PES.2007.385730]

Peterson, M., Singh, B.N., 2009. Multipulse controlled AC-DC converters for harmonic mitigation and reactive power management. *IET Power Electron.*, **2**(4):443-455. [doi:10.1049/iet-pel.2007.0199]

Rezazadeh, A., Sedighizadeh, M., Hasaninia, A., 2010. Coordination of PSS and TCSC controller using modified particle swarm optimization algorithm to improve power system dynamic performance. *J. Zhejiang Univ.-Sci. C (Comput. & Electron.)*, **11**(8):645-653. [doi:10.1631/jzus.C0910551]

Rodríguez, J.R., Pontt, J., Silva, C., Wiechmann, E.P., Hammond, P.W., Santucci, F.W., Alvarez, R., Musalem, R., Kouro, S., Lezana, P., 2005. Large current rectifiers: state of the art and future trends. *IEEE Trans. Ind. Electron.*, **52**(3):738-746. [doi:10.1109/TIE.2005.843949]

Rodríguez, J.R., Pontt, J.O., Silva, C.A., Correa, P., Lezana, P., Cortés, P., Ammann, U., 2007. Predictive current control of a voltage source inverter. *IEEE Trans. Ind. Electron.*, **54**(1):495-503. [doi:10.1109/TIE.2006.888802]

Saied, B.M., Zynal, H.I., 2007. Harmonic Current Reduction of a Six-Pulse Thyristor Converter. Int. Aegean Conf. on Electrical Machines and Power Electronics, p.596-602. [doi:10.1109/ACEMP.2007.4510575]

Schroder, D., 2009. Predictive Control Strategies for Converter and Inverter. IEEE Int. Conf. on Industrial Technology, p.1-8. [doi:10.1109/ICIT.2009.4939723]

Singh, B.P., Gairola, S., 2007. Pulse Doubling in 18-Pulse AC-DC Converters. 7th Int. Conf. on Power Electronics and Drive Systems, p.533-539. [doi:10.1109/PEDS.2007.4487752]

Srdic, S., Nedeljković, M., 2011. Predictive fast DSP-based current controller for thyristor converters. *IEEE Trans. Ind. Electron.*, **58**(8):3349-3358. [doi:10.1109/TIE.2010.2089941]

Tanaka, T., Nakazato, M., Funabiki, S., 2001. A New Approach to the Capacitor-Commutated Converter for

HVDC—a Combined Commutation-Capacitor of Active and Passive Capacitors. Power Engineering Society Winter Meeting, p.968-973. [doi:10.1109/PESW.2001.917004]

Wiechmann, E.P., Burgos, R.P., Holtz, J., 2000. Sequential connection and phase control of a high-current rectifier optimized for copper electrowinning applications. *IEEE Trans. Ind. Electron.*, **47**(4):734-743. [doi:10.1109/41.857953]

Wiechmann, E.P., Aqueveque, P., Morales, A.S., Acuna, P.F., Burgos, R., 2008. Multicell high-current rectifier. *IEEE Trans. Ind. Appl.*, **44**(1):238-246. [doi:10.1109/TIA.2007.912728]

Yang, C., Zhu, S., Kong, W., Lu, L., 2006. Application of generalized predictive control in networked control system. *J. Zhejiang Univ.-Sci. A*, **7**(2):225-233. [doi:10.1631/jzus.2006.A0225]

Yaramasu, V., Wu, B., Rivera, M.E., Rodríguez, J.R., Wilson, A., 2012. Cost-Function Based Predictive Voltage Control of Two-Level Four-Leg Inverters Using Two Step Prediction Horizon for Standalone Power Systems. 27th Annual IEEE Applied Power Electronics Conf. and Expo., p.128-135. [doi:10.1109/APEC.2012.6165808]

Young, C.M., Chen, M.H., Lai, C.H., Shih, D.C., 2012. A novel active interphase transformer scheme to achieve three-phase line current balance for 24-pulse converter. *IEEE Trans. Power Electron.*, **27**(4):1719-1731. [doi:10.1109/TPEL.2011.2169684]

Zargari, N.R., Yuan, X., Bin, W., 1997. A multilevel thyristor rectifier with improved power factor. *IEEE Trans. Ind. Appl.*, **33**(5):1208-1213. [doi:10.1109/28.633798]