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Algorithm and evaluation of generating pseudo datasets for integrated circuits power analysis

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Abstract: Average power analysis plays a crucial role in the design of large-scale digital integrated circuits (ICs). The integration of data-driven machine learning (ML) methods into the electronic design automation (EDA) fields has increased the demand for extensive datasets. To address this need, we propose a novel pseudo-circuit generation algorithm rooted in graph topology. This algorithm efficiently produces a multitude of power analysis examples by converting randomly generated directed acyclic graphs (DAGs) into gate-level Verilog pseudo-combinational circuit netlists. The subsequent introduction of register units transforms pseudo-combinational netlists into pseudo-sequential circuit netlists. Hyperparameters facilitate the control of circuit topology, while appropriate sequential constraints are applied during synthesis to yield a pseudo-circuit dataset. We evaluated our approach using mainstream power analysis software, conducting pre-layout average power tests on the generated circuits, comparing their performance against benchmark datasets, and verifying through circuit topology complexity analysis and static timing analysis (STA). The results confirm the effectiveness of the dataset and demonstrate the operational efficiency and robustness of the algorithm, underscoring its research value.

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1 Introduction

Power analysis plays a pivotal role in the design of large-scale digital integrated circuits (ICs), where accurate and efficient power evaluation during the design phase can substantially improve chip performance. In the industry, power analysis typically refers to average power estimation facilitated by electronic design automation (EDA) software. Notable examples of commercial software for this purpose include Synopsys PrimeTime PX (PTPX) and Cadence Voltus. Typically, average power analysis is performed at the gate level, where power is calculated based on circuit activity.

Circuit activity can be categorized into annotated and vectorless types. The annotated approach utilizes simulators like Synopsys VCS with predefined test vectors to monitor activity at each circuit node, typically recorded in switching activity interchange Format (SAIF) files. Although the simulation-based annotated method offers high accuracy, it is time-consuming and demands significant storage space. Consequently, the industry often employs a vectorless method in the pre-simulation phase, which uses a mathematical model to estimate the activity probability at each node and then compute power consumption.

The concept of probability-based power estimation was first introduced by (Najm, 1993) and has since spurred extensive research within the academic community on such theoretical models (Burch et al., 1992; Xie, 2023). These models are used solely for

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algorithm validation and do not require large sample sizes. However, as circuit complexity escalates, traditional algorithms struggle with efficiency and accuracy, particularly in large-scale combinational and sequential circuits. This challenge has led to a growing interest in data-driven machine learning (ML) approaches. Several researchers have explored innovative methods; for instance, (Zhou et al., 2019) introduced PRIMAL, utilizing convolutional networks for power estimation, while (Kumar and Gerstlauer, 2019) adopted a decision tree approach. Others, like (Zhang et al., 2020), (Khan et al., 2024), and (Rakesh et al., 2023), have employed graph neural networks to represent circuit topology for power prediction, while some researchers like (Li et al., 2022), (Fang et al., 2023),and (Kumar et al., 2023) have utilized traditional neural networks. In addition to the mentioned power prediction, there are also circuit power optimization methods, such as the ML-based circuit power optimization proposed by (Zou et al., 2024) and others.

Despite the advancements in power analysis techniques, the requirement for extensive circuit data and diverse topological scenarios remains a significant challenge for model training (Nasser et al., 2021). Current standard datasets in the IC industry are often inadequate for ML applications, lacking in both quantity and specificity (Hansen et al., 1999; Brglez et al., 1989). Moreover, accessing large-scale industrial or competition data frequently entails navigating copyright and other legal constraints (Xie et al., 2023a,b), posing substantial barriers to data acquisition.

In response to the limitations of existing datasets and to support the needs of ML-driven average power analysis methods, we propose a novel pseudo-circuit dataset generation algorithm specifically tailored for power analysis, as depicted in Fig. 1. Our methodology leverages graph topology calculations to generate pseudo circuit datasets. Initially, a random DAG is created, followed by mapping directed acyclic graph (DAG) nodes to gate-level nodes to form a combinational circuit. By integrating register units, these combinational circuits are converted into sequential circuits, which are subsequently optimized using the Synopsys Design Compiler (DC) under defined constraints. The accuracy of circuit activity is verified through golden power analysis from Synopsys VCS simulation with random vectors. This approach allows for the generation of an unlimited number of dataset samples independently of open-source RTL code. In random vector tests on sequential circuits, we observed a signal non-flipping phenomenon due to loop impacts, which results in low average power consumption. The signal non-flipping phenomenon, termed the zero power issue, was further explored to understand the influence of sequential circuit topology on power consumption.

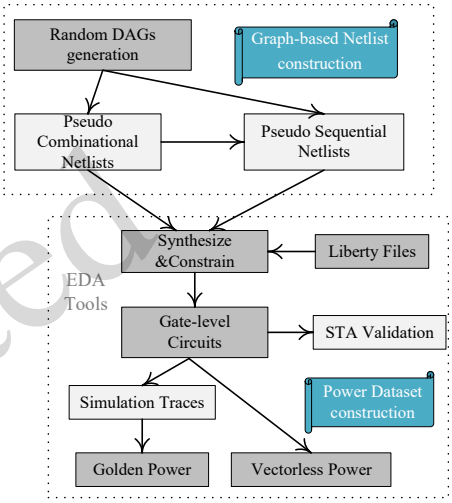

Fig. 1: Overview of the pseudo-circuit dataset generation process for pre-simulation power analysis

The work is structured as follows: an introduction and literature review in Sections 1 and 2, a detailed discussion on methods for generating pseudo-combinational and sequential circuit netlists in Sections 3 and 4, synthesis and analysis of pseudo-circuit netlists in Section 5, and a comprehensive summary in the final section.

2 Combinational circuit netlists and DAG topology

Combinational circuits are characterized by steady-state outputs that depend solely on the current input values and not on any previous states (Kaeslin, 2008).The output nodes as F_i for $i = 1, 2, \ldots, n$ and the input nodes as x_j for $j = 1, 2, 3, \ldots, m$, with the relationship $F_i = f(x_1, x_2, \ldots, x_m)$. Here, $f(\cdot)$ symbolizes the function encapsulated by the combinational logic circuit.

The architectural elements of the circuit—AND, OR, NOT gates, and other combinational logic units are abstracted as nodes $V = \{v_1, v_2, \ldots, v_M\}$.

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The connections between inputs, outputs, and these nodes are represented as directed edges $E = \{e_1, e_2, \ldots, e_N\}$. The circuit topology typically adheres to a DAG structure, where the set of nodes and edges, V and E, form the acyclic graph $G = (V, E)$. Given the inherent DAG-like properties of combinational circuits, it is feasible to initially construct a DAG and subsequently adapt it into a combinational circuit configuration.

2.1 Random DAG generation algorithm

In scenarios requiring specific numbers of inputs and outputs, traditional brute force methods for generating random DAGs are often suboptimal due to inefficiencies and performance limitations stemming from the random structures failing to meet circuit specifications. We propose an efficient and rapid algorithm for generating random DAG topologies that adhere to the following constraints:

1. m inputs, n outputs.
2. A topology consistent with a DAG and comprising a single connected component.

We define the sets of primary input nodes as $\mathcal{X}$, internal interconnection nodes as $\mathcal{W}$, and primary output nodes as $\mathcal{O}$. Here, $\mathcal{W}$ and $\mathcal{O}$ are collectively referred to as output nodes $\mathcal{O}'$. The initial state of the graph $\mathcal{G}$ includes only nodes without any connecting edges. We introduce the Random Multi-Connected Component DAG Generation method, detailed in Algorithm 1, which efficiently establishes initial connections within $\mathcal{G}$. This algorithm ensures that each component of $\mathcal{G}$ is a subgraph conforming to the structure of a DAG. γ represents the expected number of nodes, and is used to modulate the complexity of the resultant topology, with higher values indicating increased complexity.

During the random selection of input nodes, the size of set $\mathcal{X}$ is approximately m. However, the number of output nodes $\mathcal{O}$ can substantially deviate from n. This discrepancy arises as edges that do not adhere to the DAG structure are eliminated. This process may also lead to the formation of multiple connected components within the computational graph $\mathcal{G}_M$. To resolve these potential problems, we introduced Algorithm 2.

Algorithm 2 enhances the graph's structure by examining and connecting separate components, ensuring that the graph maintains weak connectivity and forms a single connected component. Post-processing with Algorithm 2 results in a computational graph $\mathcal{G}_S$ that comprises only one connected component. Together, Algorithms 1 and 2 guarantee that $\mathcal{G}_S$ adheres to the necessary topological specifications. Nonetheless, the count of primary output nodes ($\mathcal{O}_S$) in $\mathcal{G}_S$ may not align with the expectation. To mitigate this issue, we introduce Algorithm 3, which augments the topology on the existing $\mathcal{O}_S$, thus minimizing the difference in the number of primary input nodes.

Algorithm 3 segregates the output nodes into two categories: retained nodes, denoted as $\mathcal{O}_S^+$, and discarded nodes, denoted as $\mathcal{O}_S^-$. The algorithm subsequently appoints nodes from $\mathcal{O}_S^-$ as progenitors for the nodes in $\mathcal{O}_S^+$. This involves a stochastic selection of parent nodes from $\mathcal{O}_S^-$ for $\mathcal{O}_S^+$, which may not ensure a precise match to the desired number of output nodes, n. Consequently, multiple iterations may be required to mitigate the error within

Algorithm 1 Random Multi-Connected Component DAG Generation

Require: Graph G defined by nodes only, without edges.
Ensure: Multi-connected DAG graph $\mathcal{G}_M$.

$\mathcal{S} \leftarrow \mathcal{W} + \mathcal{X}$;
for all $o \in \mathcal{O}'$ **do**
  Randomly select γ nodes from $\mathcal{S}$ as parent nodes for o, forming the set $\mathcal{P}$;
  for all $p \in \mathcal{P}$ **do**
    add edge $\langle p, o \rangle$ to G;
    if G does not conform to DAG structure **then**
      Remove edge $\langle p, o \rangle$;
    end if
    Add p to $\mathcal{S}$;
  end for
end for

Algorithm 2 Single Connected Component Assurance

Require: $\mathcal{G}_M$ with multiple connected components.
Ensure: $\mathcal{G}_S$ with only one connected component.

$\mathcal{G}_S = \mathcal{G}_M$;
while $\mathcal{G}_S$ is not weakly connected **do**
  List all connected components of $\mathcal{G}_S$;
  Select different nodes from two different components;
  Connect these two nodes;
  Update $\mathcal{G}_S$;
end while

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Algorithm 3 Adjustment of Primary Outputs

Require: Single connected computation graph $\mathcal{G}_S$, expected output node number n.
Ensure: Computation graph $\mathcal{G}$ with adjusted output.

```
Let G = G_S;
while true do
    O_S ← G;
    O_S^+, O_S^- ← O_S;
    for all σ ∈ O_S^+ do
        Select nodes from O_S^- as parent P_S for σ
        for p ∈ P_S do
            Add edge ⟨p, σ⟩ to G;
        end for
    end for
    if number of outputs in G approximates n then
        Break loop;
    end if
end while
```

an acceptable threshold. Post processing with Algorithm 3, the resultant computation graph $\mathcal{G}$ forms a single-connected DAG, which is suitable for implementation in combinational circuits.

2.2 From DAG to combinational circuit netlist

Upon deriving the abstract topology represented by $\mathcal{G}$, we convert this computation graph into a pseudo-combinational circuit. The conversion follows these rules:

1. Nodes are initially categorized based on their indegree and outdegree into three distinct types: primary inputs, wires, and primary outputs. Nodes with an indegree of zero are primary inputs, those with an outdegree of zero are primary outputs, and all remaining nodes are wires.

2. For nodes categorized as wires, gate units are assigned variably based on the indegree size. Specifically, if the indegree is one, a gate unit is randomly assigned either as NOT or BUFF. If the indegree is one, the gate unit type is randomly selected from AND, NAND, OR, and NOR.

As shown in Fig. 2, the methodology for generating a pseudo-random combinational circuit netlist from a random DAG is delineated. The process begins with the generation of nodes based on the predefined number of primary input and output nodes. Using Algorithm 1, these nodes are interconnected to form a multi-connected DAG structure, denoted as $\mathcal{G}_M$. To integrate multiple connected components into a coherent structure, Algorithm 1 is again utilized, resulting in a unified DAG, $\mathcal{G}_S$. To avoid $\mathcal{G}_S$ failing to align with the primary output node count n, adjustments are made using Algorithm 3, thereby achieving a final computation graph $\mathcal{G}$ that satisfies the specified requirements. The graph node is then converted into gate units at random to convert graph into the desired random combinational circuit netlist.

3 Sequential circuits and DCG topology

Sequential circuits are defined as circuits whose steady-state output at any given time depends not only on the current input but also on the input from previous states (Kaeslin, 2008). Let the primary input nodes be denoted by $x_i, i = 1, 2, 3 \ldots m$, the output state equation by $f_j(\cdot), j = 1, 2, 3 \ldots n$, and primary output nodes by y_j. Additionally, define the drive excitation function as $g_r(\cdot), r = 1, 2, 3 \ldots k$, the drive excitation as z_r, the signal state function as $h_o(\cdot), o = 1, 2, 3 \ldots l$, and the signal state as q_o. The output logic for sequential circuits can thus be expressed through the following equations:

$$y_j = f_j\left(x_1, x_2, x_3, \ldots, x_m, q_1, q_2, \ldots q_l\right). \quad (1)$$

Drive excitation equation:

$$z_r = g_r\left(x_1, x_2, x_3, \ldots, x_m, q_1, q_2, \ldots q_l\right). \quad (2)$$

Signal state equation:

$$q_o^{t+1} = h_o\left(z_1, z_2, \ldots, z_k, q_1^t, q_2^t, \ldots, q_l^t\right), \quad (3)$$

where t denotes discrete time steps indexed by clock periods.

Sequential circuits, unlike combinational circuits, incorporate a state storage structure consisting of registers and combinational logic arranged in a loop. Our research focuses on sequential circuits that adhere to a directed cycle graph (DCG) structure. Directly generating a DCG structure into a practical circuit netlist can be challenging. We propose an efficient and swift method that leverages gate-level combinational circuits to generate a pseudo-sequential circuit netlist in compliance with a DCG structure.

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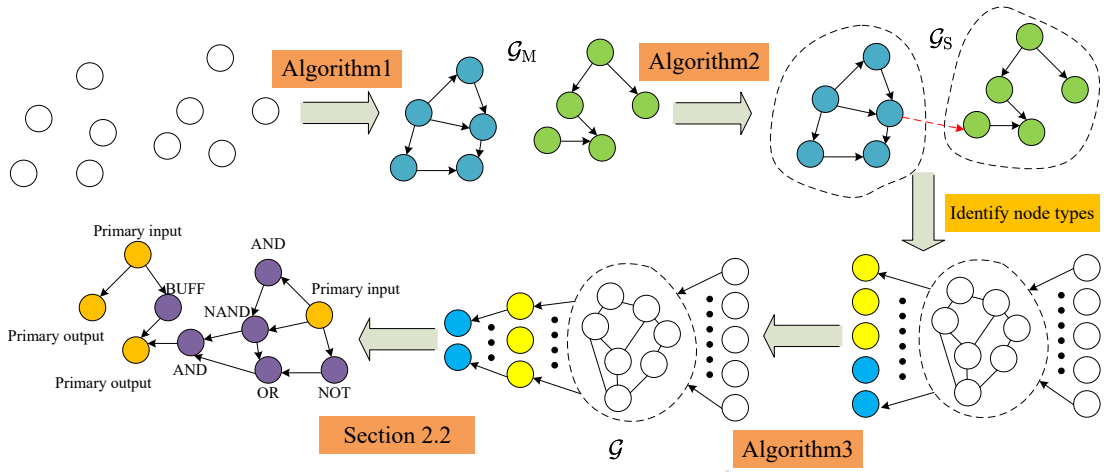

Fig. 2: Random combinational circuit netlist generation. Algorithm 1 processes the nodes into different connected components, Algorithm 2 transforms multiple connected components into a single connected component, and Algorithm 3 adjusts the number of identified output pins. Finally, the algorithm proposed in Section 2.2 converts the generated DAG topology into the combinational circuit netlist.

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The transformation from a combinational circuit netlist to a sequential circuit netlist can be facilitated by introducing registers. This method involves selecting a specific number of primary inputs and outputs from the existing gate-level combinational circuit and connecting them using predefined gate-level registers. This process effectively transforms the DAG combinational circuit into a DCG-structure pseudo-sequential circuit netlist. It is crucial that the descriptions of these gate-level registers align with the logic descriptions used in the DC synthesis phase.

The ratio of the number of selected IO ports to the number of DAG IO ports is defined as α, $\alpha = l/m$, which is called the sequential circuit generation factor, and the functional trend of the generated circuits can be changed by varying this factor. For example, a larger α implies that there are more registers in the circuit, which may correspond to the memory function chip, while a smaller α corresponds to the computation function chip.

4 Experimental results

4.1 Dataset generation flow and parameter setting

The proposed algorithm can generate pseudo-circuit Verilog netlists that contain gate-level unit descriptions. These netlists are random in function and do not have strict specific practical application scenarios or functional meanings. Pseudo-netlists are mainly used in the field of power analysis, and this section will start with the synthesis and power consumption testing of the generated pseudo-netlists.

For synthesis, we use the generated pseudo-gate-level netlist, applying it to the SMIC 40nm digital circuit process library. We employ various logic components, such as AND, NAND, OR, NOR, BUF, INV, and DFF. Appropriate timing constraints are set to facilitate the synthesis of the gate-level Verilog descriptions into a gate-level circuit netlist based on the industrial process library.

The randomly generated pseudo gate-level netlist may exhibit redundancies in logic functions or issues like logic constants stemming from nested circuit designs. It is essential to meticulously analyze the internal logic of circuits to eliminate any redundant functionality. The DC offers methods for checking and correcting the logic functions and timing of circuits. The synthesis process with DC aims not only to align the circuits with process libraries but also to optimize the circuit design and ensure the integrity of the generated pseudo-circuits.

Experimentally, the number of input/output nodes in combinational circuits is randomly selected between 50 and 400, with the number of wires varying from 500 and 5,000. For sequential circuits, the initial number of input/output nodes ranges from

Table 1: Overview of pseudo-power datasets

Type		Inputs	Outputs	Wires	Logical gates	
Combinational Circuit	Mean	49	58	3,311	3,370	
	Min	22	35	887	939	
	Max	79	83	5,638	5,715	
		Inputs	Outputs	Wires	Logical gates	Registers
Sequential Circuit	Mean	254	256	4,769	4,918	107
	Min	90	98	686	1,104	37
	Max	436	440	4,950	7,429	185

100 to 600, with wires also between 500 to 5,000. A parameter setting of $\gamma = 2$ is applied. The pseudo-combinational circuits' netlist for generating the DAG structure uses a conversion factor of $\alpha = 0.3$ to transition to a pseudo-sequential circuit. During the DC synthesis, the software would adjust the IO ports and wires based on timing constraints.

4.2 Pseudo-power datasets

As per the algorithm discussed earlier, $1k$ sets each of combinational and temporal circuit netlists are generated. Then DC is used to generate the pseudo-dataset, as depicted in Table 1.

The dataset comprises samples where the average number of logic gates in the combinational circuits is approximately $3.3k$, with a range from $0.9k$ to $5.7k$. The number of primary input/output nodes in these circuits varies from 20 to 80. In sequential circuits, the gate count ranges from $1.1k$ to $7.4k$, averaging about $4.9k$ gates. The number of primary I/O nodes ranges from 90 to 430. Notably, the generated netlists maintain consistency in the number of primary inputs and outputs, exhibiting a broad diversity in the number of output ports and internal gate-level units. Variations between the pseudo-circuit configurations and pseudo-topology parameters arise due to corrections and simplifications made during the synthesis, specifically in timing, power consumption, and functional adjustments.

4.3 Comparison with state-of-the-art dataset methods

ML methods rely on a large amount of sample data, but there is still a gap in public datasets dedicated to power consumption analysis for ML methods. Established datasets, such as ISCAS (Hansen et al., 1999), MCNC (Brglez et al., 1989), and EPFL (Amarú et al., 2015) offer limited samples and scenarios, which do not fully meet the demands of ML-based. Alternative datasets for circuit tasks often derive from specific open-source RTL codes, such as RISC-V designs (YosysHQ, 2021; OnchipUIS, 2021, 2016), CPU-Core designs (OpenCores Team, 2024), or other circuit codes (Zhou et al., 2018; Amid et al., 2020; Corno et al., 2000).

Table 2 presents a comparative overview of representative digital IC datasets for ML alongside the proposed dataset. Current dataset methodologies (Chai et al., 2022; Chowdhury et al., 2021; Wei et al., 2023; Gautier et al., 2016) rely on collating specific RTL codes, thereby expanding sample sizes compared with traditional datasets. However, these datasets remain constrained in sample volume. By contrast, the proposed algorithm employs a graph-based circuit generation approach for gate-level circuits focused on power consumption analysis. This method liberates itself from dependence on open-source RTL codes, enabling the generation of an unlimited array of samples by configuring computational graph parameters. Moreover, the resulting circuits exhibit diverse and intricate topologies, facilitating ML models in effectively learning the internal circuit topologies.

4.4 Static timing analysis

In digital circuit systems, maintaining the correct timing relationship is crucial, as improper timing can lead to erroneous circuit behavior. This employs static timing analysis (STA) to verify the signal integrity of the circuit and ascertain if the design constraints are met. We used Synopsys PrimeTime (PT) for this analysis and set the clock period of the sequential circuit as 10ns.

As shown in Fig. 3, both the maximum and minimum time slacks of the sequential circuits exceed 0. As the circuit size increases, the minimum margins remain stable, while the maximum margins decrease to the level of 10^{-2} ns. Since combinational circuits

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Table 2: Comparison between the proposed power consumption dataset and the ML EDA dataset of application specific integrated circuit (ASIC) and field programmable gate array (FPGA) in existing studies

Work	# Cases	# Sources	Platform & Level	Usage
CircuitNet (Chai et al., 2022)	20 k	6	ASIC PR design	DRC; IR drop
OpenABC-D (Chowdhury et al., 2021)	870 k	29	ASIC RTL	Synthesis
HLSDataset (Wei et al., 2023)	19 k	34	FPGA HLS	Power; timing
Spector (Gautier et al., 2016)	8 k	9	FPGA HLS	NA
Proposed	∼ unlimited	NA	ASIC gate-level Verilog	Power

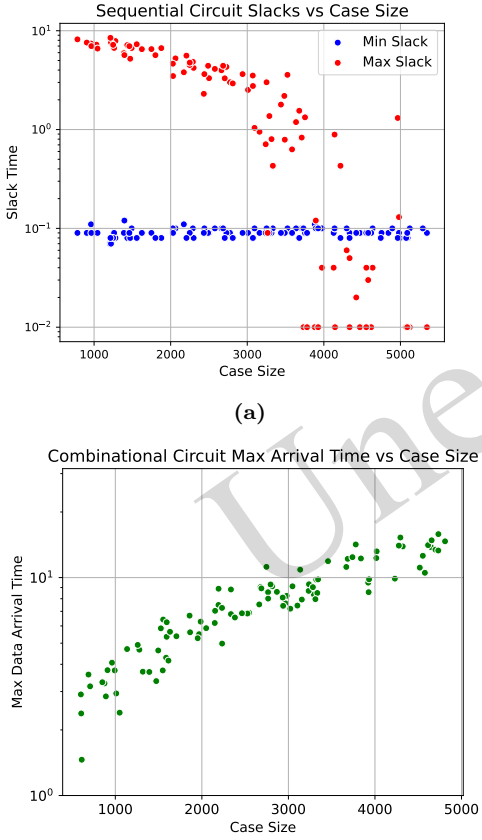

Fig. 3: Relationship between STA and circuit size, (a) shows the slacks of the sequential circuit, and (b) shows the maximum arrival time of the signal of the combinational circuit

lack clock constraints, our research also examines the maximum arrival time from the primary input to the primary output in these circuits. We observed that the maximum signal arrival time increases with the circuit size, reaching up to 16 ns.

In conclusion, the timing slacks identified are sufficient, validating the reliability of our proposed pseudo-circuit dataset.

4.5 Experiment of different power analysis methods

This section evaluates the performance of prevalent average power analysis methods applied to digital circuits at the pre-layout routing stage, using our dataset. We examine the capabilities of mainstream software algorithms for vectorless power analysis as comparative methods. Power focuses on the average power types prevalent in mainstream digital integrated circuits: leakage power, internal power, and switching power. The industry software tools analyzed include PTPX and Voltus, while OpenROAD's OpenSTA(Ajayi and Blaauw, 2019) is used solely for power analysis in sequential circuits, given its inability to perform such analysis in combinational circuits.

The "Golden" result is established through a random vector test. Initially, the highly accurate activity traces are evaluated using the Monte Carlo method, which applies random vectors to assess circuit activity across generated samples. The testing utilizes Synopsys VCS software to simulate and generate circuit activity files. These files, alongside netlists, constraints, process libraries, and other relevant data, are input into PTPX for comprehensive power consumption analysis.

Subsequent to these simulations, the circuit activity file, along with other netlists, constraints, and process library files, is imported into PTPX to determine the final power analysis results. A vectorless power analysis, employed as a control in each software, does not require reading the circuit activity file. Instead, it directly performs power analysis based on the primary input signal probability and toggle rate. This vectorless analysis is then compared to the Golden to quantify discrepancies.

In this context, signal probability is defined as the ratio of the duration at a high signal level to the

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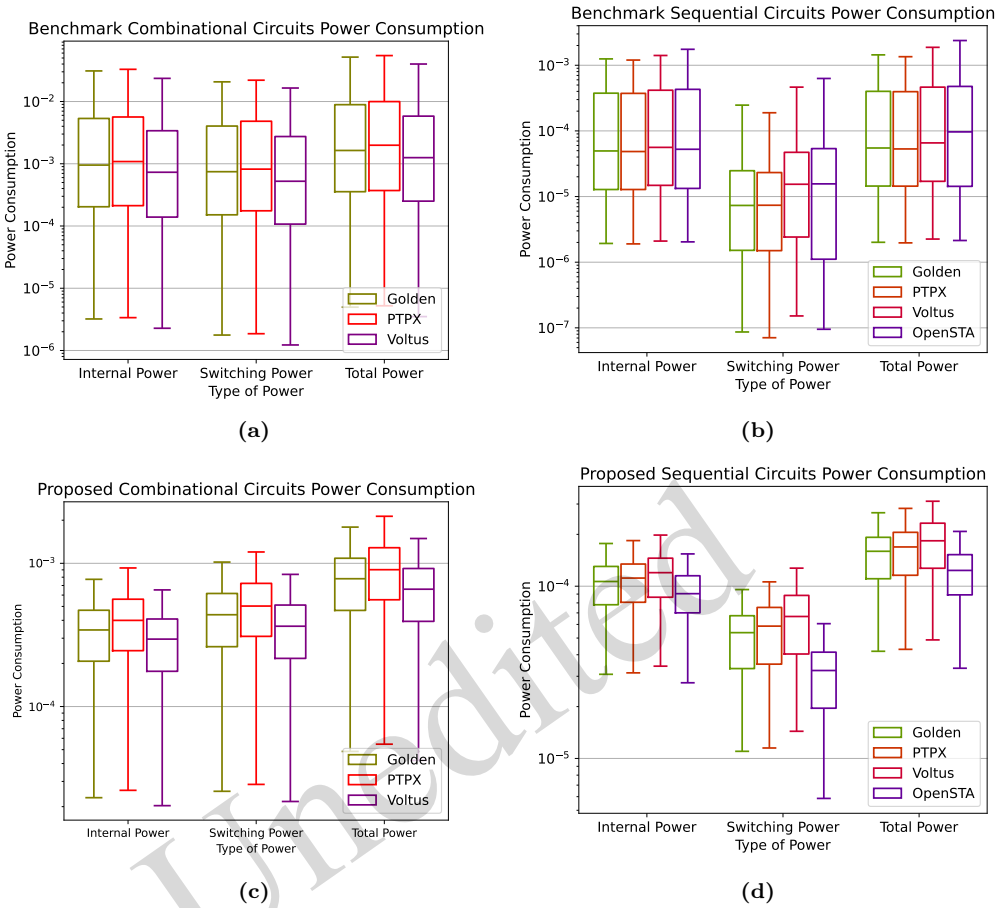

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Fig. 4: Results of the three power consumption statistics for all samples are shown on the left for combinational circuits and on the right for sequential circuits. (a)-(d) show the benchmark combinational circuit power consumption, benchmark sequential circuit power consumption, proposed combinational circuit power consumption, proposed sequential circuit power consumption

total test period, while the toggle rate refers to the ratio of signal transitions relative to the same test duration.

Specific parameters are set as follows: The signal probability at the primary input port is fixed at 0.5, and the toggle rate varies randomly between 0.01 and 0.4. The signal transfer time is designated as 0.05 ns, with a clock period of 10 ns for sequential circuits.

To demonstrate the validity of the proposed power dataset, a benchmark comprising a blend of wildly acknowledged academic and industrial datasets was created. The combinational circuit benchmark includes samples from ISCAS85 (Hansen et al., 1999) and EPFL (Amarú et al., 2015), and Oracle's OpenSPARC (Parulkar et al., 2008) open-source project. The sequential circuit benchmark is derived from ISCAS89 (Brglez et al., 1989).

To elucidate the outcomes of various average power analysis algorithms, we analyzed the internal, switching, and total power consumption across all samples and derived the powers corresponding to probability density distributions. However, leakage power was excluded due to its negligible error margin. Fig. 4 displays the power consumption test box plots for both the benchmark and generated datasets, highlighting the mean power consumption values and the upper and lower distribution limits.

In combinational circuits, the values of internal, switching, and total power indicate that, compared to Golden's results, PTPXs are higher, whereas Voltus's results are lower. The power trend in the proposed dataset aligns with that of the benchmark dataset. In sequential circuits, PTPX aligns most

closely with Golden's average values in the benchmark dataset, while Voltus and OpenSTA exhibit substantial discrepancies. Although the generated dataset trends align with PTPX and Voltus from the benchmark dataset, they diverge from OpenSTA. Considering being an open-source tool, OpenSTA's calculations lack precision, whereas PTPX and Voltus, as industry standards, provide more reliable results.

The data distribution range for the benchmark dataset spans from 10 gates to $400k$ gates, while the generated dataset predominantly encompasses around $10k$ gates. This discrepancy arises due to the prevalent use of circuits sized around $5k$ gates in the field of deep learning EDA power estimation and probabilistic prediction (Shi et al., 2023), which influences the bounds of case size distributions across different datasets.

The consistency in power consumption distribution trends between PTPX and Voltus corroborates the practical utility of the proposed algorithm.

4.6 Exploring circuit topology complexity

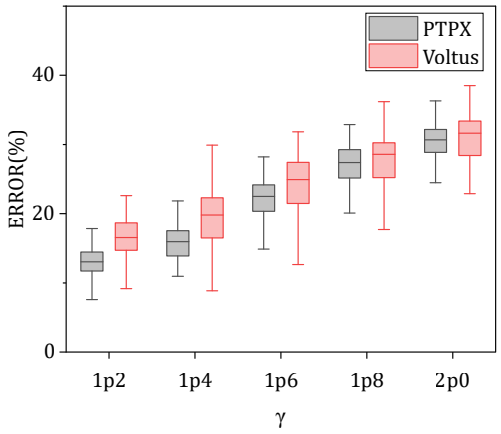
We will further illustrate the effectiveness of the proposed algorithm in terms of circuit topology complexity. Sequential circuits are derived from combinational circuits, so this section focuses on topological complexity analysis of combinational circuits. Assuming that the number of IO ports and the number of internal interconnects are determined, the complexity of the combinational circuits can be adjusted by the expectation γ of the number of nodes mentioned in Algorithm 1.

We define the error between different methods as follows:

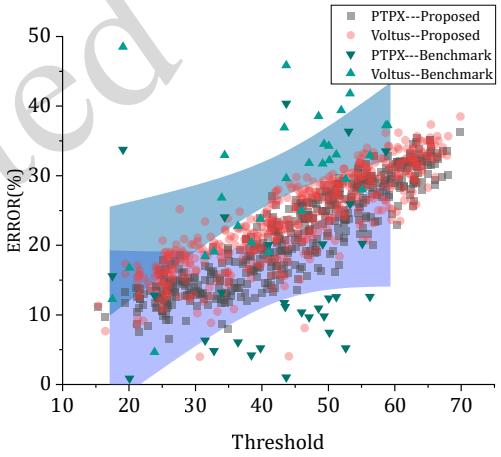
$$ERR\% = \frac{|P_{vectorless} - P_{\text{golden}}|}{P_{\text{golden}}} \times 100, \quad (4)$$

where $P_{\text{vectorless}}$ is vectorless power analysis method, including PTPX, Voltus, and OpenSTA; and P_{golden} is the Golden power.

Under different circuit complexity, the errors of PTPX and Voltus behave differently when the same input stimulus is guaranteed. The higher the circuit topology complexity, the higher the spatial correlation of the signals inside the circuit, and the higher the power errors of PTPX and Voltus, using this point, we obtain Fig. 5a, where γ takes the values of 1.2, 1.4, 1.6, 1.8 and 2.0. For example, $\gamma = 1.2$ means that the probability of a node having two fan-ins is 0.2, the probability of one fan-in is 0.8, the expected number of fan-in nodes is 1.2, and so on. According to Fig. 5a, as γ increases, the circuit complexity rises, and the power consumption errors of both PTPX and Voltus rise, proving the effectiveness of γ on the circuit complexity.



(a) Effect of γ value on power consumption error



(b) Threshold measures, where the upper blue region is the 95% confidence interval of the PTPX error for benchmark and the lower purple region is the 95% confidence interval of the Voltus error.

Fig. 5: Experiments on the topological complexity of the generated combinational circuits, where the vertical coordinates are all the total power consumption errors. (a) shows the effect of the γ, and (b) shows the threshold measures

To further illustrate the effectiveness of the proposed algorithm, we validate it from the perspective of circuit complexity in comparison with a standard dataset. We first propose a measure to describe the circuit complexity: the threshold measure. The

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Algorithm 4 Threshold Measurement

Require: Circuit topology G, input pin signal probability.
Ensure: Measurements T

```
Topo ← Topology ordering of G;
N ← Number of nodes of G;
T ← 0;
for n ∈ Topo do
    Calculate the n signal probability p and the flip rate t according to the circuit logic;
    if t > 0.2 then
        t ← 0.2;
        T ← T + 1;
    end if
end for
T ← (T/N) × 100;
```

threshold measure is described in Algorithm 4, i.e., the signal probability and toggle rate of the circuit are analyzed by inference. Due to the influence of circuit spatial correlation, the toggle rate tends to increase with the deepening of the circuit hierarchy, and the threshold measure mainly plays the role of resetting the toggle rate when the set threshold is reached and adding up the number of times that the threshold is triggered, and the probability of triggering the threshold is taken as a threshold measure after the completion of the inference at all the nodes.

The signal probability is the probability of the signal being high, and the toggle rate is the frequency of flipping during the test cycle. The calculation of SP and TR does not take into account the spatial correlation of the signals, e.g., for a NAND logic gate with two inputs, A and B, the signal probability of its output pin, Z, is $SP(Z) = 1 - SP(A) \times SP(B)$, and the toggle rate is $TR(Z) = SP(A) \times TR(B) + SP(B) \times TR(A)$. As the circuit hierarchy deepens, signal spatiality accumulates resulting in a large t, and using this feature, we approximate the complexity of the circuit by setting a threshold and resetting t to characterize the circuit. The circuits generated under different γ are compared with the benchmark dataset to compute the threshold measures, and the power consumption error distributions of PTPX and Voltus are statistically obtained in Fig. 5b. The error distributions of the proposed algorithm are in the 95% confidence interval of the benchmark algorithm, and the trend is basically the same, which validates the effectiveness of the proposed algorithm for the generation of the dataset from the viewpoint of the circuit topology.

4.7 Sample generation time overhead

The time to generate a dataset with a large number of samples requires high generation efficiency for each sample. The time used for generating a single sample includes the steps of pseudo netlist generation, DC synthesis processing, and power analysis. while synthesis and power test are standard chip processes, we discuss the efficiency of pseudo-netlist generation. Considering that the sequential circuits are based on combinational circuits with gate-level register components, the key factor of generation efficiency is the generation time overhead of the DAG topology, i.e., the algorithmic efficiency discussed in Section 2. To test the efficiency of the algorithm, we generated $1k$ pseudo-netlists of different combinational circuits ranging in size from a few gates to $20k$ gates.

The test hardware platform is Intel Xeon CPU E5-2695 v3 @ 2.30 GHz Dual-CPU server, which has a maximum of 56 threads, and a single sample is run on a single thread. As shown in Fig. 6, there is an approximately linear relationship between the sample size and the time overhead of generating DAGs. The test here generates a maximum circuit of $24k$ gates, which takes nearly 40 min. However, the samples can be generated in parallel, and for multiple sample datasets, parallel computation can significantly reduce the runtime.

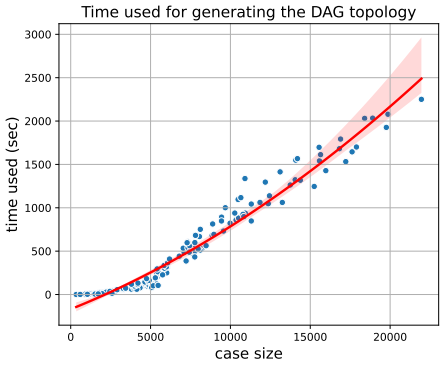

Fig. 6: Time overhead for generating DAGs of different sizes

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4.8 Exploring sequential circuits zero values phenomenon

Due to the effect of loops in the circuit, the sequential circuit may have no signal switching registers in some wires throughout the test duration. For sequential circuits with a large number of loops, a large number of nodes with no signal switching implies that the switching and short-circuit power consumption in the circuit tend to be zero-valued, and the circuit's vectorless average power consumption tends to be the same as that of the leakage power consumption. The proposed algorithm can control the percentage of zero values of switching activity in sequential circuits by adjusting the sequential circuit generation factor α defined in Section 3. We first set up 100 circuits with α ranging from 0.01 to 1.0, with all other parameters being equal, to test their circuit activation performance. According to Fig. 7a as the sequential circuit generation factor α increases, there are more feedback loops in the circuits, and the Monte Carlo random vectors are used to test the internal switching activity of the circuits, and we find that the proportion of non-zero values is decreasing, which also indicates that the increase of feedback loops in the circuits will make the circuit switching activity deteriorate, and this type of high α value circuits corresponds to the storage circuits with high α values. The high α value circuits correspond to the storage circuit model, while the low α value circuits correspond to the computational task circuit model. The α has an approximately linear correlation with the percentage of zeros in Monte Carlo-tested circuits, and the results show that this linear relationship is independent of the size of the circuit.

We also tested the vectorless power analysis algorithms with different generation factors α, as shown in Fig. 7b, using the same sample circuits as in Fig. 7a to test the error performance of different algorithms in terms of the average power dissipation on these samples, and in order to normalize the results, the error computation method is different from that of the previous section. The error calculation differs from the previously mentioned one:

$$ERR\% = \frac{|P_{\text{vectorless}} - P_{\text{golden}}|}{\max(P_{\text{golden}}, P_{\text{vectorless}})} \times 100. \quad (5)$$

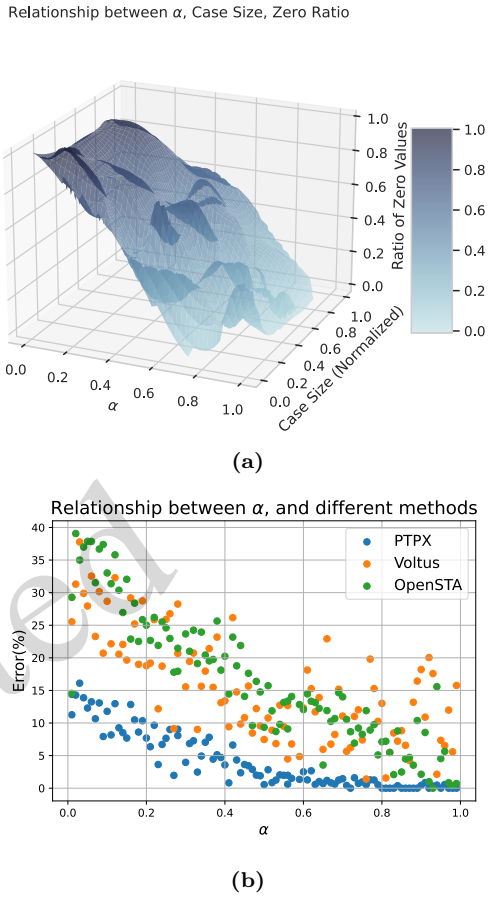

Fig. 7: Sequential circuit Monte Carlo method for flipping active non-zero value duty cycle tests. (a) Effect of α on circuit flip-flop activity, and (b) Performance of different power test methods for different α values of power analysis results

According to Fig. 7b, as the circuit generation factor increases from 0 to 1 , the PTPX has the smallest error value for the average power consumption, which is at the bottom of the list. The errors of Voltus and OpenSTA are larger, especially when α tends to 0, i.e., the setting generates less register loop topology, and the circuits tend to be combinational circuits, the Voltus and OpenSTA errors are both larger than the PTPX. When α tends to 1, according to Fig. 7a the percentage of zeros in the circuit rises, the error of PTPX is close to 0%, and the errors of Voltus and OpenSTA also decrease.

In summary, based on the results in Fig. 7, we can control the topology of the circuit by adjusting the sequential circuit generation factor α to generate richer sequential circuit samples.

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5 Conclusions

In response to the current increase in demand for power consumption analysis circuit amounts, this study proposed a novel method for generating abundant pseudo-datasets for power consumption analysis. Unlike traditional approaches, our method utilizes graph topology computations to efficiently generate random DAG structures. These DAGs are then transformed into pseudo-combinatorial circuit netlists, with registers added to convert them into pseudo-sequential circuit netlists. We manage the complexity of these circuits by setting an expected node count γ and address the zero-value problem in power analysis of sequential circuits by introducing a sequential circuit generation factor α that influences their topology. The gate-level description netlists produced are subject to DC synthesis constraints to create the pseudo-dataset. We validated this dataset using mainstream power analysis tools such as PTPX, Voltus, and OpenSTA, comparing power consumption results against a standard dataset. Additional evaluations included timing and DAG generation time, and an investigation into the zero-value phenomenon of sequential circuits. Our findings demonstrate that the proposed algorithm can rapidly and efficiently generate a large and diverse set of pseudo-combinatorial and sequential circuit samples. By examining complexity and comparing it with benchmark datasets, the results demonstrate and validate the effectiveness of the proposed dataset.

Future research will focus on generating larger-scale pseudo-circuits and expanding the methodology to other areas of IC design, such as IR drop, to enhance the application of learning-based methods within the EDA field.

Contributors

Zejia LYU conducted the investigation, experimental validation, data organization, and drafted the original paper. Jizhong SHEN provided experimental guidance, supervision, paper review, and editing. Xi CHEN assisted with investigation and validation.

Conflict of interest

All the authors declare that they have no conflict of interest.

Data availability

The data that support the findings of this study are available from the corresponding author upon reasonable request.

References

Ajayi T, Blaauw D, 2019. Openroad: Toward a self-driving, open-source digital layout implementation tool chain. Proc of Government Microcircuit Applications and Critical Technology Conf, p.1105-1110.

Amarú L, Gaillardon PE, De Micheli G, 2015. The epfl combinational benchmark suite. Proc of the 24th Int Workshop on Logic & Synthesis.

Amid A, Biancolin D, Gonzalez A, et al., 2020. Chipyard: Integrated Design, Simulation, and Implementation Framework for Custom SoCs. *IEEE Micro*, 40(4):10-21. https://doi.org/10.1109/MM.2020.2996616

Rakesh MB, Das P, Sai Pranav KR, et al., 2023. GRILAPE: Graph Representation Inductive Learning-based Average Power Estimation for Frontend ASIC RTL Designs. 36th Int Conf on VLSI Design and 2023 22nd Int Conf on Embedded Systems , Hyderabad, India, p.1-6. https://doi.org/10.1109/VLSID57277.2023.00053

Brglez F, Bryan D, Kozminski K, 1989. Combinational Profiles of Sequential Benchmark Circuits. IEEE Int Symp on Circuits and Systems, p.1929-1934. https://doi.org/10.1109/ISCAS.1989.100747

Burch, Najm, Yang, et al., 1992. McPOWER: A Monte Carlo approach to power estimation. IEEE/ACM Int Conf on Computer-Aided Design, Santa Clara, CA, USA, p.90-97. https://doi.org/10.1109/ICCAD.1992.279392

Chai ZM, Zhao YX, Lin YB, et al., 2022. CircuitNet: An open-source dataset for machine learning applications in electronic design automation (EDA). *Sci China Inf Sci*, 65(12):227401, s11432-022-3571-8. https://doi.org/10.1007/s11432-022-3571-8

Chowdhury AB, Tan B, Karri R, et al., 2021. OpenABC-D: A Large-Scale Dataset For Machine Learning Guided Integrated Circuit Synthesis. https://doi.org/10.48550/arXiv.2110.11292.

Corno F, Reorda M, Squillero G, July-Sept./2000. RT-level ITC'99 benchmarks and first ATPG results. *IEEE Des Test Comput*, 17(3):44-53. https://doi.org/10.1109/54.867894

Fang WJ, Lu Y, Liu S, et al., 2023. MasterRTL: A Pre-Synthesis PPA Estimation Framework for Any RTL Design. IEEE/ACM Int Conf on Computer Aided Design, San Francisco, CA, USA, p.1-9. https://doi.org/10.1109/ICCAD57390.2023.10323951

Gautier Q, Althoff A, Meng PF, et al., 2016. Spector: An OpenCL FPGA benchmark suite. Int Conf on Field-Programmable Technology, Xi'an, China, p.141-148. https://doi.org/10.1109/FPT.2016.7929519

Hansen MC, Yalcin H, Hayes JP, July-Sept./1999. Unveiling the ISCAS-85 benchmarks: A case study in reverse engineering. *IEEE Des Test Comput*, 16(3):72-80. https://doi.org/10.1109/54.785838

Kaeslin H, 2008. Digital Integrated Circuit Design: From VLSI Architectures to CMOS Fabrication. Cambridge University Press, New York, USA, p.386-458. https://doi.org/doi.org/10.1017/CBO9780511805172

Unedited

Khan S, Shi ZY, Li M, et al., 2024. Deepseq: Deep sequential circuit learning. Design, Automation & Test in Europe Conf & Exhibition, p.1-2. https://doi.org/10.23919/DATE58400.2024.10546639

Kumar AKA, Gerstlauer A, 2019. Learning-Based CPU Power Modeling. ACM/IEEE 1st Workshop on Machine Learning for CAD , Canmore, AB, Canada, p.1-6. https://doi.org/10.1109/MLCAD48534.2019.9142100

Kumar AKA, Al-Salamin S, Amrouch H, et al., 2023. Machine Learning-Based Microarchitecture- Level Power Modeling of CPUs. *IEEE Trans Comput*, 72(4):941-956. https://doi.org/10.1109/TC.2022.3185572

Li M, Khan S, Shi Z, et al., 2022. DeepGate: Learning neural representations of logic gates. Proc of the 59th ACM/IEEE Design Automation Conf, San Francisco California, p.667-672. https://doi.org/10.1145/3489517.3530497

Najm FN, Feb./1993. Transition density: A new measure of activity in digital circuits. *IEEE Trans Comput Aided Des Integr Circuits Syst*, 12(2):310-323. https://doi.org/10.1109/43.205010

Nasser Y, Lorandel J, Prévotet JC, et al., 2021. RTL to Transistor Level Power Modeling and Estimation Techniques for FPGA and ASIC: A Survey. *IEEE Trans Comput Aided Des Integr Circuits Syst*, 40(3):479-493. https://doi.org/10.1109/TCAD.2020.3003276

OnchipUIS, 2016. MRISCV: A 32-bit Microcontroller featuring a RISC-V core. https://github.com/onchipuis/mriscv

OnchipUIS, 2021. VexRiscv: A FPGA friendly 32 bit RISC-V CPU implementation. https://github.com/SpinalHDL/VexRiscv

Parulkar I, Wood A, Hoe JC, et al., 2008. Opensparc: An open platform for hardware reliability experimentation. 4th Workshop on Silicon Errors in Logic-System Effects, p.1-6.

Shi ZY, Pan HY, Khan S, et al., 2023. DeepGate2: Functionality-Aware Circuit Representation Learning. IEEE/ACM Int Conf on Computer Aided Design, p.1-6. https://doi.org/10.1109/ICCAD57390.2023.10323798

OpenCores Team, 2024. OpenCores Homepage. https://opencores.org/.

Wei ZG, Arora A, Li RH, et al., 2023. HLSDataset: Open-Source Dataset for ML-Assisted FPGA Design using High Level Synthesis. IEEE 34th Int Conf on Application-specific Systems, Architectures and Processors, Porto, Portugal, p.197-204. https://doi.org/10.1109/ASAP57973.2023.00040

Xie ZY, Pan JY, Chang CC, et al., 2023a.Y The Dark Side: Security and Reliability Concerns in Machine Learning for EDA. *IEEE Trans Comput Aided Des Integr Circuits Syst*, 42(4):1171-1184. https://doi.org/10.1109/TCAD.2022.3199172

Xie ZY, Zhang T, Peng YF, 2023b. Security and Reliability Challenges in Machine Learning for EDA: Latest Advances. 24th Int Symp on Quality Electronic Design, San Francisco, CA, USA, p.1-6. https://doi.org/10.1109/ISQED57927.2023.10129359

Xie ZY, 2023. Efficient Runtime Power Modeling with On-Chip Power Meters. Proc Int Symp on Physical Design, Virtual Event USA, p.168-174. https://doi.org/10.1145/3569052.3578927

YosysHQ, 2021. PicoRV32—A Size-Optimized RISC-V CPU. https://github.com/YosysHQ/picorv32

Zhang YQ, Ren HX, Khailany B, 2020. GRANNITE: Graph Neural Network Inference for Transferable Power Estimation. 57th ACM/IEEE Design Automation Conf , San Francisco, CA, USA, p.1-6. https://doi.org/10.1109/DAC18072.2020.9218643

Zhou GF, Zhou JY, Lin HJ, 2018. Research on nvidia deep learning accelerator. 12th IEEE Int Conf on Anti-counterfeiting, Security, and Identification, p.192-195. https://doi.org/10.1109/ICASID.2018.8693202

Zhou Y, Ren HX, Zhang YQ,, et al., 2019. PRIMAL: Power Inference using Machine Learning. Proc of the 56th Annual Design Automation Conf, article 39. https://doi.org/10.1145/3316781.3317884

Zou SN, Zhang JX, Shi BZ, et al., 2024. PowerSyn: A Logic Synthesis Framework With Early Power Optimization. *IEEE Trans Comput Aided Des Integr Circuits Syst*, 43(1):203-216. https://doi.org/10.1109/TCAD.2023.3297069

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