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Series transformer based diode-bridge-type solid state fault current limiter

Key words: Solid state fault current limiter (SSFCL), Power quality, Voltage sag, Point of common coupling (PCC), Isolation transformer

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Introduction

- An ideal FCL should have zero impedance in its normal operation mode, high impedance during fault conditions, quick response to fault occurrence, fast recovery after fault clearance, acceptable reliability, and also low cost. Bridge-type FCLs use a current fed full-bridge converter. This topology is inherently suitable for using switches (diodes, thyristors, or other power electronic switches) as line commutated switches.
- In this paper, the proposed solid state FCL (SSFCL) has a simple and applicable structure, which can limit the magnitude of the fault current to a certain and safe value. Also, the proposed structure can reduce the harmonic distortion and switching overvoltages, and adjust the PCC voltage. The comparative study of the suggested SSFCL with the FCL presented in Abapour and Hagh (2009) shows its superior characteristics. The SSFCL operation in normal and faulty conditions is studied and the experimental prototype clearly confirms the simulation results.

Electrical network topology

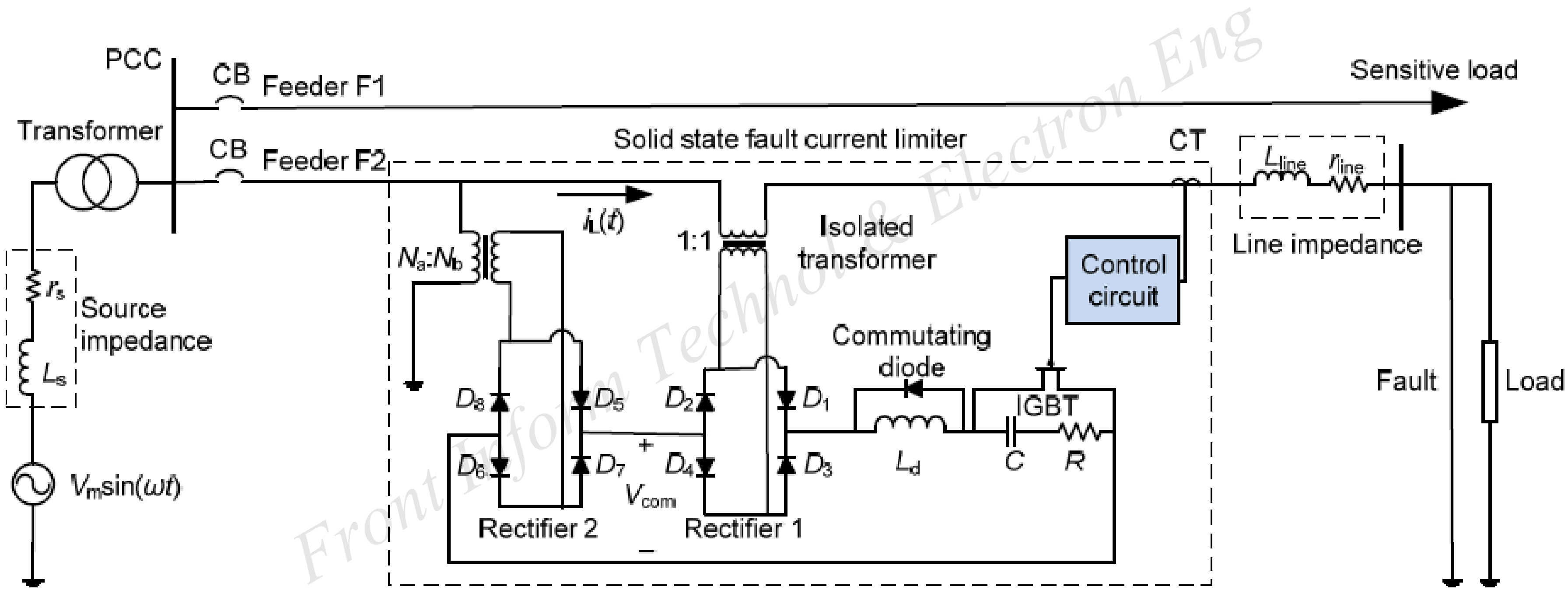


Fig. 1 Single-line diagram of the electrical network including the proposed SSFCL

SSFCL operation principles

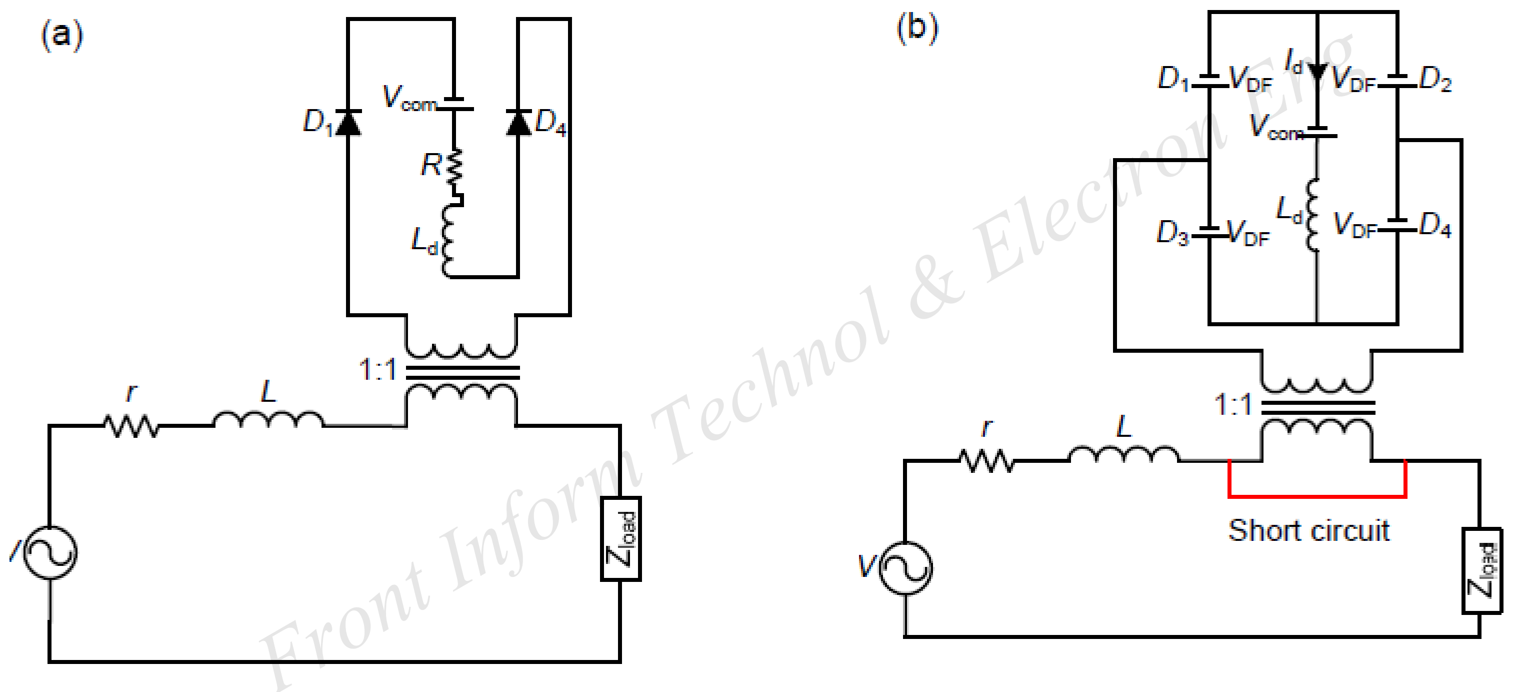


Fig. 2 Electrical network equivalent circuit in the normal mode: (a) charging mode; (b) discharging mode

SSFCL operation principles (Con’d)

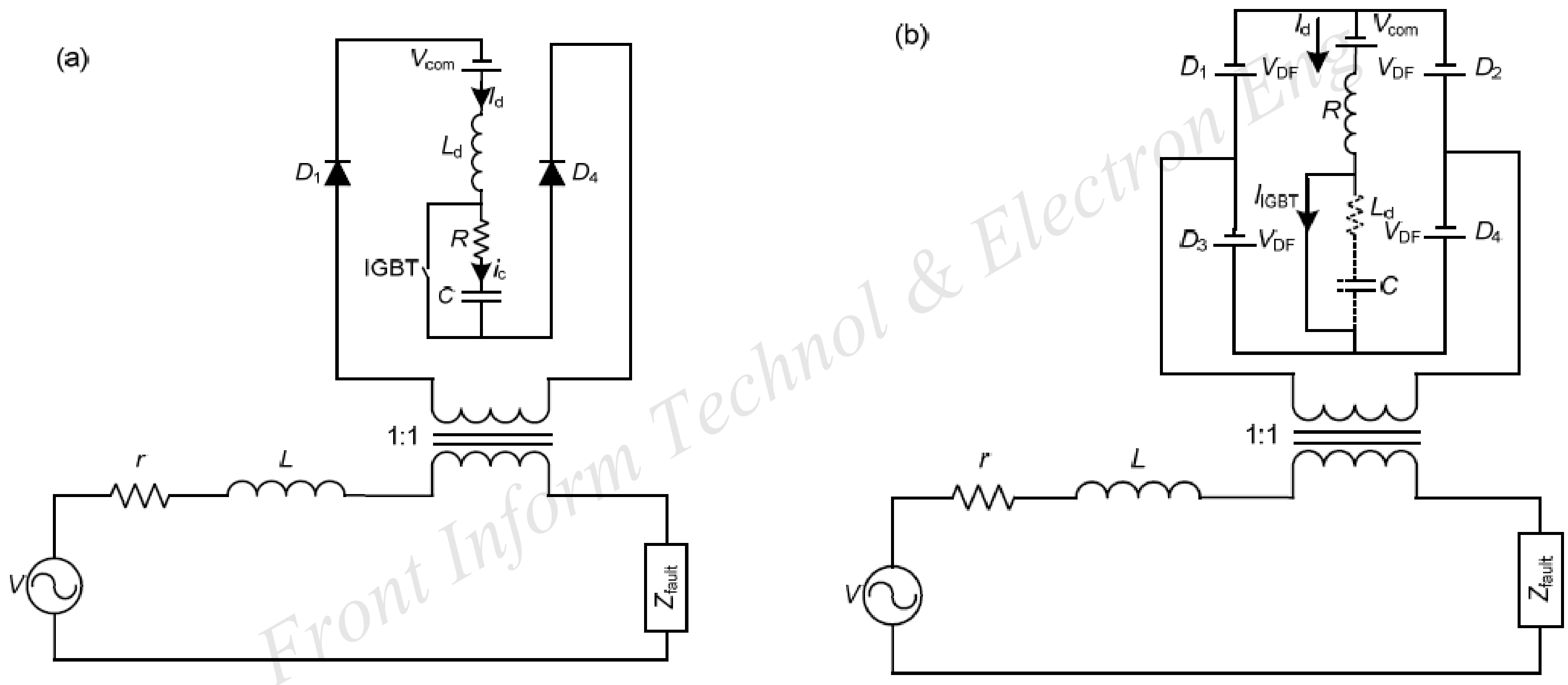


Fig. 3 Electrical network equivalent circuit during fault: (a) charging mode; (b) discharging mode

Simulation results

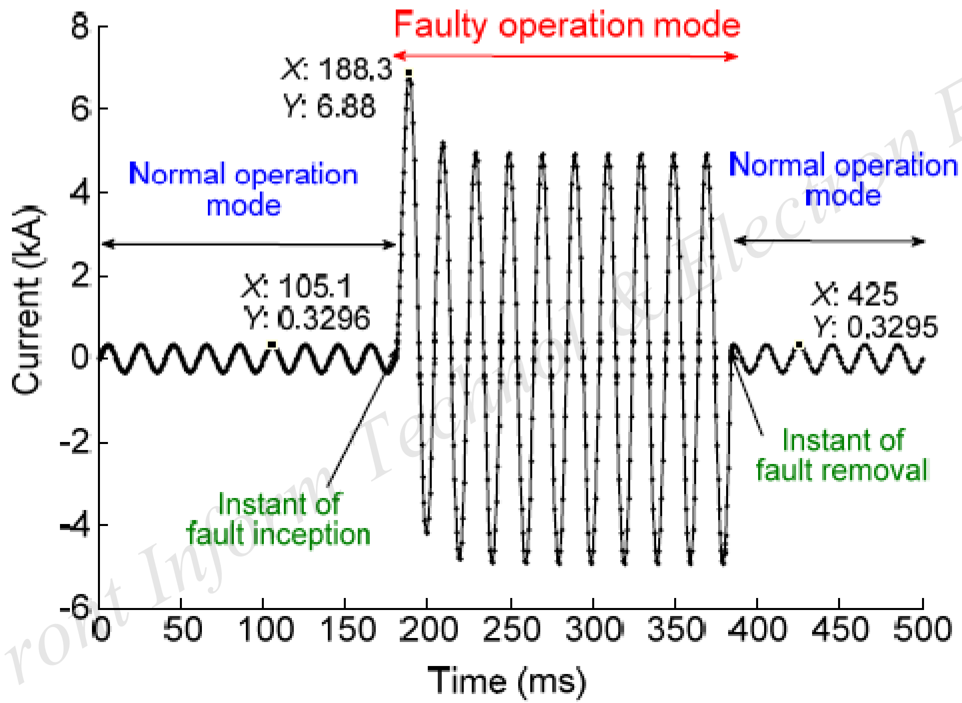


Fig. 5 Line current during the pre-fault, fault, and post-fault modes without using SSFCL

Simulation results (Con'd)

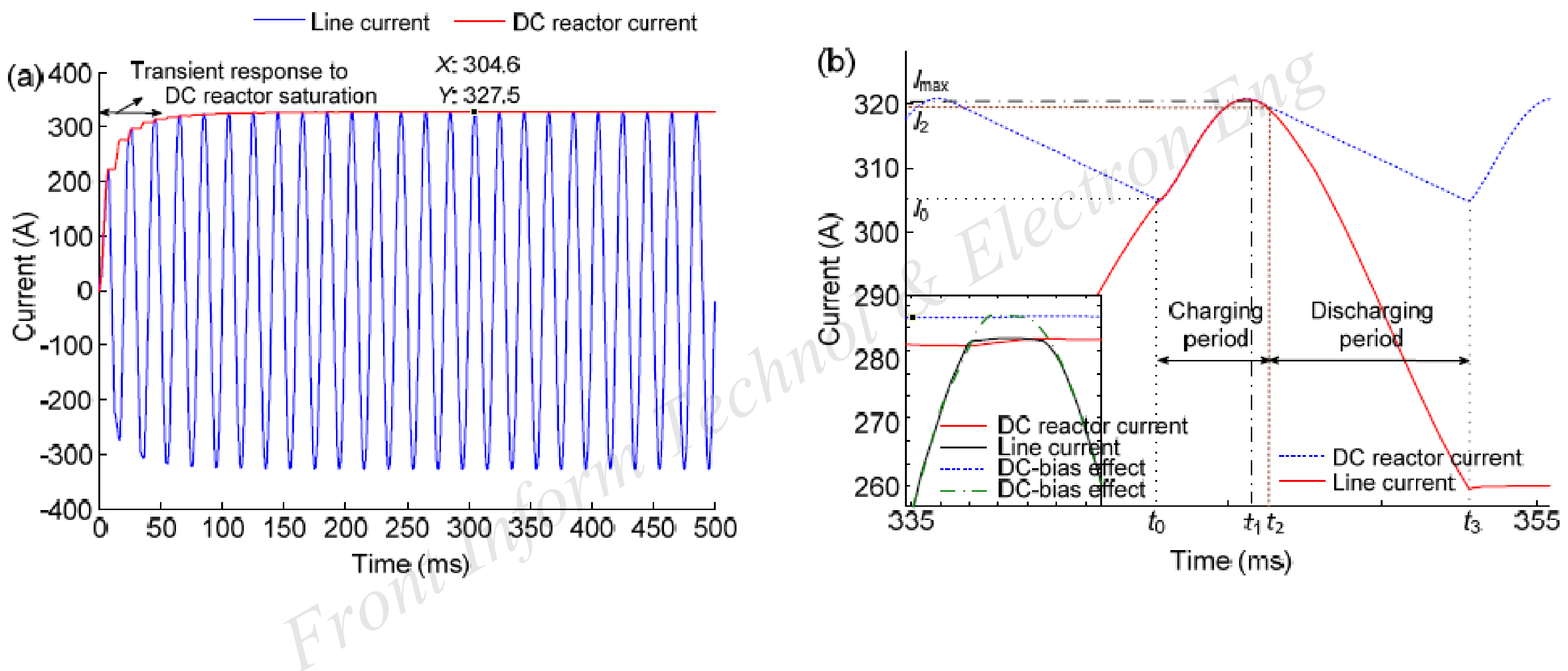


Fig. 6 DC reactor current in the normal operation mode while IGBT is on: (a) normal view; (b) expanded view

Simulation results (Con'd)

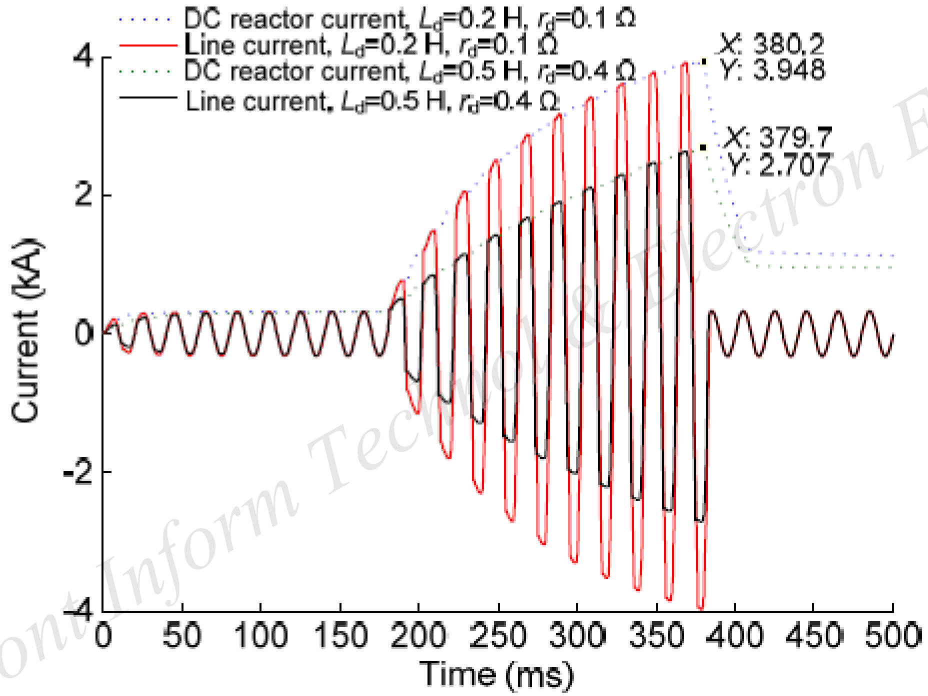


Fig. 7 Line and DC reactor currents in the normal, fault, and post-fault operation modes (IGBT and RC branch are not connected)

Simulation results (Con'd)

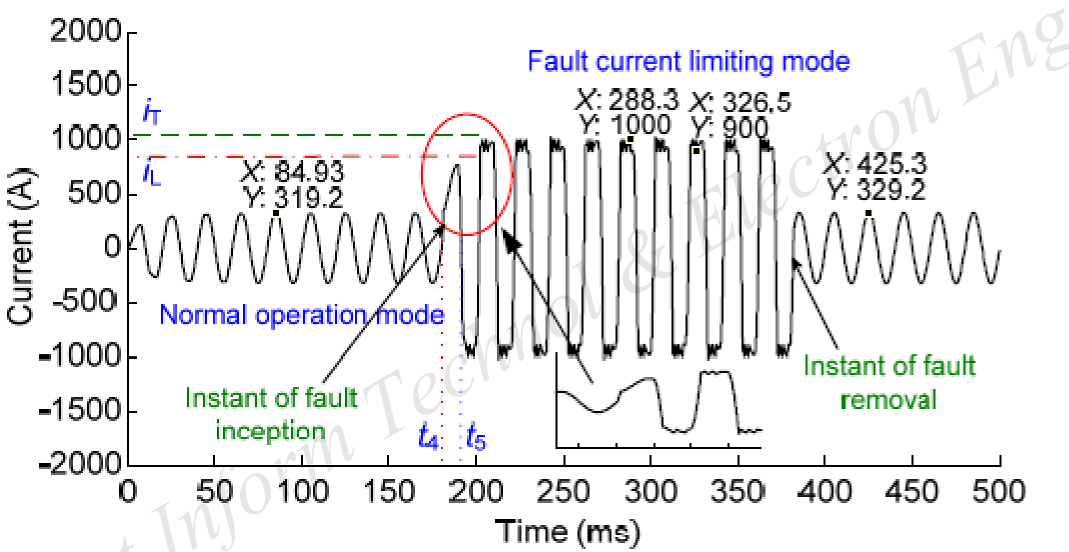


Fig. 8 Line current during the normal, fault, and post-fault operation modes with a proper duty cycle of IGBT

Experimental results

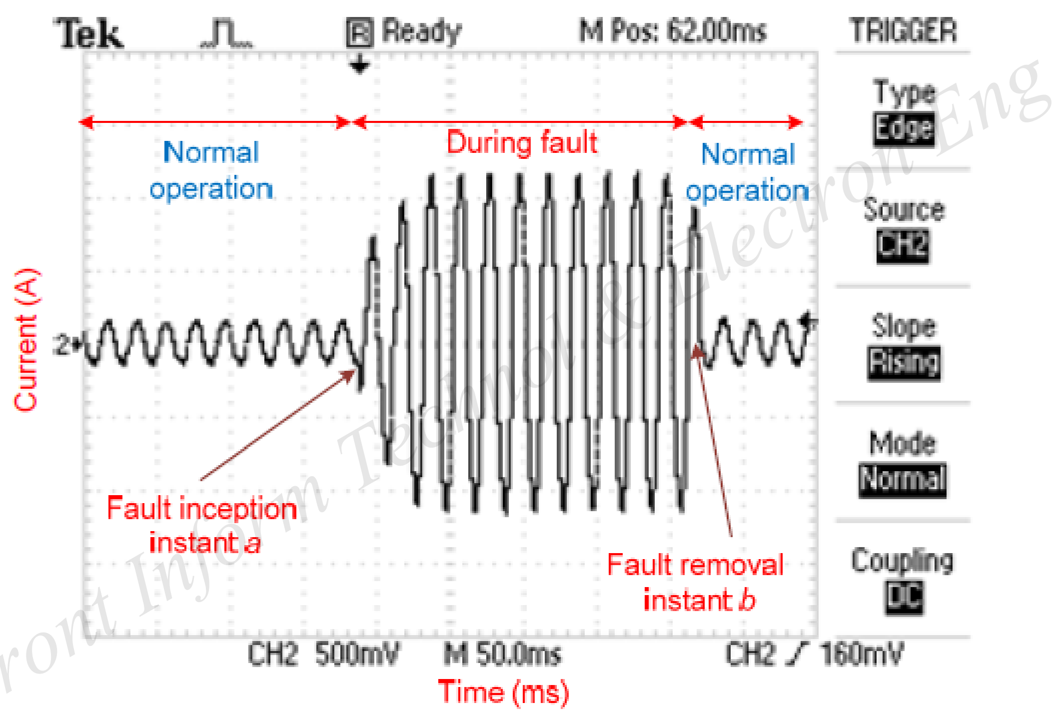
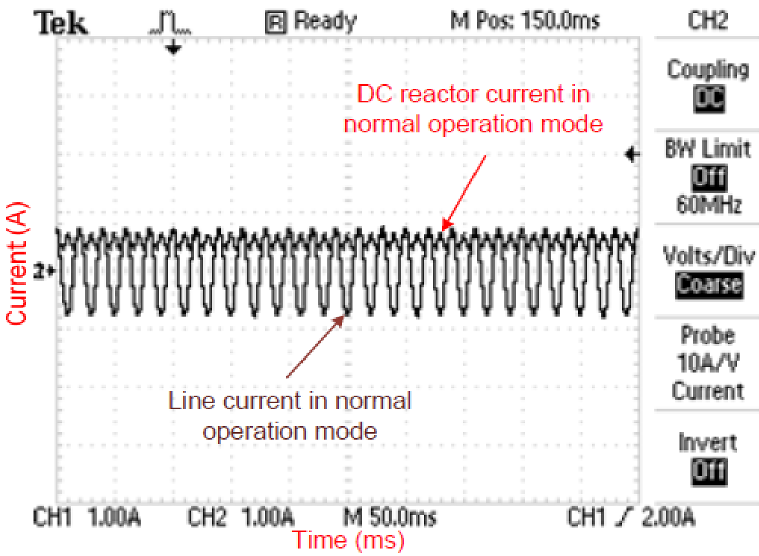
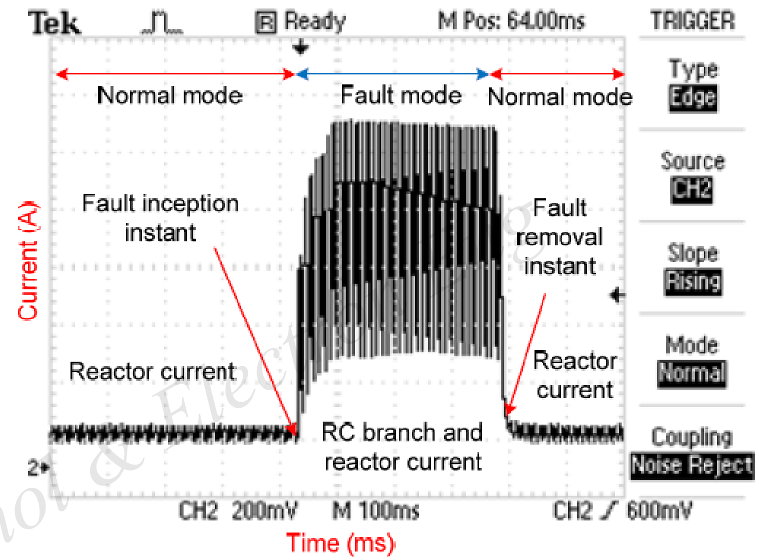


Fig. 14 SSFCL effect on line current during the normal, fault, and post-fault modes (current/division=500 mA with probe X3 and time/division=50 ms)

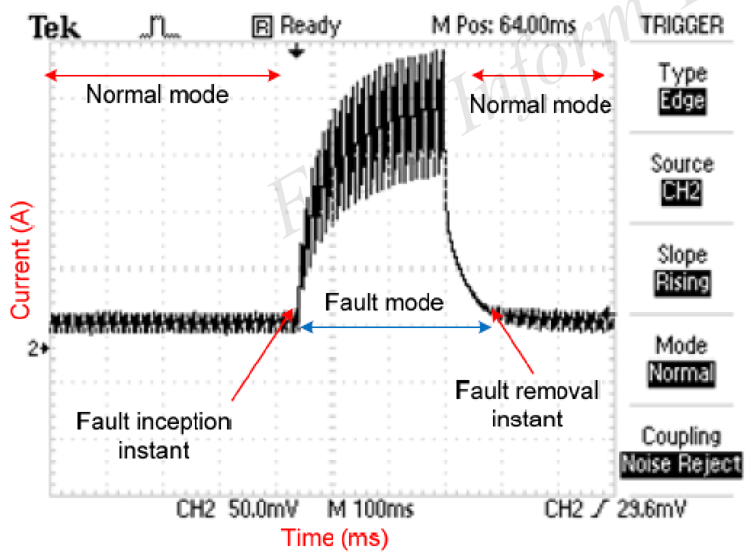
Experimental results (Con’d)



(a)



(b)



(c)

Fig. 15 Line, series RC branch, and DC reactor currents during normal and faulty operation modes

(a) Line and reactor currents in the normal operation mode (current/division=1 A with probe X1 and time/division= 50 ms); (b) Series RC branch and IGBT current in normal and faulty operation modes (current/division=200 mA with probe X6 and time/division=100 ms); (c) DC reactor current in normal and faulty operation modes (current/division= 50 mA with probe X100 and time/division=100 ms)

Conclusions

The main advantages of the suggested SSFCL is organized as follow:

- An improved SSFCL configuration
- Lower switching overvoltage compared with similar structures
- Lower initial cost
- Acceptable power losses
- Reduction of the inductance and current rating of the DC reactor
- Lower IGBT overvoltage
- Reduced cooling system cost
- SSFCL structure is simple
- Better power quality