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# Multi-stage dual replica bit-line delay technique for process-variation-robust timing of low voltage SRAM sense amplifier

**Key words:** Process-variation-robust, Sense amplifier (SA), Replica bit-line (RBL) delay, Timing variation

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# Introduction

- Sense-amplifier enable (SAE) signal should be activated accurately for reliable read operation in high speed and low-power SRAM design.
- With fabrication technology scaling, the conventional RBL technique cannot track the  $V_{TH}$  variation of the transistor particularly for low-supply applications.
- A multi-stage dual replica bit-line delay (MDRBD) technique for further suppressing the SAE timing variation for low voltage SRAM applications is presented.

# Multi-stage dual replica bit-line delay technique with emphasis on this work

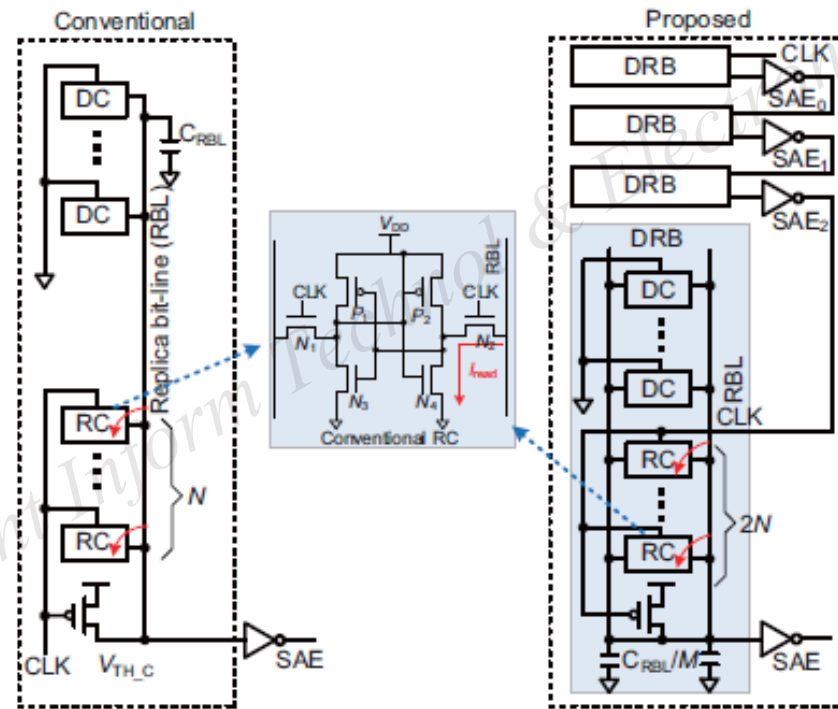


Fig. 5 Block diagram of the conventional RBL and proposed MDRBD circuits

# Relations of distribution of SAE timing variation among different techniques

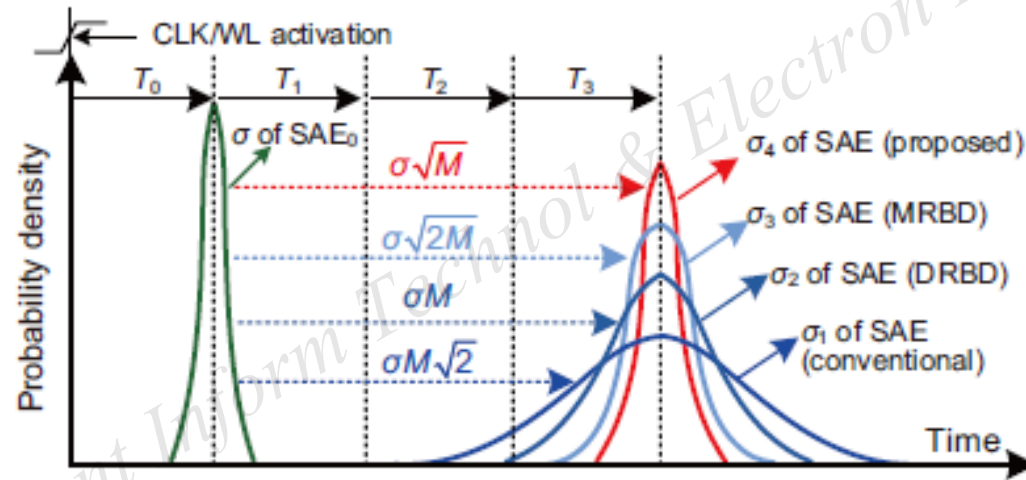


Fig. 6 Relations of distribution of the SAE timing among different techniques

# Simulation results comparison

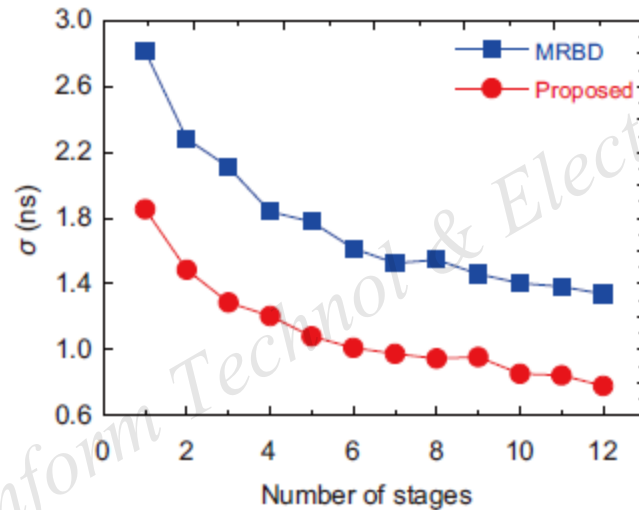


Fig. 7 Standard deviation of SAE timing with different numbers of stages, using MRBD and the proposed MDRBD technique, respectively (i.e., 0.8 V, SS,  $-40^{\circ}\text{C}$ ,  $N = 2$ )

# Simulation results comparison (Con'd)

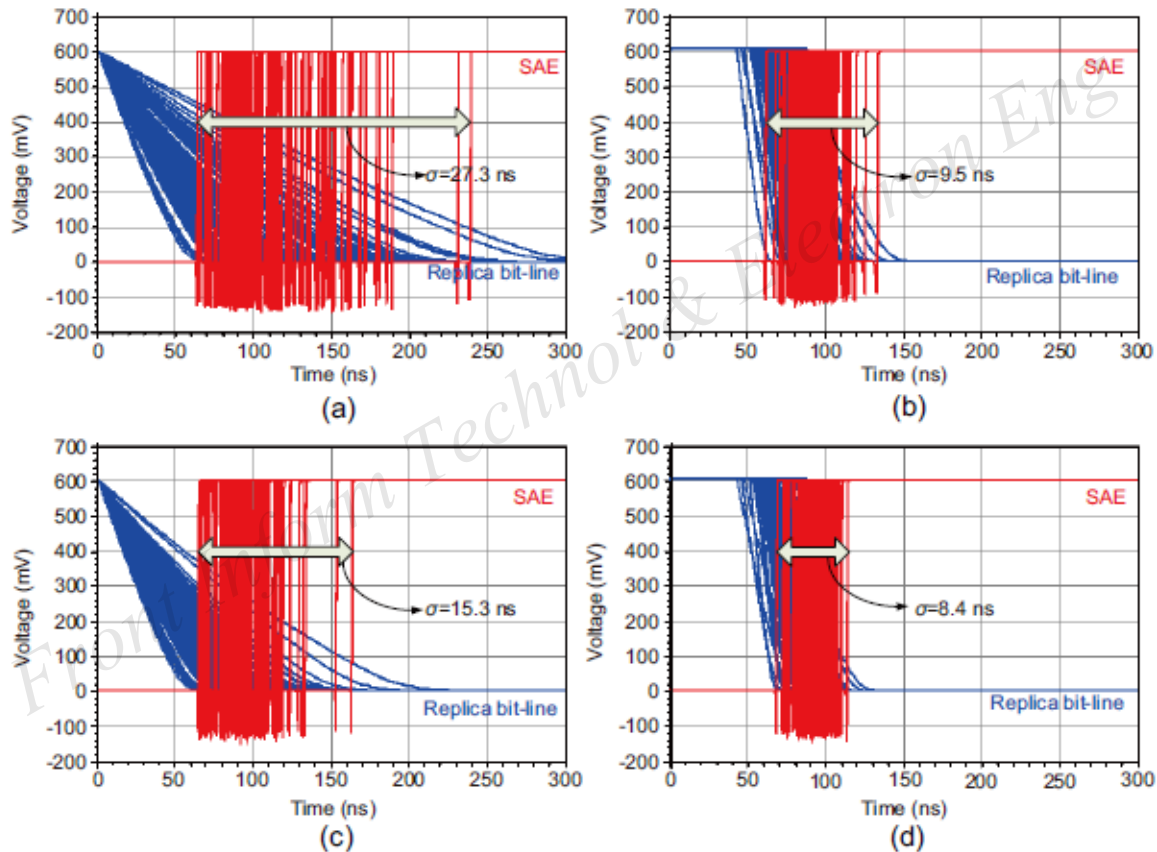


Fig. 8 Standard deviation comparison of SAE timing in the worst case (i.e., 0.6 V, SS, -40 °C): (a) conventional RBL; (b) MRBD; (c) DRBD; (d) proposed MDRBD

# Simulation results comparison (Con'd)

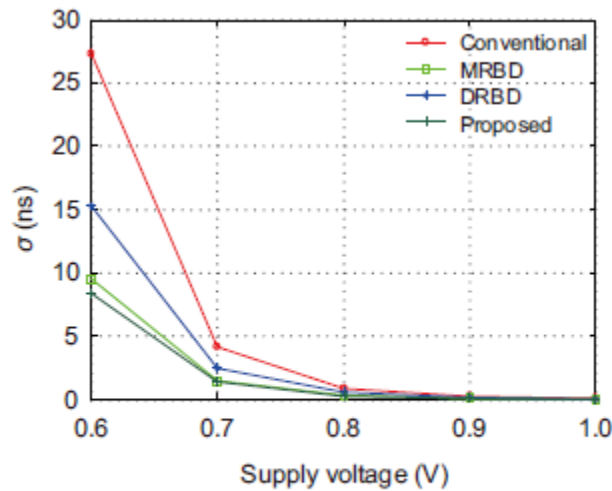


Fig. 9 Standard deviation comparison of SAE timing with different voltages (i.e., SS,  $-40^{\circ}\text{C}$ )

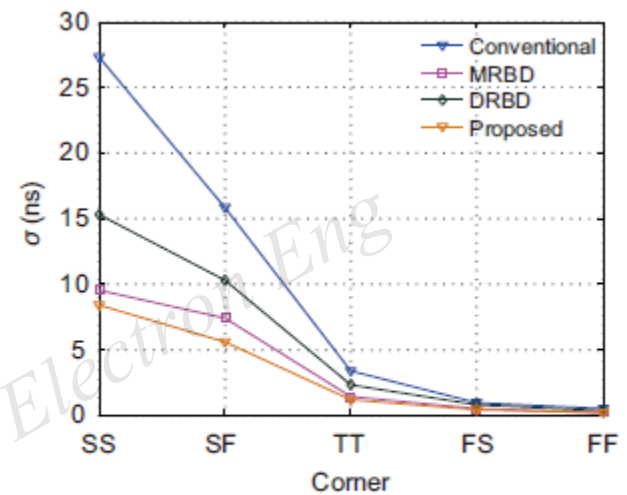


Fig. 10 Standard deviation comparison of SAE timing with different process corners (i.e.,  $0.6\text{ V}$ ,  $-40^{\circ}\text{C}$ )

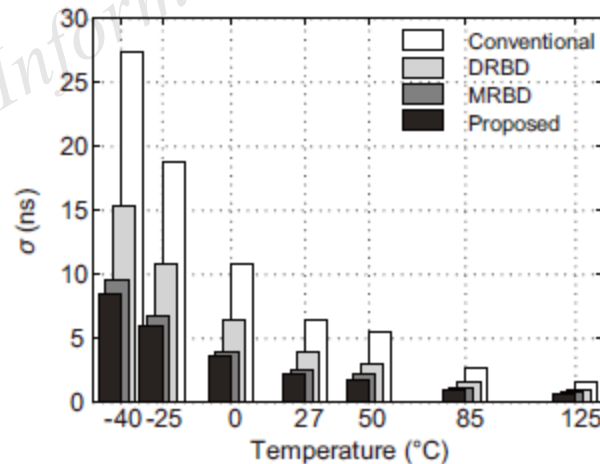


Fig. 11 Standard deviation comparison of SAE timing with different temperatures (i.e.,  $0.6\text{ V}$ , SS)

# Power and area comparison

**Table 2 Comparison of different timing strategies for SA (SS,  $-40\text{ }^{\circ}\text{C}$ )**

Strategy	Power consumption (nW)				Area overhead
	0.6 V	0.8 V	1.0 V	1.2 V	
Conventional	89.82	120.6	153.8	190.0	–
MRBD	98.70	133.6	170.9	210.1	Yes
DRBD	175.90	234.7	293.6	354.3	No
Proposed	185.20	247.7	310.8	375.5	Yes

# Conclusions

- By using multi-stage and dual replica bit-line, the proposed MDRBD technique, to some degree, decreases the mismatch between global RBL and normal bit-line owing to the gate delay of inverters.
- In the worst case, the standard deviation in the proposed design has decreased by 69.2% relative to that of the conventional scheme, and the cycle time has reduced by 47.2%.