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Schedule refinement for homogeneous multi-core processors in the presence of manufacturing-caused heterogeneity

Key words: Schedule refining, Multi-core processor, Heterogeneity, Representative chip operating point

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Introduction

- The unified maximum operating frequencies of all cores on the homogeneous processor makes the task scheduling simple but has a heavy performance penalty.

- To diminish the performance penalty, task scheduling has to take the heterogeneity into consideration.

- A heterogeneity aware schedule refining is proposed to efficiently exploit the manufacturing-caused heterogeneity to improve performance in this work.

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The impact of manufacturing-caused heterogeneity on performance

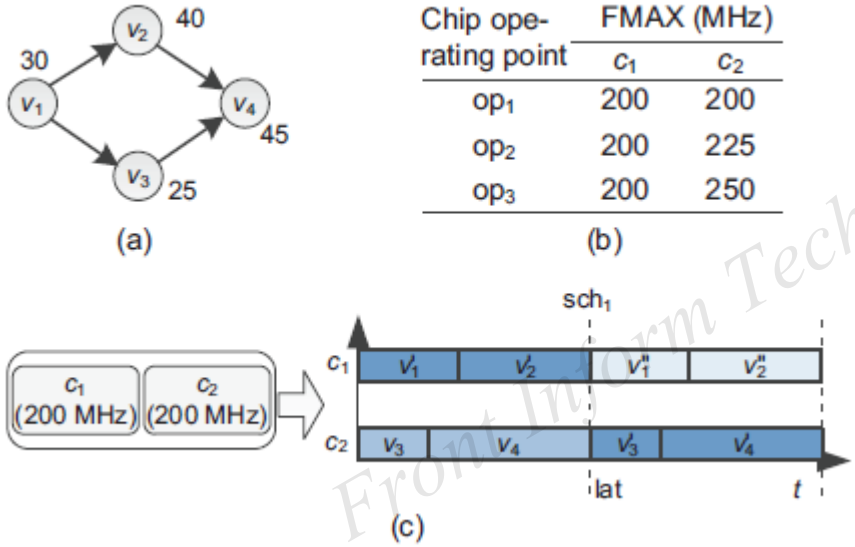

Fig. 1 A simple example: (a) an application with four tasks; (b) three chip operating points; (c) the traditional schedule; (d) traditional scheduling scheme

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Heterogeneity aware schedule refining scheme

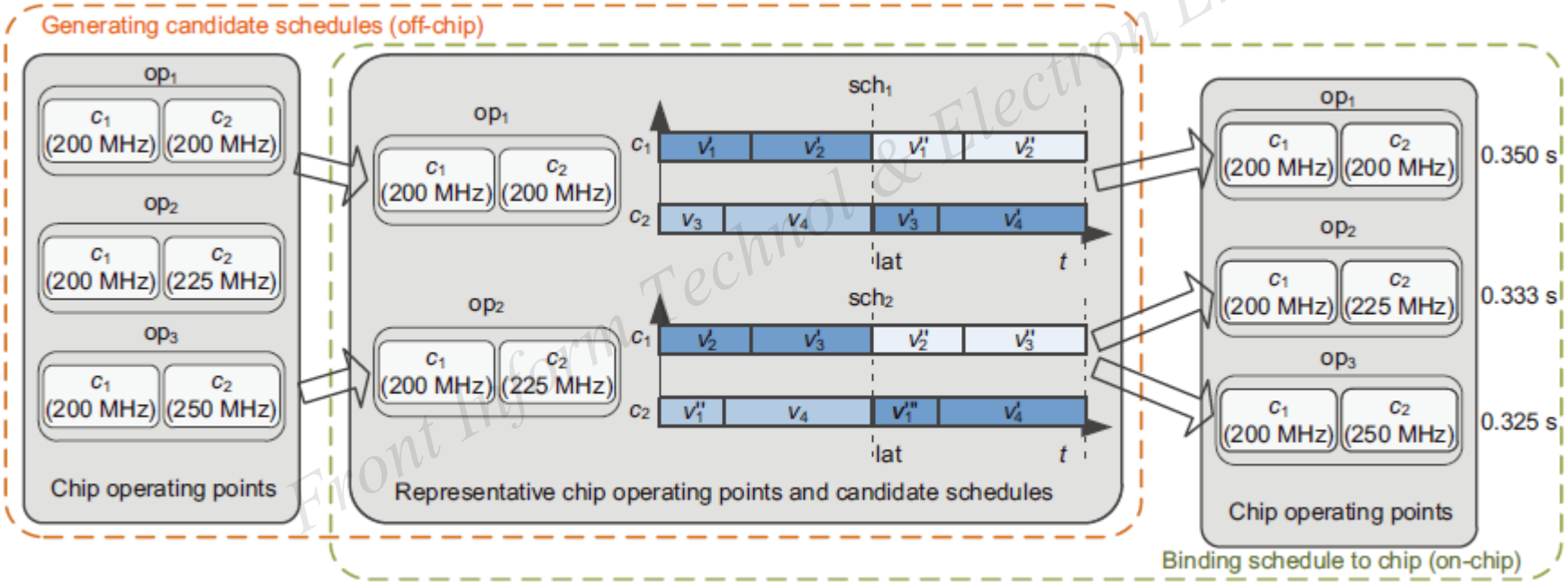

Fig. 3 Heterogeneity-aware schedule refining scheme for the task graph and processor in Fig. 1

CDF of chips over the performance improvement

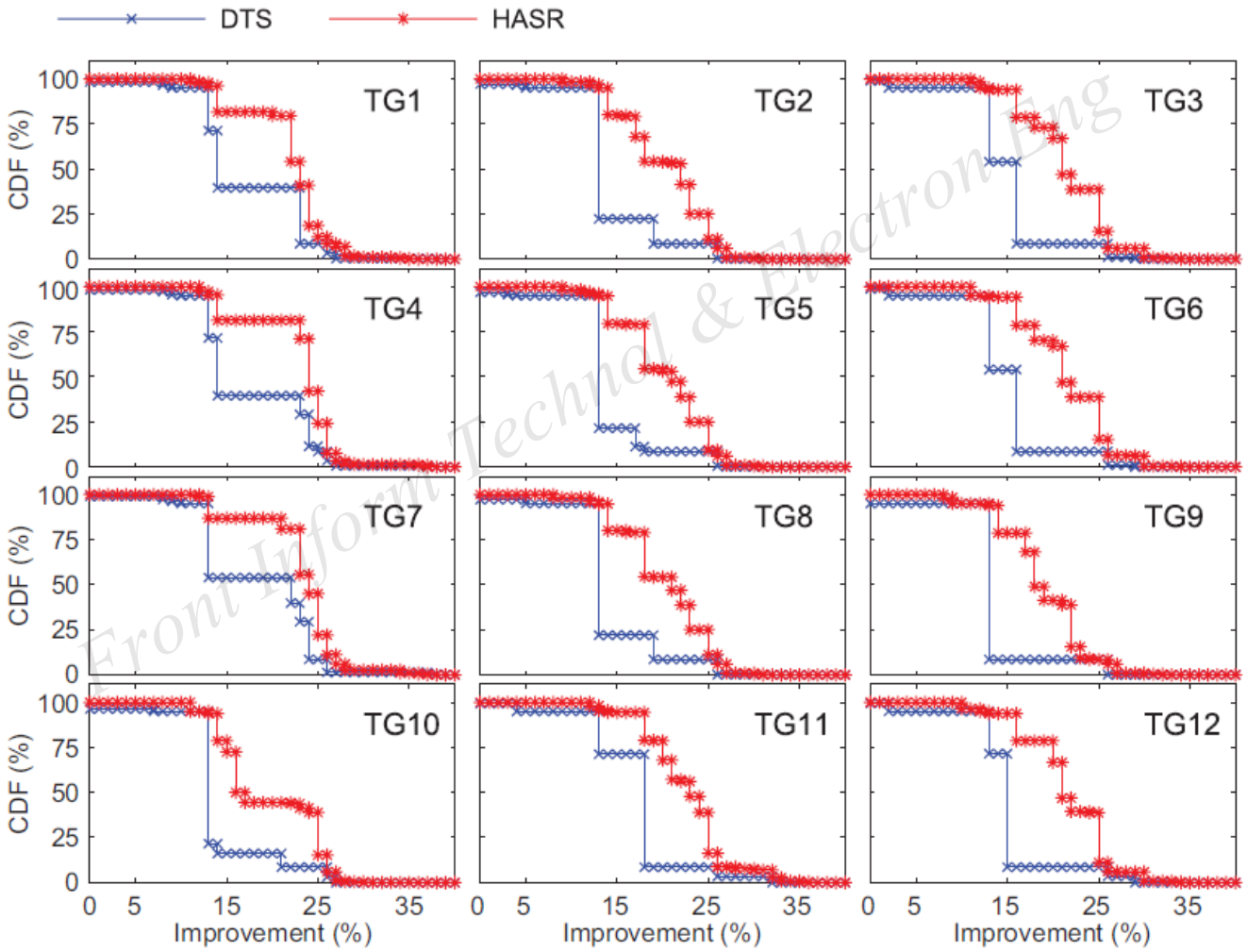

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Fig. 8 The CDF of chips over the improvement of results achieved by HASR and DTS against base performance for different applications

Probability density function of throughput improvement

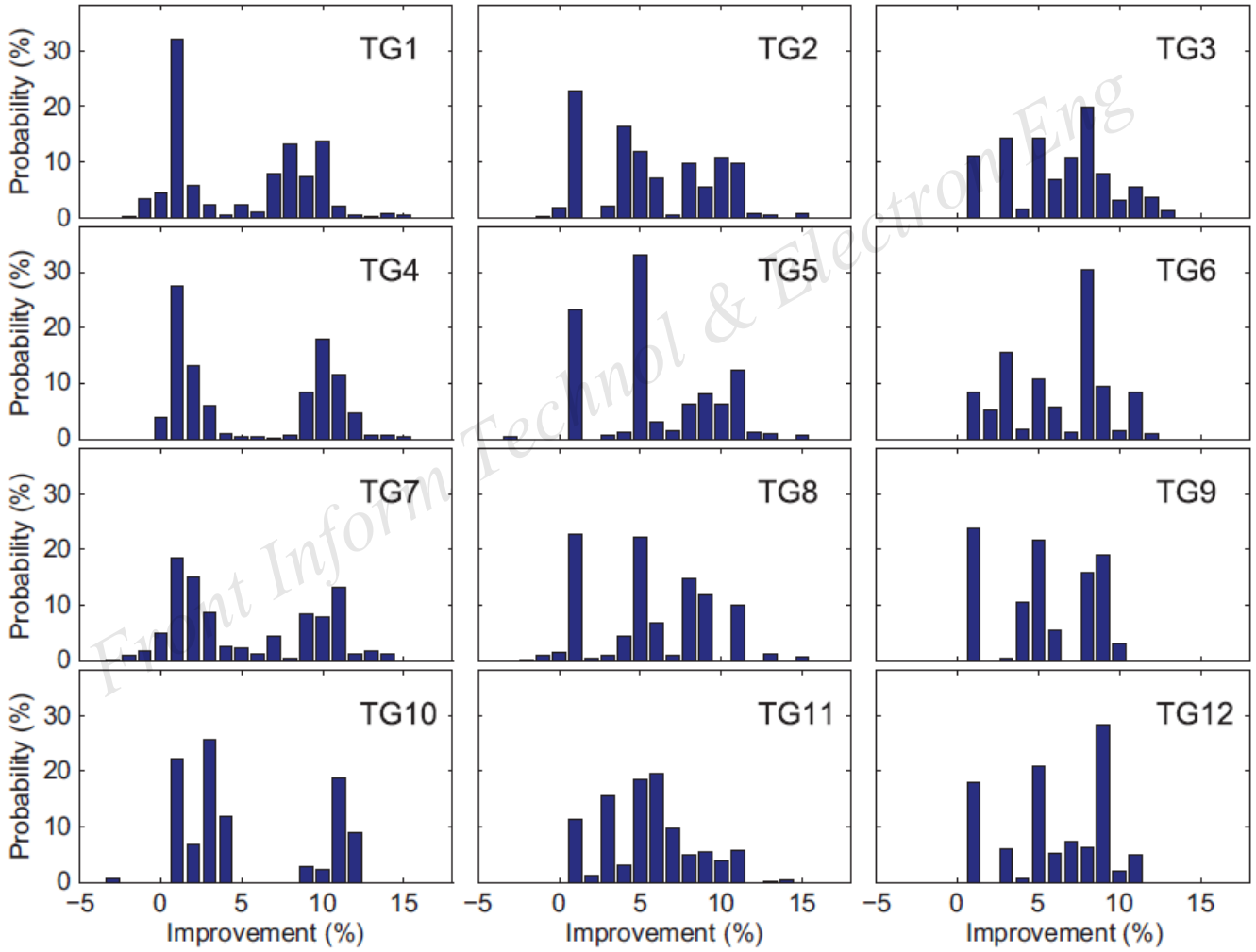

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Fig. 9 The probability density function of throughput improvement achieved by HASR against DTS on different applications

Throughput improvement over numbers of tasks and cores

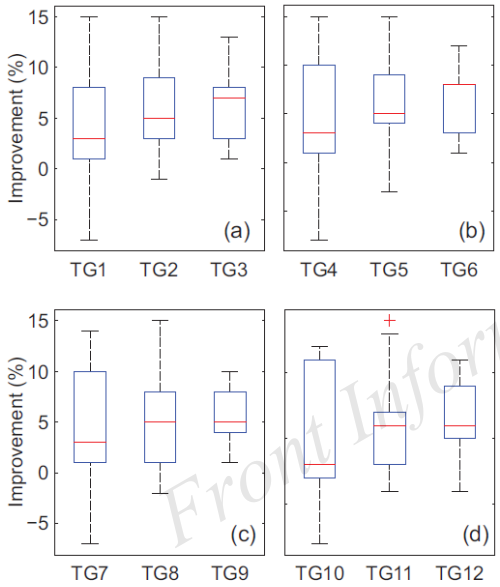

Fig. 10 The throughput improvement achieved by HASR against DTS on different applications

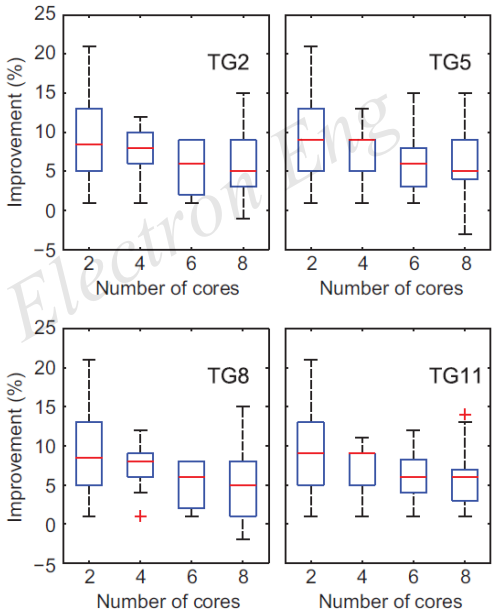

Fig. 11 The throughput improvement achieved by HASR against DTS on different multi-core processors for synthetic applications

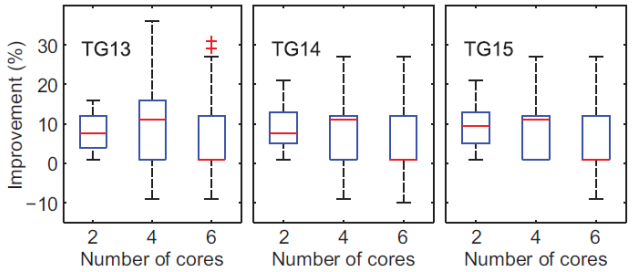

Fig. 12 The throughput improvement achieved by HASR against DTS on different multi-core processors for real applications

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CDF of chips over performance improvement

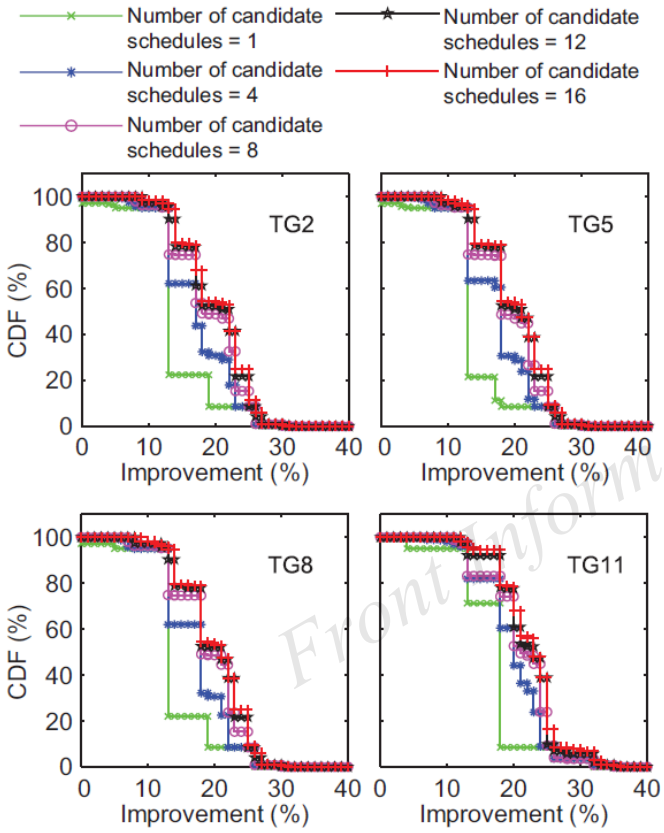

Fig. 13 The CDF of chips over the improvement of results achieved by HASR and DTS against base performance for synthetic applications with different quantities of candidate schedules

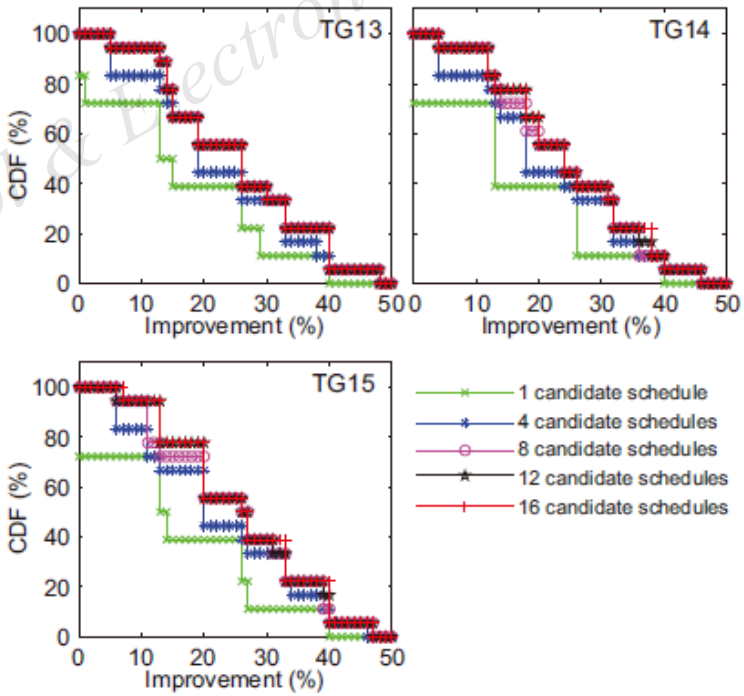

Fig. 14 The CDF of chips over the improvement of results achieved by HASR and DTS against base performance for real applications with different candidate schedule quantities

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Conclusions

- The heterogeneity aware schedule refining scheme constructs representative chip operating point set to generate candidate schedules and find the optimal schedule binding to improve performance.
- Experimental results show that HASR outperforms the traditional single schedule based approach.

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