Xin Li, Jin Sun, Fu Xiao, Jiang-shan Tian, 2016. An efficient bi-objective optimization framework for statistical chip-level yield analysis under parameter variations. *Frontiers of Information Technology and Electronic Engineering,* **17**(2):160-172. http://dx.doi.org/10.1631/FITEE.1500168

An efficient bi-objective optimization framework for statistical chip-Level yield analysis under parameter variations

Key words: Parameter variations, Parametric yield, Multi-objective optimization, Chebyshev affine, Adaptive weighted sum

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Introduction

- The correlation between leakage power and delay will consequently bring on a confliction during optimization procedure and cause designers to be in a dilemma.

- To deal with arbitrary correlations among PVT parameters and handle parameter variations partially specified, an effective parametric yield optimization approach must be developed.

- A novel bi-objective optimization framework under parameter variations has been presented in this work.

PLPB representation

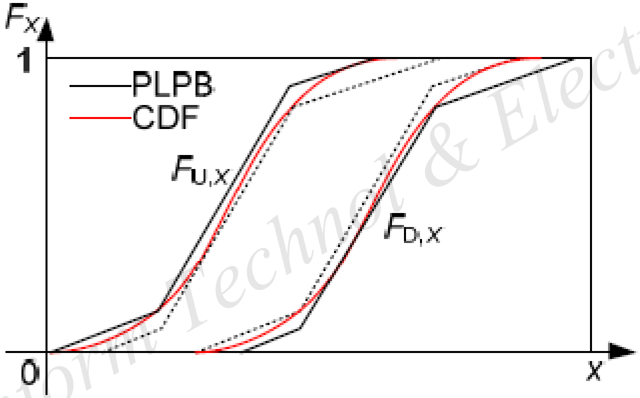

Fig. 1 Piecewise linear probability bounds (PLPB) representation of an uncertain random variable (the dotted lines are PLPB bounds, which are not focused on in this study)

Optimization procedures

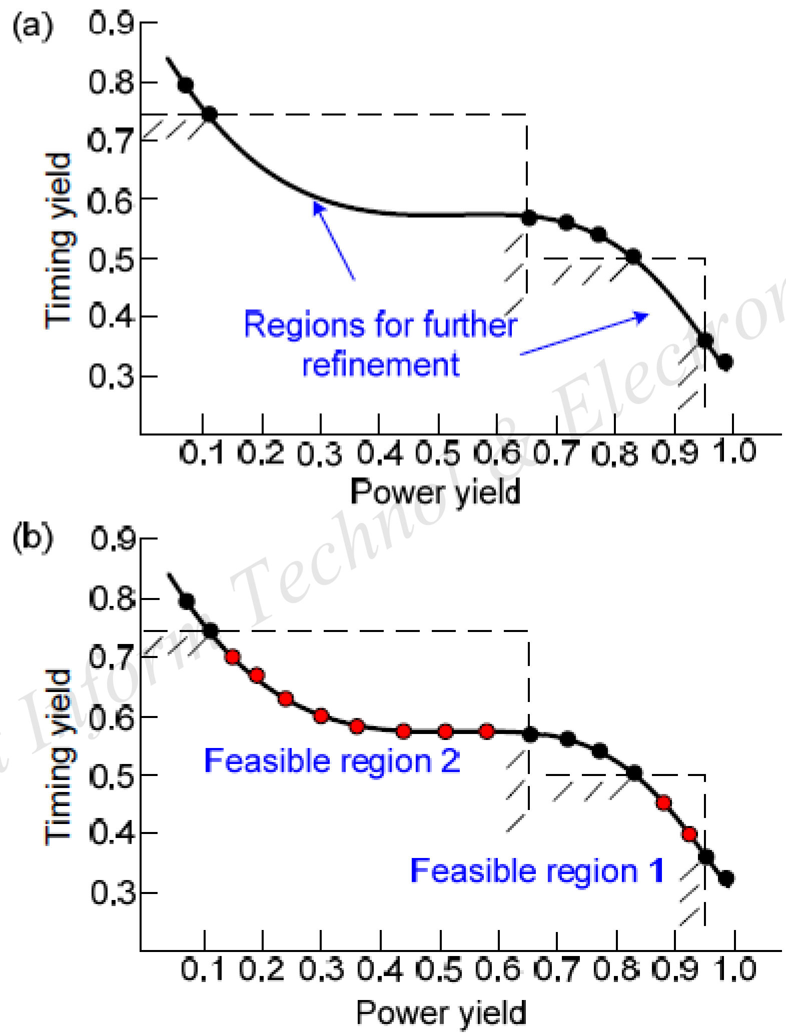

Fig. 6 First round solutions of optimization procedures (a) and second round refinement of optimization procedures (b)

Performance distribution

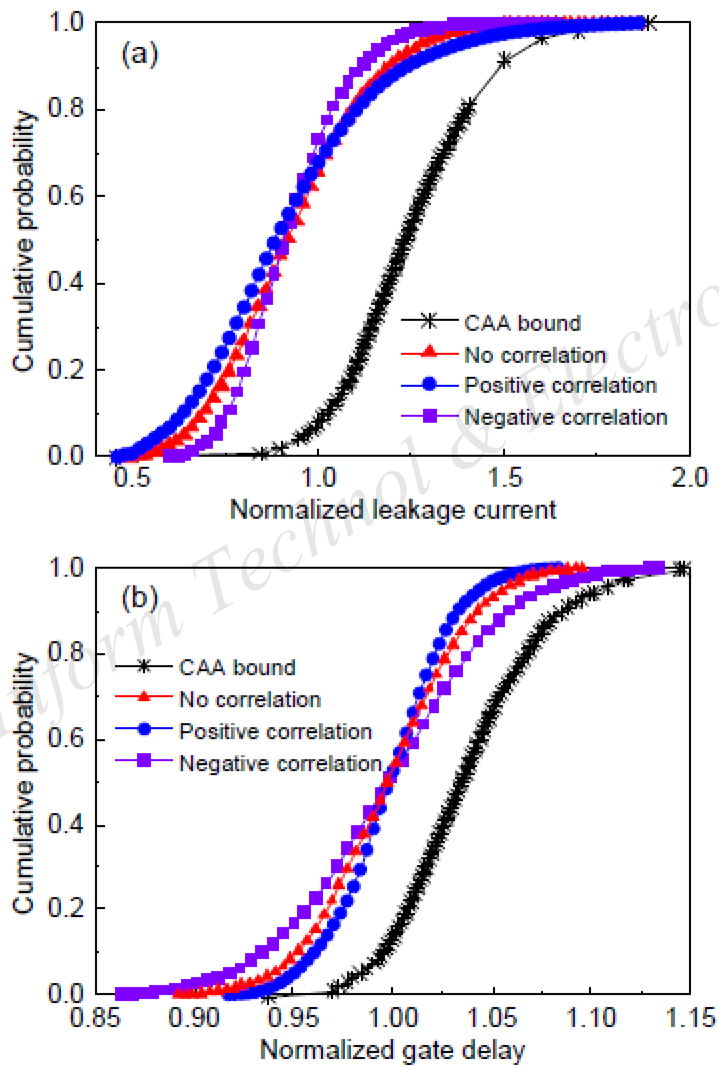

Fig. 7 Leakage power distributions (a) and gate delay distributions (b) for circuit C432

Optimization results (I)

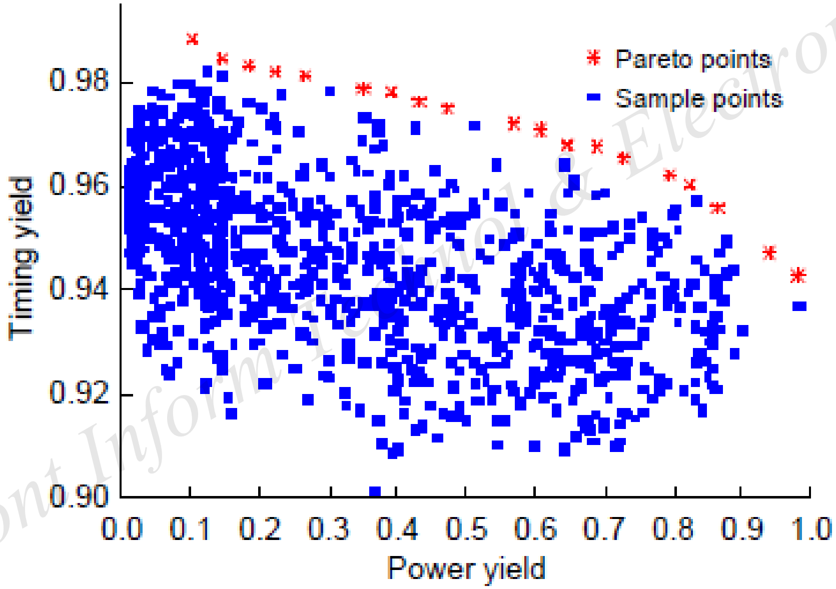

Fig. 8 Monte Carlo verification for circuit C432

Optimization results (II)

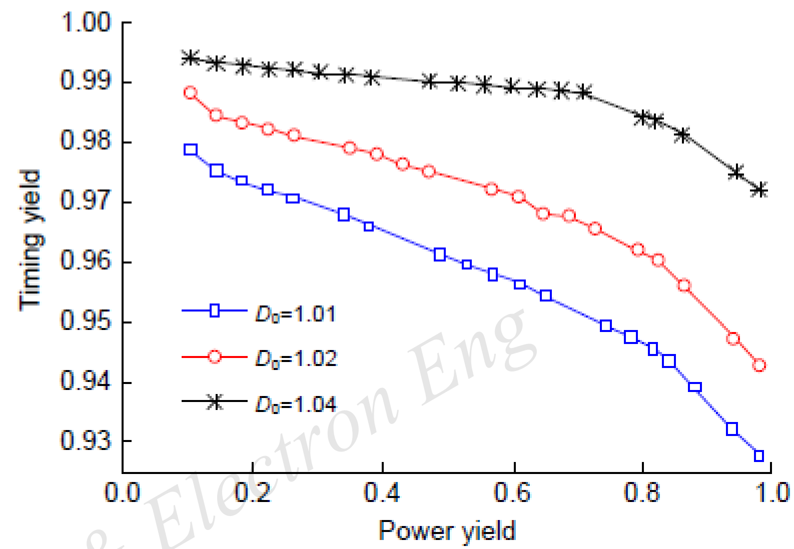

Fig. 10 The Pareto fronts for circuit C432 under different timing limits

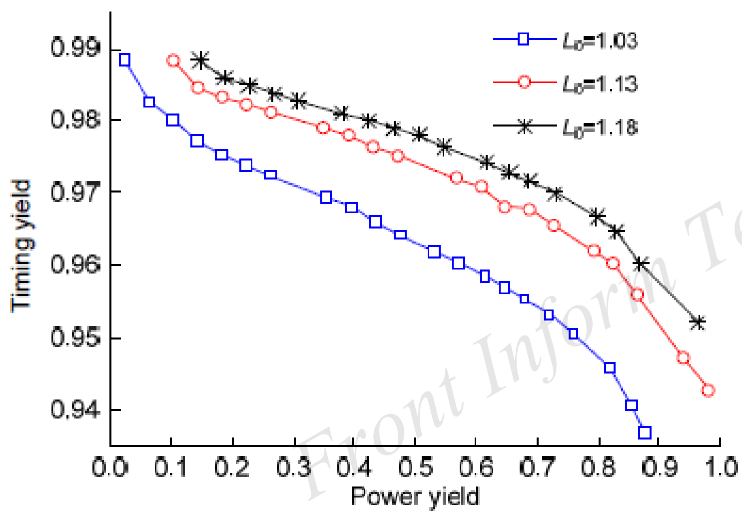

Fig. 9 The Pareto fronts for circuit C432 under different power limits

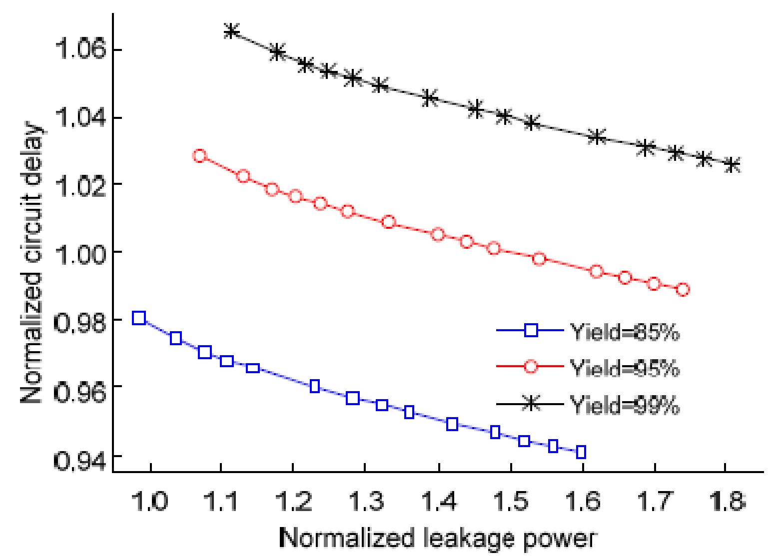

Fig. 11 Power-delay curves for circuit C432 at different yield levels

Pareto-optimal solutions (I)

Table 1 A few Pareto-optimal solutions obtained by AWS for parametric yield

Circuit name	Number of solutions	Power yield			Timing yield			Runtime (s)
		α=1.0	α=0.5	α=0	α=1.0	α=0.5	α=0	
C432	21	0.9947	0.8176	0.1037	0.9370	0.9608	0.9883	41
C499	21	0.9947	0.8200	0.1037	0.9209	0.9479	0.9797	37
C880	18	0.9947	0.6987	0.0180	0.9568	0.9788	0.9844	81
C1335	20	0.9940	0.8171	0.1034	0.9474	0.9688	0.9893	85
C1908	23	0.9943	0.8507	0.0182	0.9054	0.9161	0.9446	106
C2670	20	0.9942	0.8200	0.0179	0.9326	0.9554	0.9672	148
C3540	22	0.9947	0.8199	0.1037	0.9369	0.9595	0.9506	201
C5315	23	0.9947	0.1037	0.0181	0.9163	0.9709	0.8741	253
C6288	23	0.9946	0.1037	0.0179	0.9283	0.9652	0.9611	361
C7552	21	0.9947	0.1036	0.0181	0.9359	0.9850	0.9707	373

Pareto-optimal solutions (II)

Table 2 A few Pareto-optimal solutions obtained by AWS for yield percentile

Circuit name	Number of solutions	Leakage (95%)			Delay (95%)			Runtime (s)
		α=1.0	α=0.5	α=0	α=1.0	α=0.5	α=0	
C432	15	1.071	1.262	1.740	1.029	1.072	0.989	41
C499	15	1.070	1.197	1.738	1.039	1.025	0.998	37
C880	14	1.070	1.355	1.739	1.015	0.997	0.979	81
C1335	14	1.071	1.479	1.740	1.022	0.996	0.985	85
C1908	15	1.070	1.245	1.739	1.047	1.033	1.008	106
C2670	15	1.069	1.240	1.739	1.031	1.017	0.994	148
C3540	15	1.070	1.257	1.740	1.029	1.014	0.991	201
C5315	15	1.070	1.264	1.740	1.043	1.028	1.005	253
C6288	15	1.070	1.428	1.739	1.040	1.019	1.005	361
C7552	14	1.071	1.254	1.740	1.030	1.015	0.991	373

Conclusions

- A novel power-delay bi-objective optimization methodology for statistical yield optimization is proposed. Regarding both power and timing yield as objective functions, an efficient bi-objective optimization framework is suggested to optimize these two goals simultaneously under PVT parameter variations.
- The proposed algorithm was verified using ISCAS benchmark circuits, demonstrating its efficiency.