Wei Zhang, You-de Hu, Li-rong Zheng, 2016. Design and simulation of a standing wave oscillator based PLL. *Frontiers of Information Technology & Electronic Engineering*, **17**(3):258-264.
http://dx.doi.org/10.1631/FITEE.1500210

Design and simulation of a standing wave oscillator based PLL

Key words: Standing wave oscillator, Clock distribution, Phase locked loop, Varactor

Contact: Wei Zhang
E-mail: wei_zhang@fudan.edu.cn
ORCID: http://orcid.org/0000-0001-8427-3724

Introduction

- While using the technology of SWO in chip design, the frequency tuning problem should be resolved.
- Different distribution architectures of varactors have different frequency tuning ranges and power consumptions.
- An SWO based PLL has been presented in this work.
- Proposed usage of this new PLL is introduced in this work.

Two types of SWO frequency tuning architecture in this work

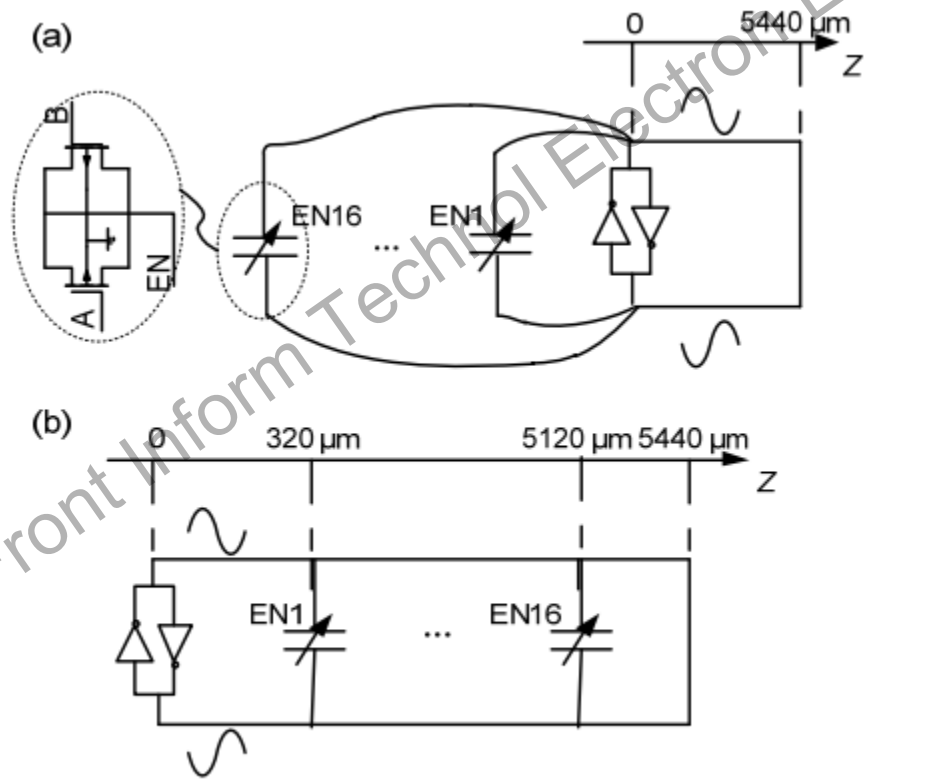


Fig. 4 Lumped varactor's architecture (a) and distributed varactor's architecture (b)

Simulation results of two tuning architectures

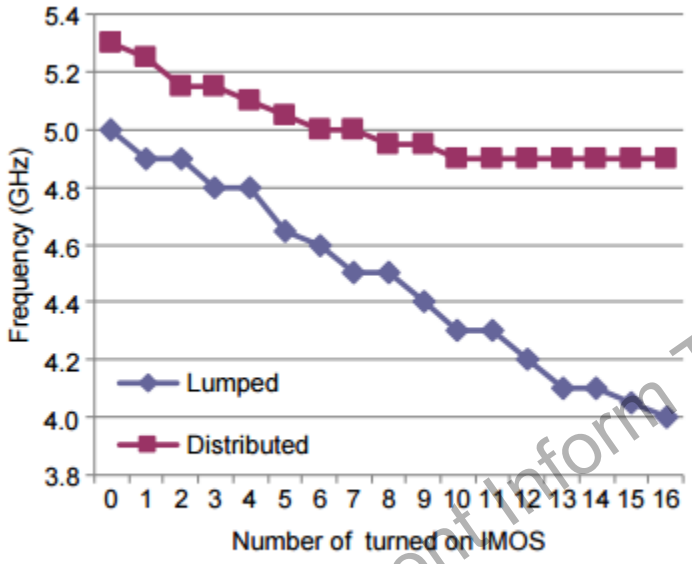


Fig. 5 Frequency tuning results of the lumped and distributed varactor's architecture

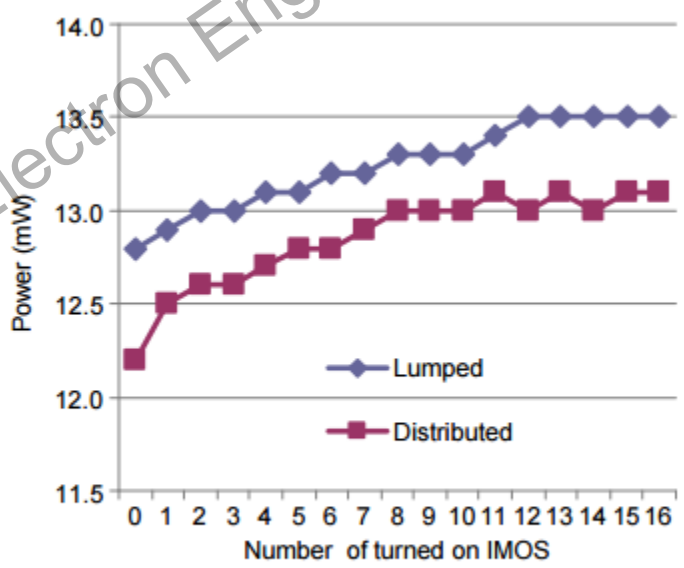


Fig. 6 Power consumptions of the lumped and distributed varactor's architecture

SWO based PLL

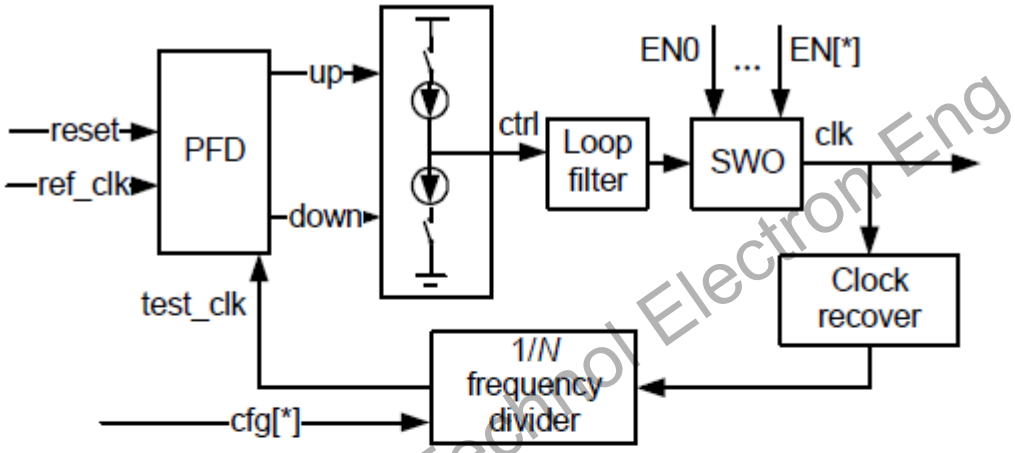


Fig. 7 SWO based PLL architecture

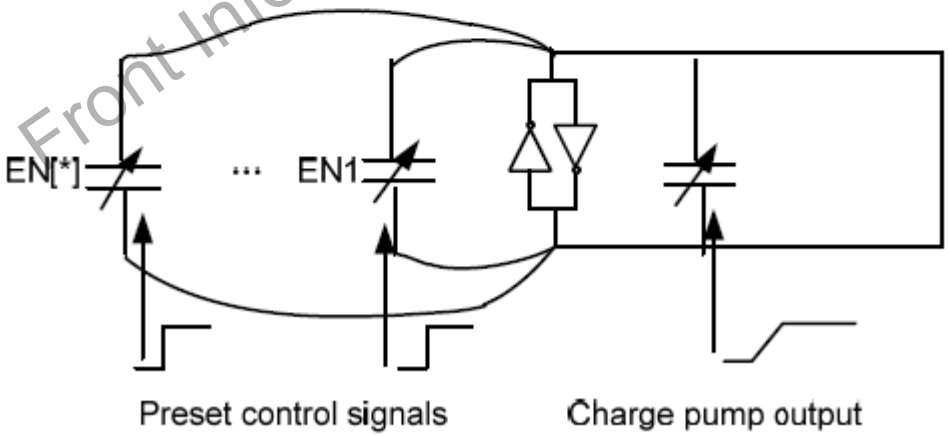


Fig. 8 Lumped varactors used in PLL

PLL working process

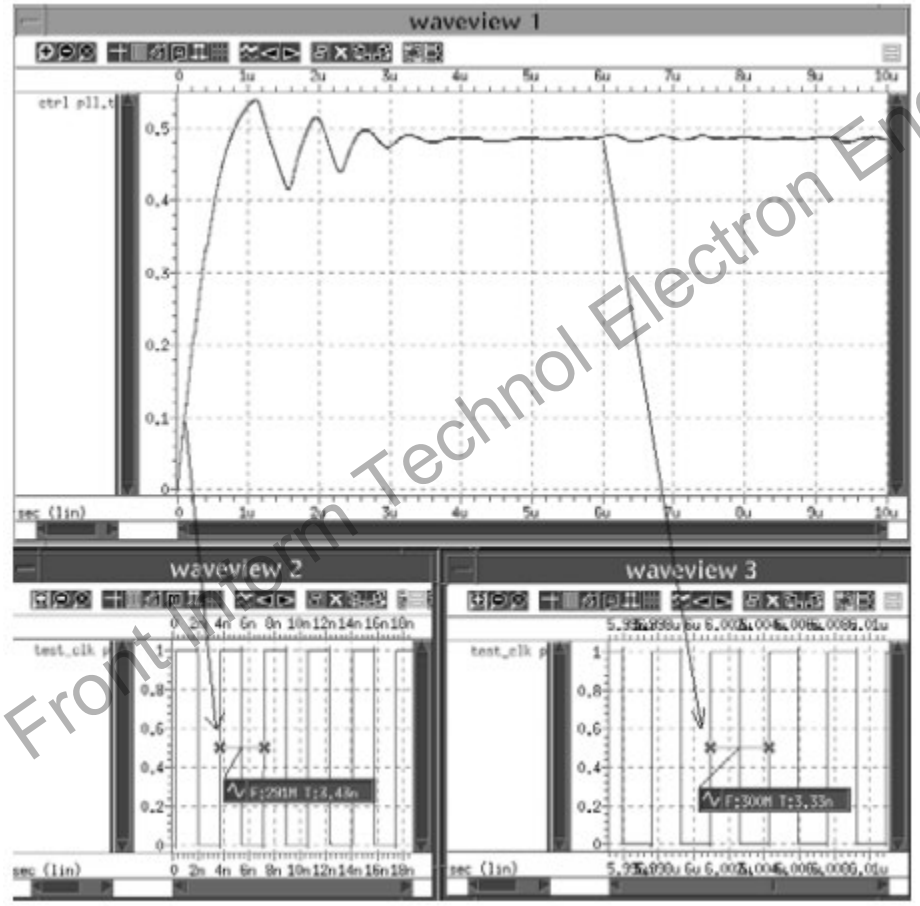


Fig. 9 Locking process of a SWO-based PLL

Usage of SWO based PLL

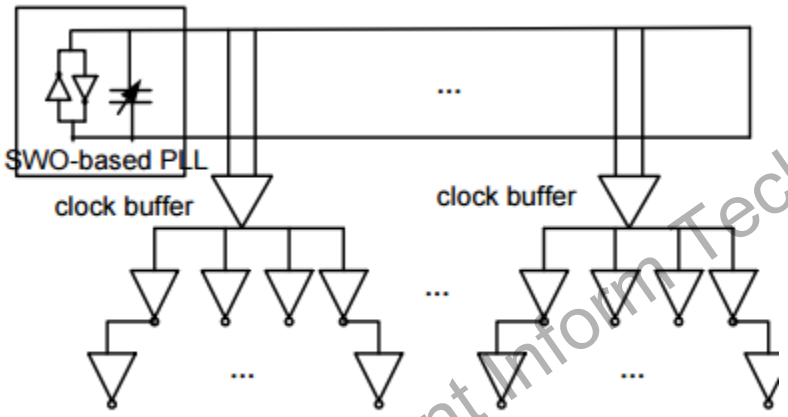
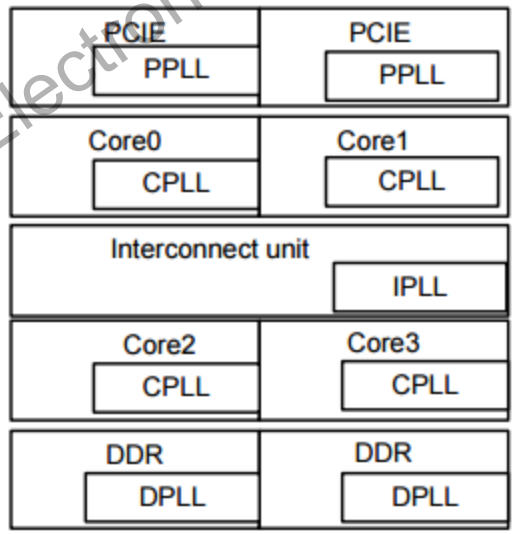


Fig. 10 SWO-based PLL with clock buffer loads



Conclusions

- The lumped varactor's architecture achieves wider tuning range than distributed varactor's architecture with more power consumption.
- The new SWO based PLL achieves over a 50% frequency tuning range, and can be used directly in globally asynchronous locally synchronous chips.