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Design and analysis of carbon nanotube FET-based quaternary full adders

Key words: Nanoelectronics, Carbon nanotube FET, Multiple-Valued Logic, Quaternary Logic

Corresponding author: Mohammad Hossein Moaiyeri
E-mail: h_moaiyeri@sbu.ac.ir

ORCID: http://orcid.org/0000-0001-9711-7923

Motivation

- Space limitation for interconnections and short channel effects of the scaled Complementary Metal Oxide Semiconductor (CMOS) for binary logic leads to serious challenges.
- Use of unique properties of carbon nanotube transistors and multi-valued logic can be very advantageous in solving the limitations of scaling.
- Quaternary is the closest radix to the optimum radix (e), which has the advantage of easier communication with binary logic circuits.

Main idea

- Our proposed methods are based on cascaded quaternary half adders presented by Moaiyeri *et al*. (2012) and a carry generation unit, which significantly improves the number of transistors and performance parameters.

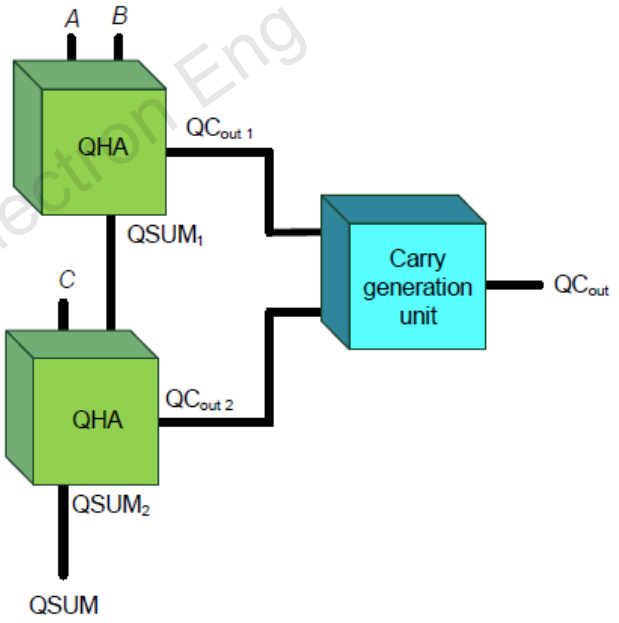

Fig. 2 The block diagram of the proposed quaternary full adder

Method

- The first proposed method has a structure based on two CNTFET binary inverters with a 0.6 V power supply, cascaded in two parallel paths.

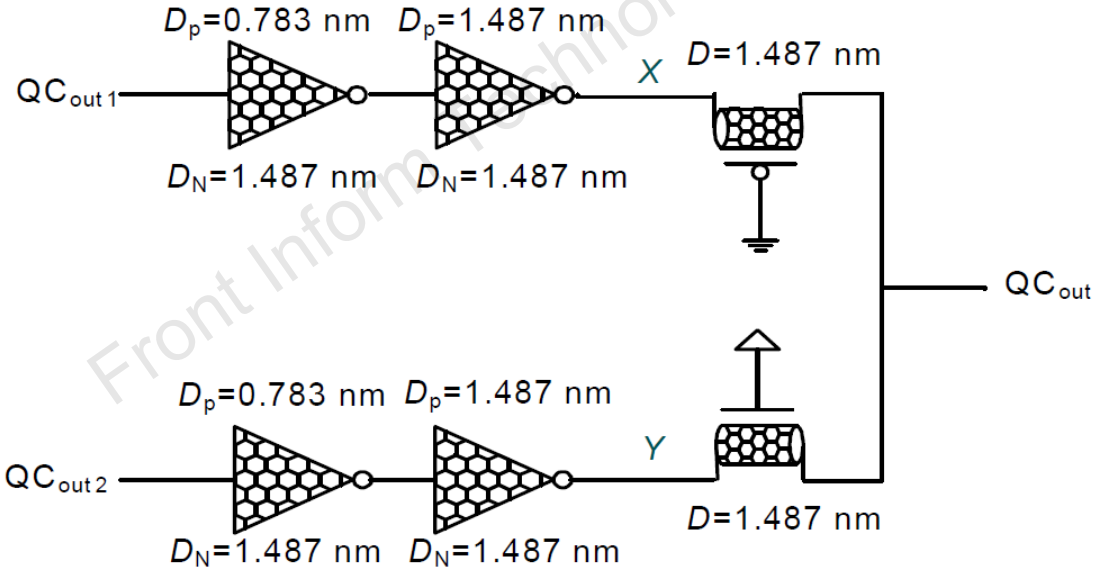

Fig. 3 The first proposed carry generation unit

Method (Cont'd)

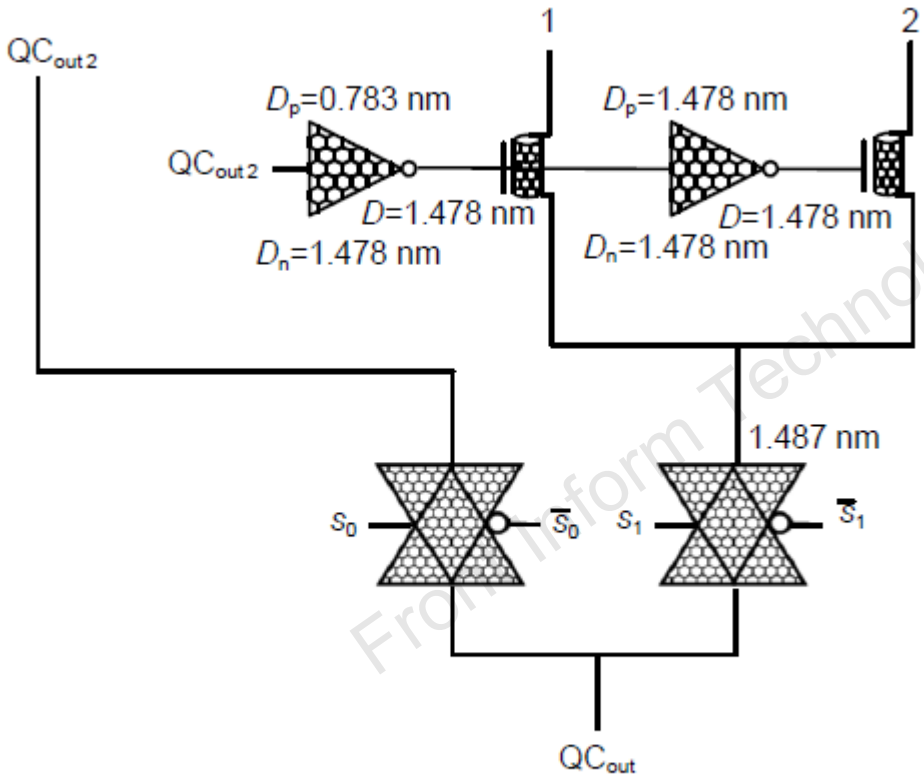

Fig. 4 The second proposed carry generation unit

- The second proposed method is based on an efficient design consisting of a CNTFET-based decoder, transmission gates, threshold detectors, and standard inverters.

Major results

- The proposed designs had on average 32% lower delay, 68% average power, 83% energy consumption, and 77% static power compared to state-of-the-art quaternary full adders.
- Simulation results indicated that the proposed designs are robust against process, voltage, and temperature variations, and are noise tolerant.

Table 3 Performance comparison of the quaternary adders (QFAs)

Design	Delay (ps)	Power (μW)	Energy (aJ)	Static power (μW)	Number of devices
The first proposed QFA	78.1	8.54	667	3.86	190
The second proposed QFA	85.9	7.67	658	3.51	200
The QFA of da Silva *et al.* (2006)	193.3	13.70	2646	8.51	320
The QFA based on Asif and Vesterbacka (2012)	173.1	37.87	6557	22.48	160
The QFA of Sharifi *et al.* (2015)	71.4	57.73	4125	41.57	154

Conclusions

- Two new CNTFET based quaternary full adder cells are proposed.
- We implemented the method using the outstanding properties of CNTFETs, which makes the design of MVL circuits easier and more efficient as compared to using MOSFETs.
- We demonstrated the higher performance of the proposed designs through a series of simulations using a HSPICE simulator with the Stanford CNTFET model at 32 nm technology.
- The results confirmed the higher robustness of the proposed designs in terms of noise margin, and sensitivity to process, voltage, and temperature variations.