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Power-efficient dual-edge implicit pulse-triggered Flip-Flop with an embedded clock-gating scheme

Key words: Low power, Flip-flop, Implicit, Clock-gating scheme, Dual-edge

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Motivation

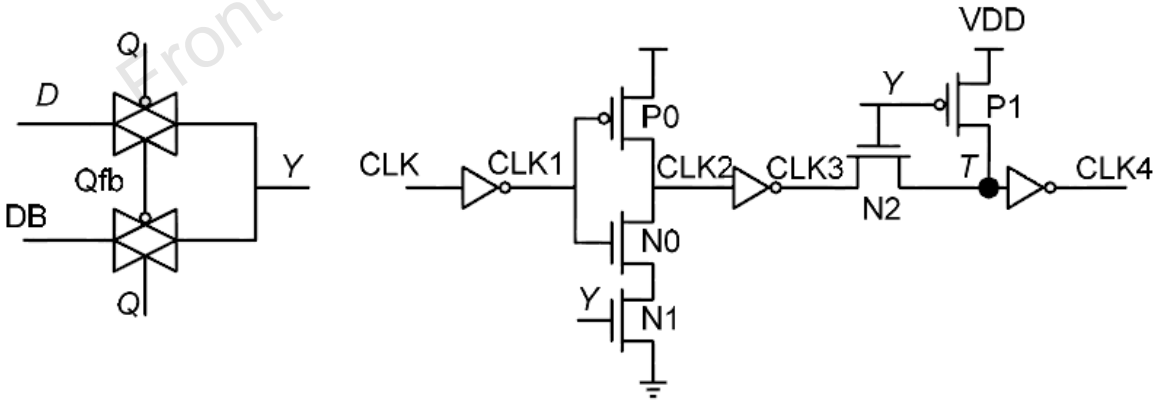
- The power dissipation of clock system that comprises clock distribution network and flip-flops (FFs), accounts for 30% to 60% of the overall system power.
- A wide section of technologies have been proposed to improve the performance of FFs.
- Pulse-triggered flip-flops (P-FFs) gain more popularity over the conventional transmission gate (TG) and master-slave based FFs in high-speed and low-power applications.
- A more power-efficient dual-edge implicit P-FF with an embedded clock-gating scheme (DIFF-CGS) is proposed and discussed in this paper.

Main idea

- Switching power consumption is one of the primary components of the total power consumption in complementary metal–oxide–semiconductor (CMOS) circuits, and is caused by charging and discharging the load capacitances when the signal of node makes a transition between low and high level.
- when the input data of FF keeps unchanged, it is not necessary to provide clock signal to the FF, and blocking the redundant clocked signals and eliminate the redundant transitions of internal nodes can decrease the power of FF.

Method

- The embedded clock gating scheme is employed to conditionally disables the inverter chain to block the redundant delayed clocked signals and eliminate the redundant transitions of internal nodes when the input data keeps unchanged.
- The specific clock gating scheme is implemented by embedding a control circuit in the adaptive clocking inverter chain, which employs a TGL-based comparator to avoid threshold voltage degradation problem.



Proposed Scheme

- The implicit pulse generation stage with an embedded clock-gating scheme and the static latching stage.

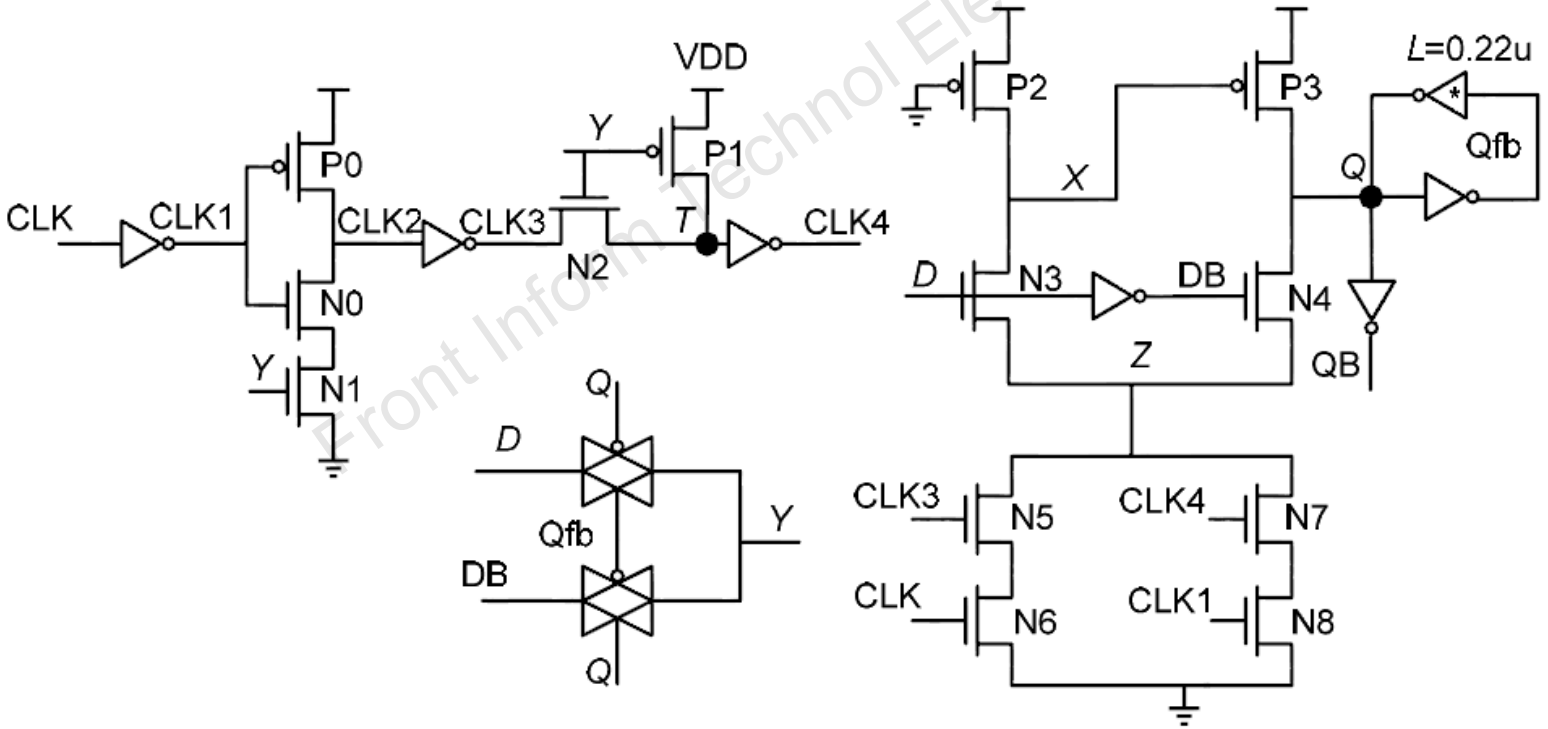


Fig. 8 Dual-edge implicit flip-flop with an embedded clock-gating scheme

Major results (1)

- The snapshots of the transient waveforms for DIFF-CGS, which demonstrates that the proposed design has correct logic functionality and redundant pulses are suppressed.

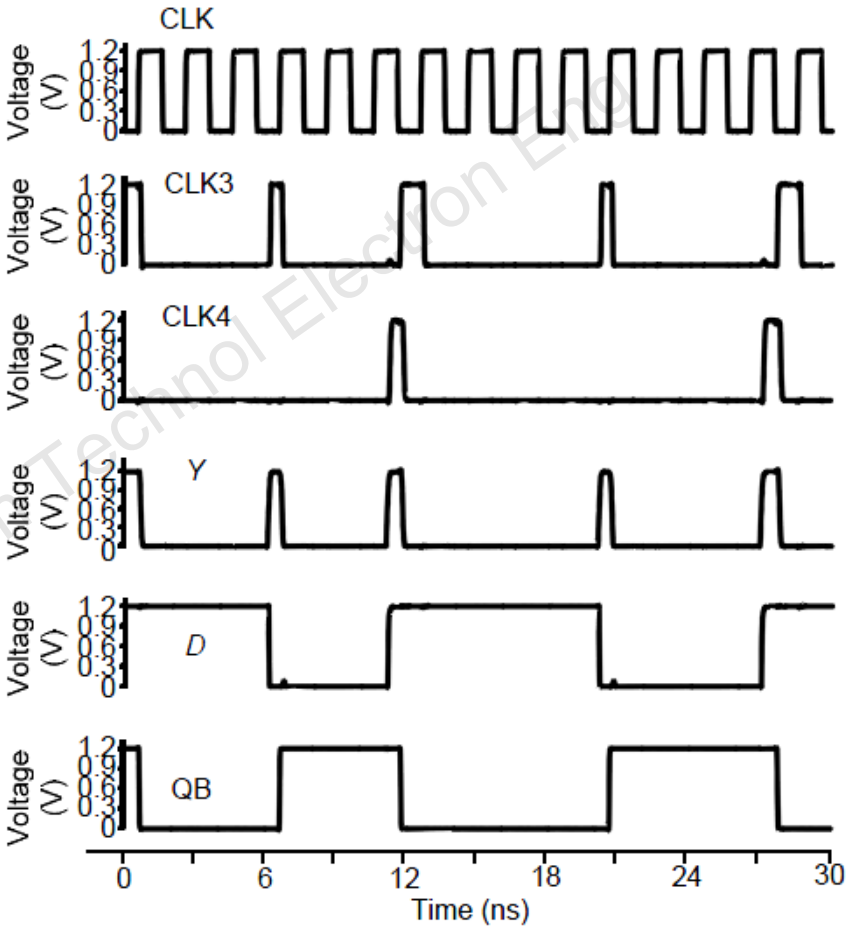


Fig. 10 Transient waveforms of dual-edge implicit flip-flop with an embedded clock-gating scheme

Major results (2)

- Comparison of various designs

Table 1 Comparison of various flip-flop designs*

Parameter	Value			
	SDETFF	CDFF	CPEFF	DIFF-CGS
Number of transistors	18	30	19	31
Layout area (μm^2)	31.57	42.33	30.93	37.86
Setup time	−128.27	−126.07	−51.46	78.67
Hold time	217.39	186.51	174.45	180.39
Minimum *D*-QB delay (ps)	167.30	191.80	181.39	292.12
CLK driving power (μW)	5.927	3.420	7.414	1.433
Data driving power (μW)	0.171	0.099	0.135	0.425
Latching power (μW)	9.048	12.626	4.513	5.211
Total average power (μW)	15.146	16.145	12.062	7.069
PDP (fJ)	2.534	3.097	2.188	2.065

* Power dissipation is measured when the data-switching activity is 10%. SDETFF: static dual edge-triggered flip-flop; CDFF: conditional discharge flip-flop; CPEFF: conditional pulse-enhancement flip-flop; DIFF-CGS: dual-edge implicit flip-flop with an embedded clock-gating scheme. PDP: power-delay product

Major results (3)

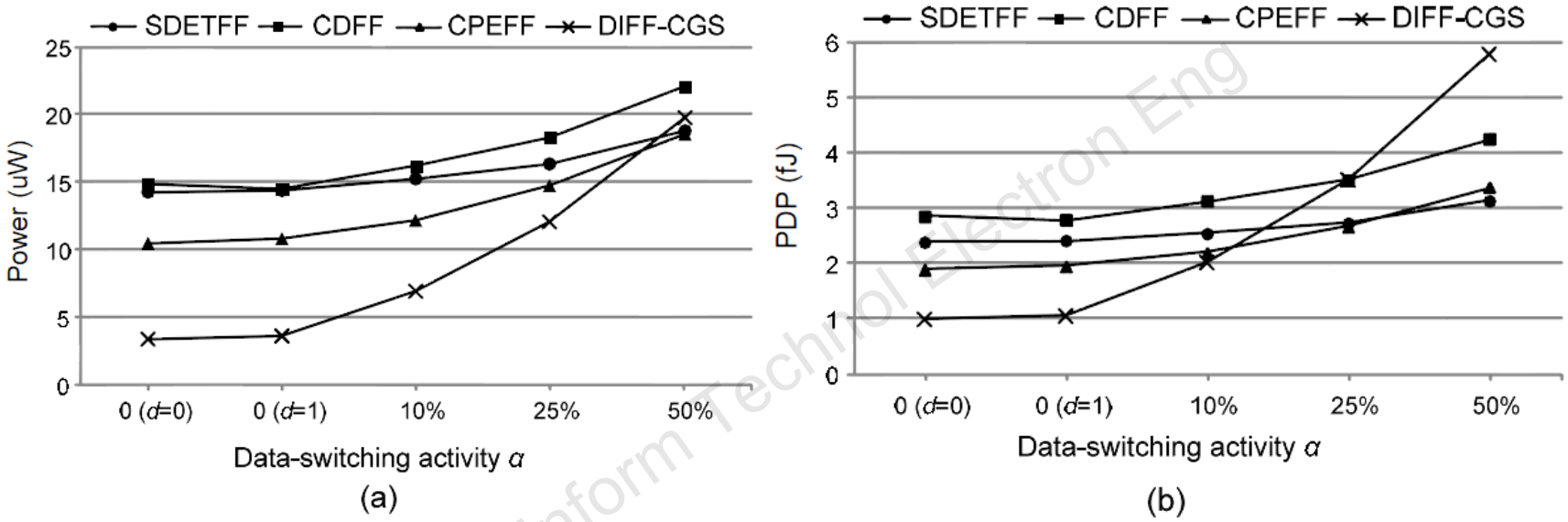


Fig. 12 Different data-switching activities: (a) power dissipation; (b) PDP performance

SDETFF: static dual edge-triggered flip-flop; CDFF: conditional discharge flip-flop; CPEFF: conditional pulse enhancement flip-flop; DIFF-CGS: dual-edge implicit flip-flop with an embedded clock-gating scheme

Major results (4)

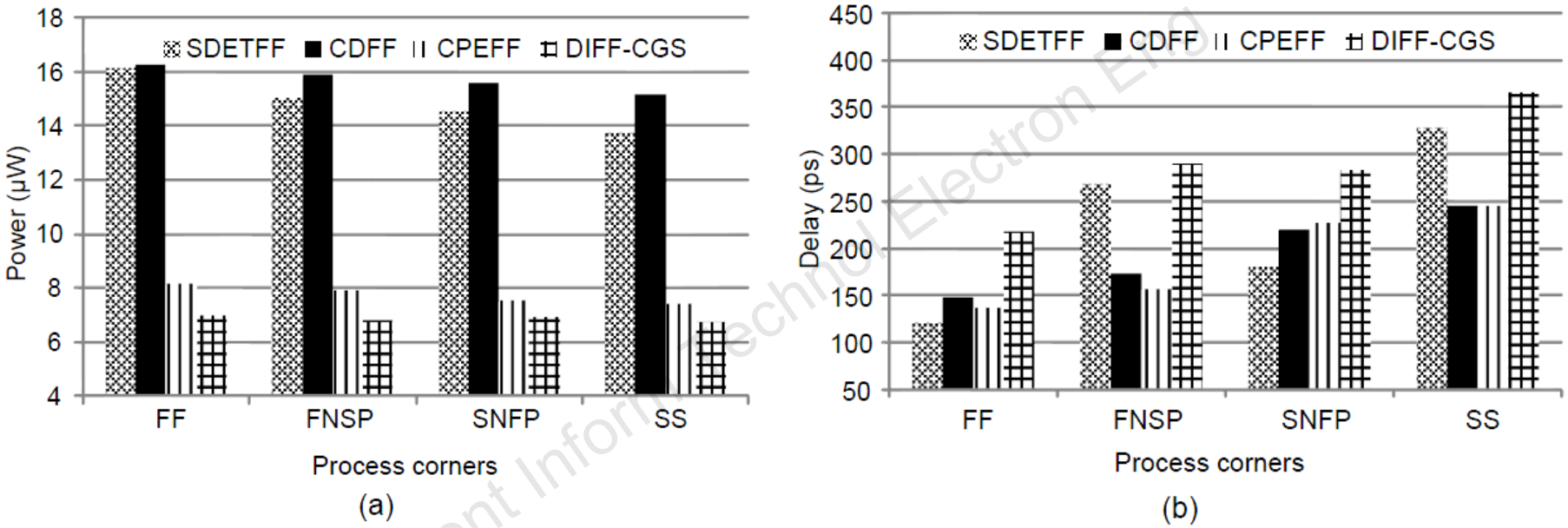


Fig. 13 Different process corners: (a) power dissipation; (b) delay

SDETFF: static dual edge-triggered flip-flop; CDFF: conditional discharge flip-flop; CPEFF: conditional pulse enhancement flip-flop; DIFF-CGS: dual-edge implicit flip-flop with an embedded clock-gating scheme

Major results (5)

- Monte-Carlo simulation results of power and delay.

Table 3 Power analysis of process–voltage–temperature variability through Monte-Carlo simulations*

Design	Mean power (μW)			Standard deviation (nW)		
	1.3 V, −40 °C	1.2 V, 25 °C	1.1 V, 125 °C	1.3 V, −40 °C	1.2 V, 25 °C	1.1 V, 125 °C
SDETFF	17.443	15.153	13.078	190.37	195.37	224.60
CDFF	18.694	16.158	13.667	87.47	77.80	83.26
CPEFF	14.223	11.998	9.536	104.77	78.46	94.98
DIFF-CGS	8.270	7.044	5.999	44.91	38.62	32.01

* The power parameters are measured when the input switching activity is 10%. SDETFF: static dual edge-triggered flip-flop; CDFF: conditional discharge flip-flop; CPEFF: conditional pulse-enhancement flip-flop; DIFF-CGS: dual-edge implicit flip-flop with an embedded clock-gating scheme

Table 4 Delay analysis of process–voltage–temperature variability through Monte-Carlo simulations*

Design	Mean *D*-QB delay (ps)			Standard deviation (nW)		
	1.3 V, −40 °C	1.2 V, 25 °C	1.1 V, 125 °C	1.3 V, −40 °C	1.2 V, 25 °C	1.1 V, 125 °C
SDETFF	140.11	166.39	194.27	3.93	5.67	9.02
CDFF	156.99	188.44	261.14	4.14	6.58	12.02
CPEFF	141.66	177.72	217.87	3.83	6.93	10.43
DIFF-CGS	239.73	286.21	369.83	4.18	9.16	15.41

* The delay parameters are measured when the output load is 20 fF. SDETFF: static dual edge-triggered flip-flop; CDFF: conditional discharge flip-flop; CPEFF: conditional pulse-enhancement flip-flop; DIFF-CGS: dual-edge implicit flip-flop with an embedded clock-gating scheme

Conclusions

- A novel DIFF-CGS exhibiting excellent power reduction by means of employing a clock-gating scheme in pulse generation is proposed.
- Extensive post-layout simulation results show that DIFF-CGS gains an improvement of 41.39%to 56.21% in terms of power consumption against its rival designs at 10% data switching activity at typical corner.
- Full-swing operations in both implicit pulse generation and the static latch improve the robustness of the design.
- Therefore, the proposed DIFF-CGS is quite suitable for power-efficient applications in VLSI designs which are not sensitive to delay.