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A novel ternary half adder and multiplier based on carbon nanotube field effect transistors

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Key words: CNTFET-based design; Ternary; Half adder; Multiplier; Nanotechnology; Multiple valued logic (MVL)

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Motivation

- The efficiency of the systems are mainly evaluated by their multipliers capability since multipliers are generally the slowest components of a system while occupying the most space.

- The most considerable obstacles of increasing the speed and decreasing the size due to the circuit RC delays are circuit interconnections so that in modern designs, more than half of the occupied space is for circuit interconnection

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Main idea

- Circuits designed based on Carbon Nanotubes Field Effect Transistors (CNTFETs) consume less power and are much faster than the conventional silicon FET-based circuits.
- Multiple-Valued Logic (MVL) reduces the number of required operations for a special mathematical function and reduces the circuit area as well.
- Combining the abilities of Carbon Nanotubes Transistors with the advantages of Multiple Valued can provide a unique design which has a higher speed and less complexity.

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Method

The diameters of the CNTs adjust the appropriate threshold voltages.

$$V_{TH} \approx \frac{0.43}{D_{CNT} / \text{nm}} \text{ eV}$$

In the proposed design, the diameters of CNTs are 1.487 nm, 1.096 nm and 0.783 nm, and the chi rality of the CNTs would be (19, 0), (14, 0) and (10, 0). As a result, by changing the chirality vector, the threshold voltage will also change

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The proposed designs are :

(1) ternary half-adder (THA)

(2) Proposed Ternary Multiplier (TMUL)

Proposed ternary half-adder

Half adder is a combinational circuit that adds two ternary inputs and represents ternary Sum and Carry in output.

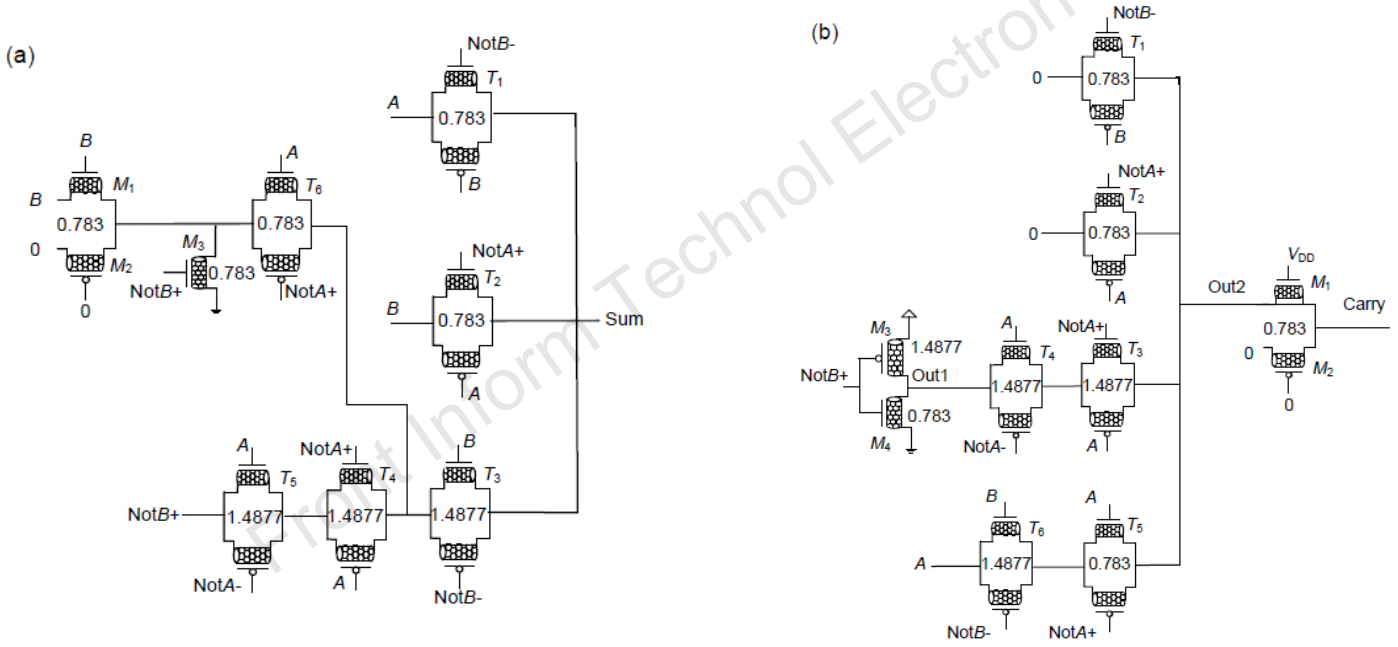


Fig. 2 Proposed CNTFET based ternary half adder: (a) Sum; (b) Carry

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Proposed ternary multiplier

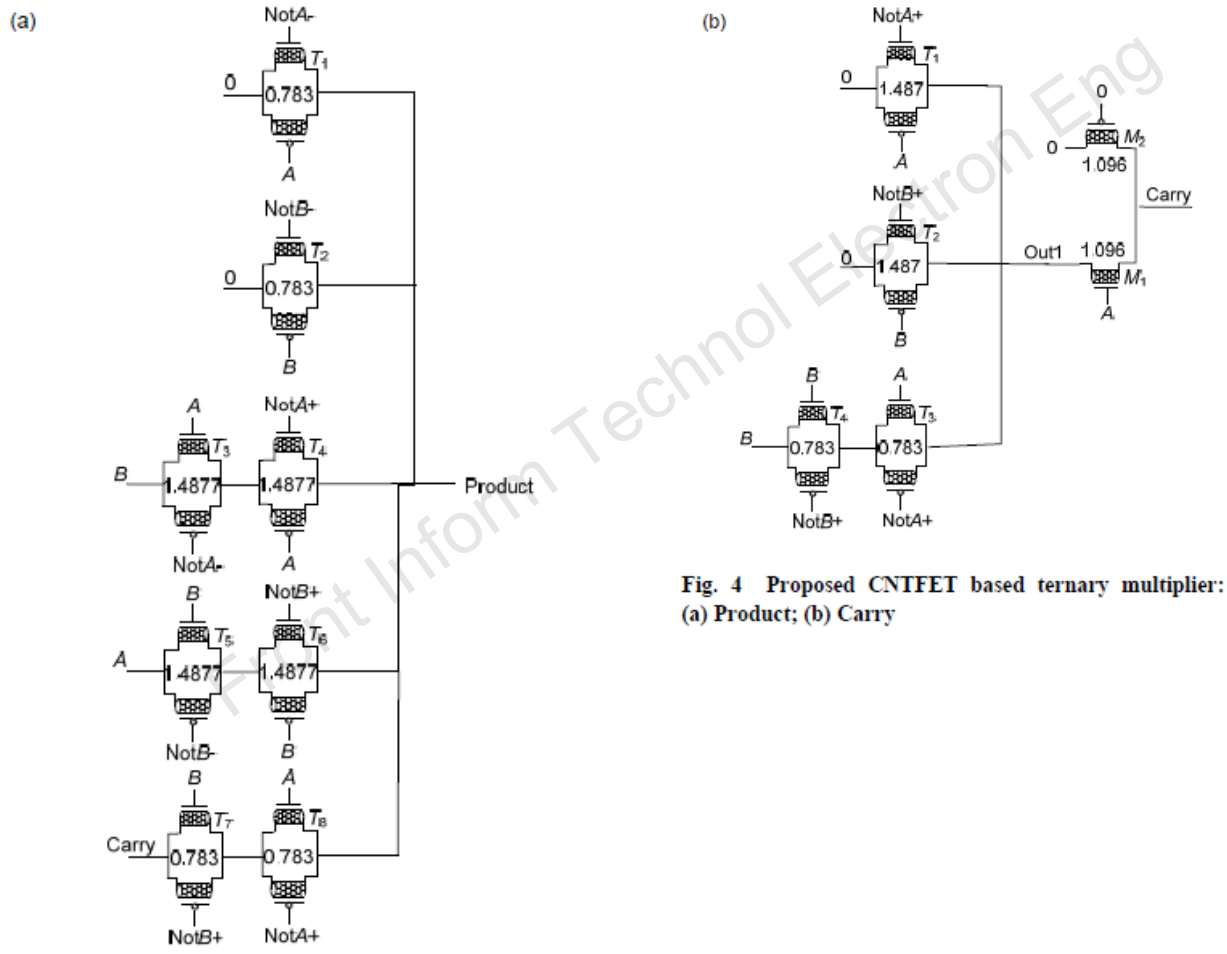


Fig. 4 Proposed CNTFET based ternary multiplier: (a) Product; (b) Carry

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Major results

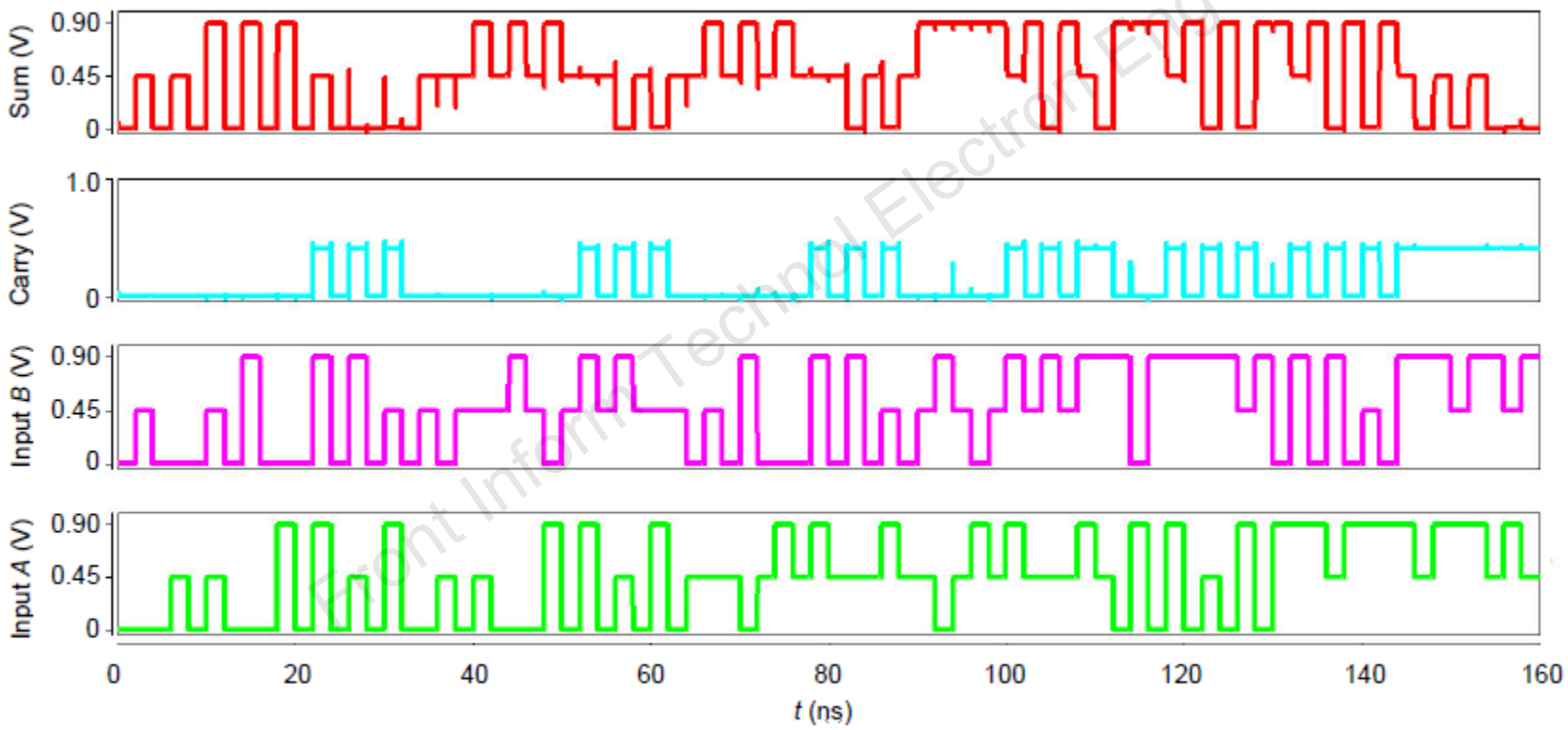


Fig. 3 Transient responses of the proposed ternary half adder

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Major results

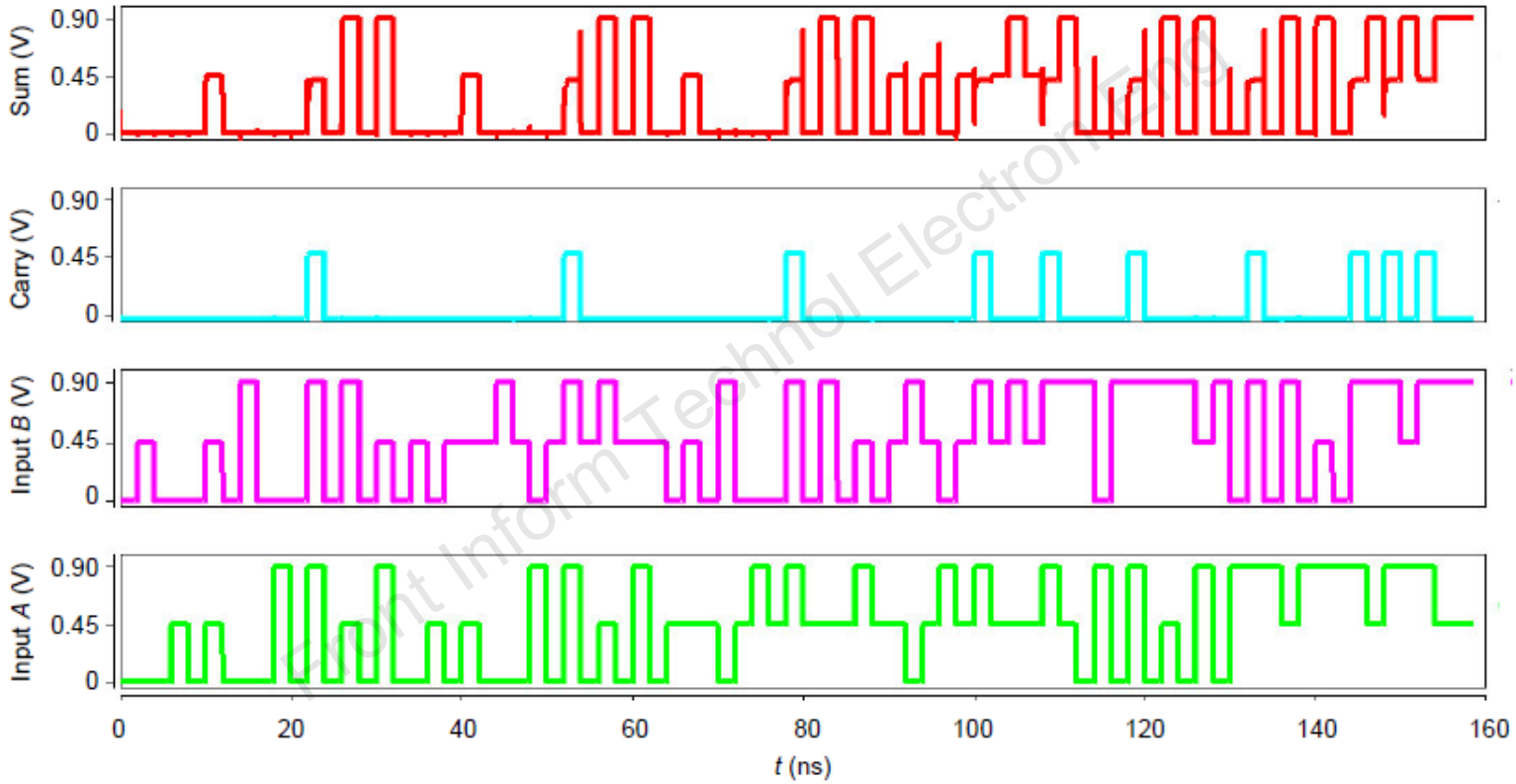


Fig. 5 Transient responses of the proposed ternary multiplier

Conclusions

- Each of the proposed ternary circuits has got transmission gates and CNT transistors.
- The simulation results demonstrate that proposed circuits have achieved higher speed, lower power consumption and reduced area.
- The presented results show that the design approach using the ternary converter combined with CNTFETs is a practical solution for low complexity and high speed VLSI design with CNTFETs in nanoscale era.

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