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Wide-range tacking technique for process-variation-robust clock and data recovery applications

Key words: Clock and data recovery; Digital loop filter; Phase interpolator

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Motivation

- The input–output (IO) bandwidth is becoming the bottleneck of the overall system. This issue underlines the existing challenges in design of a robust transceiver in complex environment.
- Designing a receiver suitable for different clocking architectures is the key in a transceiver.
- There are two methods to implement clock and data recovery (CDR): analog and digital. It is necessary to design a wide tracking range clock and data recovery circuit in receiver.

Main idea

- By comprehensively analyzing the second order Bang-Bang (BB) CDR, a digital CDR controller is adopted to extend the tracking range to compensate the large frequency offset in plesiochronous clocking system.
- A symmetrical latch is proposed to overcome the nonsymmetry problem of the conventional SR (set–reset) latch.
- A phase interpolator (PI) with clock condition circuit is proposed to improve the jitter performance of the receiver.
- A dithering source is designed to achieve 8-bit resolution out of the 6-bit phase DAC, which saves the area with a higher resolution.

Method

Second-Order CDR System Analysis

$$A \le \frac{f_{bb}}{f_{mod}}\left(1+\frac{2n}{\xi}\right)$$

Frequency tracking range and slew rate limiting of CDR loop are extended by the integrative path, and the loop dynamics is controlled by two degrees of freedom, f_{bb} and ξ.

Circuit Implementation

A. *Sampler*

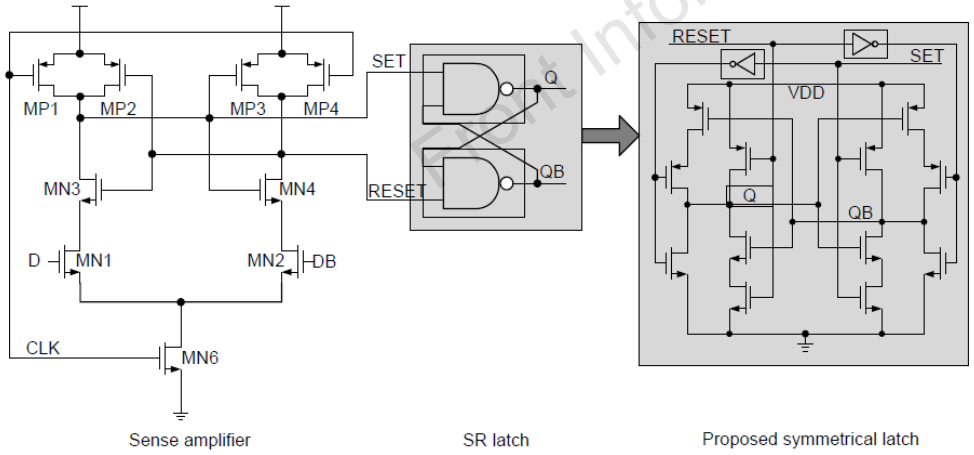

Fig. 4 Typical SAFF and the proposed symmetrical latch

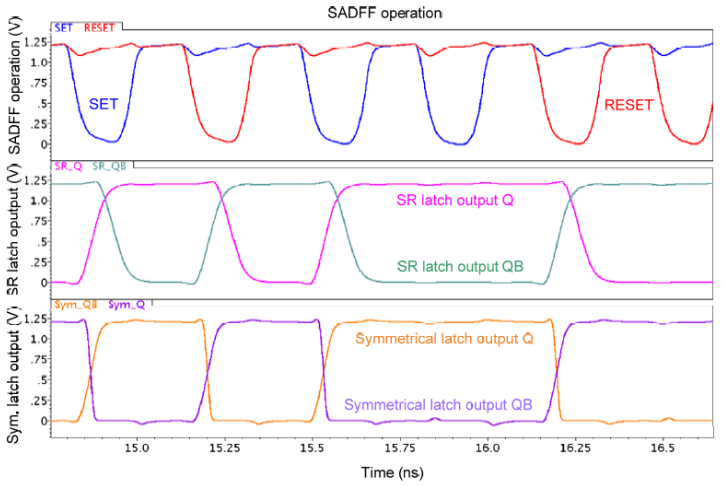

Fig. 5 Comparison between a typical SR latch and the proposed symmetrical latch output

Method (Cont'd)

Circuit Implementation

B. *Digital CDR Controller*

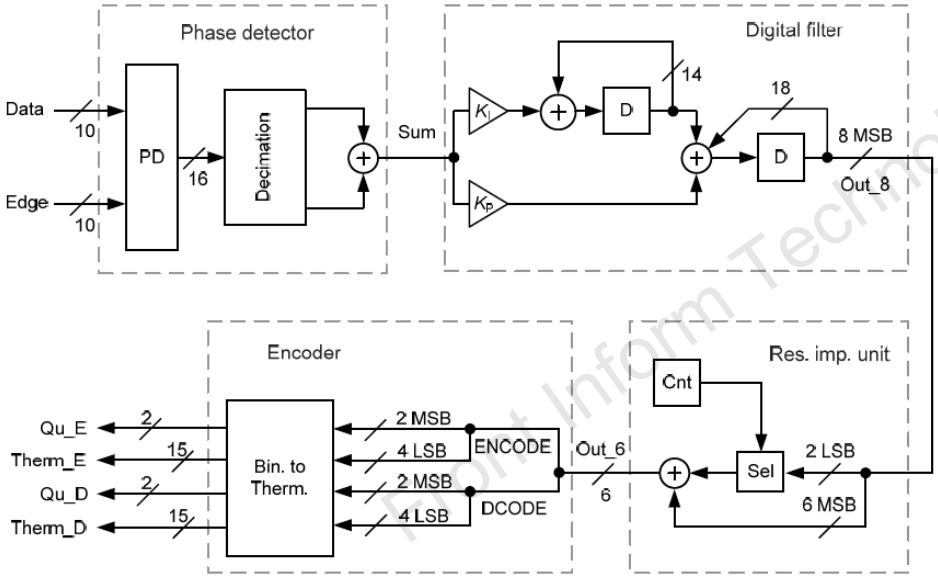

Fig. 6 Digital CDR controller architecture

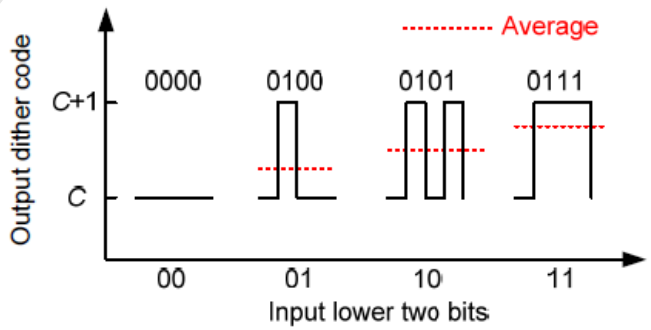

Fig. 7 Concept of phase DAC resolution improving dither

A second order digital loop filter extend the frequency tracking range to 5000 ppm. And a dithering source is designed to achieve 8-bit resolution out of the 6-bit phase DAC.

Method (Cont'd)

Circuit Implementation

C. *Phase Interpolator*

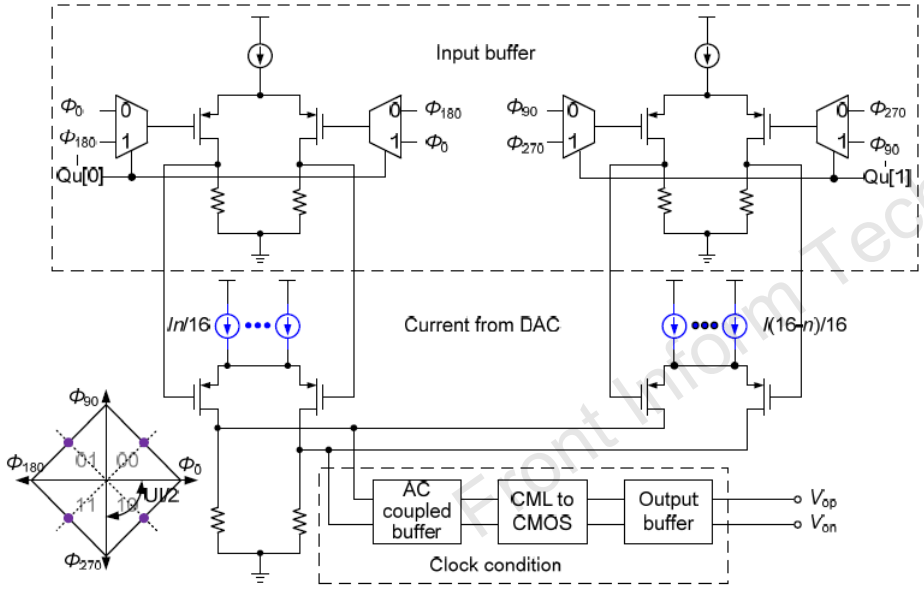

Fig. 8 Architecture of the phase interpolator

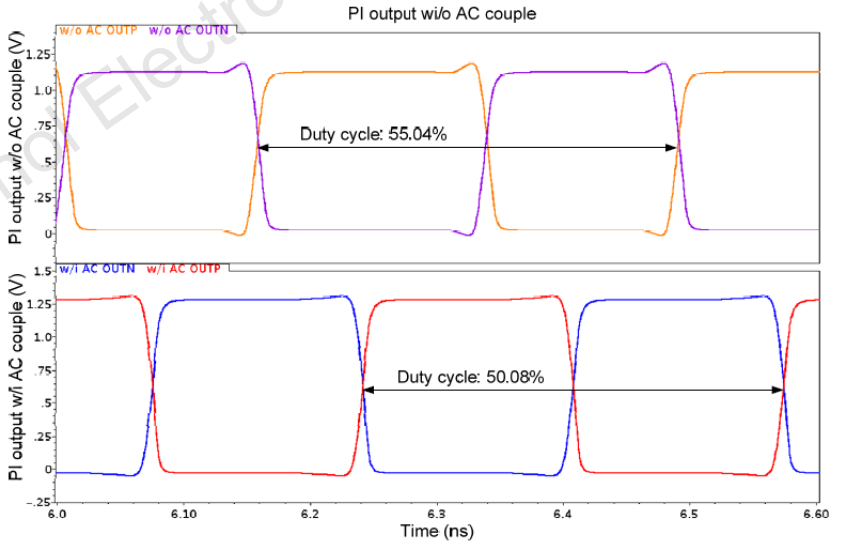

Fig. 9 Comparison between output duty-cycle distortion with and without output buffer

An AC-coupled duty-cycle correction output buffer makes the duty-cycle distortion to reduce from 55.04% to 50.08%.

Major results

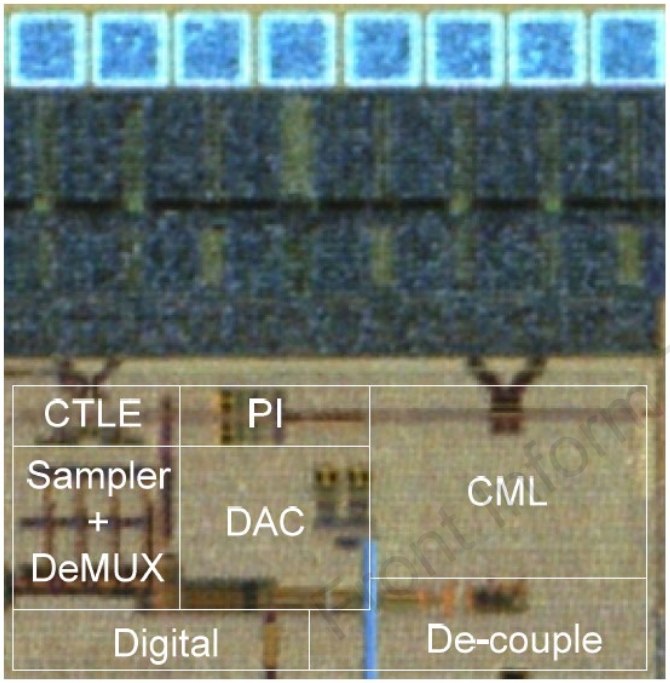

Fig. 10 Photo of the receiver macro

- The receiver has been implemented in 65-nm CMOS technology. The module occupies an area of 0.147 mm^2 with a 0.082 mm^2 core area. The measured power of the receiver is 41 mW with a 1.2 V power supply at 5 Gb/s.

- The output RMS jitter is only 6.7 ps at 5Gb/s. and the tracking range of the receiver is ±6600 ppm for 2.5 Gb/s and ±6000 ppm for 5 Gb/s with BER below 10^{-12}.

Major results (Cont'd)

Table 1 Receiver performance summary

Parameter	Value					
	Coban *et al.* (2005)	Agrawal *et al.* (2009)	Kalantari and Buckwalter (2013)	Abiri *et al.* (2011)	Sarvari *et al.* (2010)	This work
Technology (CMOS)	150 nm	130 nm	130 nm	65 nm	65 nm	65 nm
Supply voltage (V)	1.2	1.45	1.2	1.2	1.2	1.2
Operating frequency (Gb/s)	2–3.2	5	5–7	5	5	5
Maximum frequency offset ($\times 10^{-6}$)	±1200	±5000	±200	–	200	±6000
Bit error rate	–	10^{-12}	10^{-12}	10^{-12}	10^{-12}	10^{-12}
High frequency jitter tolerance (UI)	0.5	–	0.4	0.2	0.24	0.32
Power consumption (mW)	73.2	54.2	67.9	114	211.2	40.68
Active die area (mm^2)	0.43	0.35	1.025	0.4	0.374	0.082

Conclusions

- A 5 Gb/s receiver with a wide tracking range CDR circuit was presented.
- A digital CDR controller, which is not sensitive to the process variations, is adopted to extend the tracking range. A PI with clock condition circuit is adopted to improve the jitter performance. A dithering source is designed to achieve 8-bit resolution out of the 6-bit phase DAC, which saves the area with the higher resolution.
- The extremely compact receiver with relatively low power consumption is therefore suitable for high-density and robust serial link applications.