Mao-qun Yao, Kai Yang, Ji-zhong Shen, Cong-yuan Xu, 2017. Function synthesis algorithm based on RTD-based three-variable universal logic gates. *Frontiers of Information Technology & Electronic Engineering*, **18**(10):1654-1664. http://dx.doi.org/10.1631/FITEE.1601730

Function synthesis algorithm based on RTD-based three-variable universal logic gates

Key words: Resonant tunneling device (RTD); Disjunctive decomposition algorithm; Universal logic gate; Truth value matrix; Function synthesis algorithm

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Motivation

- Compared to CMOS, a resonant tunneling diode (RTD) has better performance and features.
- The universal logic gate has a powerful logic function, and has become an important unit circuit for implementing the *n*-variable logical function.
- There are no function synthesis algorithms that can implement an *n*-variable logical function by RTD-based universal logic gates.

Main idea

1. We proposed a new concept, i.e., the truth value matrix, which can express a logic function.

2. According to the expression of true value matrices of a logic function, a novel disjunctive decomposition algorithm is proposed, which can decompose an arbitrary *n*-variable logical function into three-variable subset functions.

3. Based on the three-variable subset functions of the decomposed logic function, a novel function synthesis algorithm is developed, which can implement arbitrary *n*-variable logical functions by RTD-based three-variable universal logic gates (ULG3s).

Example Implement the five-variable function with RTD-based three-variable universal logic gates (ULG3s).

$$f(x_1, x_2, x_3, x_4, x_5) = \sum_i m_i,$$

i=0, 2, 3, 5, 6, 9, 12, 15, 24, 25, 26, 27, 28, 29, 30, 31.
where m_i is the minimum item of the function.

Design:

(1) The true value matrix of $f(x_1, x_2, x_3, x_4, x_5)$ is

$$\mathbf{TM} = \begin{bmatrix} 1 & 0 & 1 & 1 & 0 & 1 & 1 & 0 \\ 0 & 1 & 0 & 0 & 1 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 \end{bmatrix}$$

(2) According to the proposed disjunctive decomposition algorithm, the function can be decomposed into three-variable subset functions as

$$f(x_1, x_2, g) = \overline{x}_1 \overline{x}_2 \overline{g} + x_1 x_2 \overline{g} + \overline{x}_1 x_2 g + x_1 x_2 g$$

$$g(x_3, x_4, x_5) = \overline{x}_3 \overline{x}_4 x_5 + x_3 \overline{x}_4 \overline{x}_5 + x_3 x_4 x_5$$

where $f(x_1, x_2, g)$ and $g(x_3, x_4, x_5)$ are three-variable non-threshold functions. They can be implemented by ULG3s.

(3) Then, $f(x_1, x_2, x_3, x_4, x_5)$ can be implemented by two ULG3s. Fig. 5 shows the ULG3 implementation of this function.

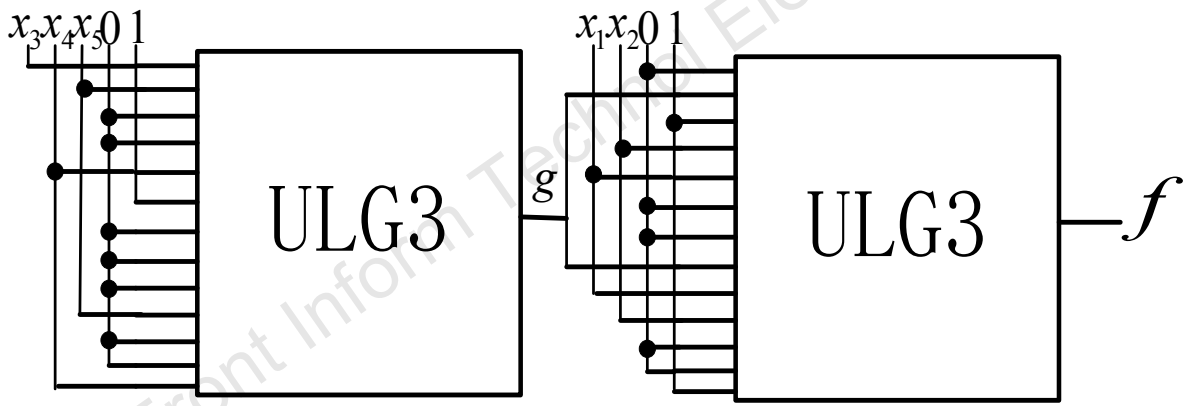

Fig. 5 Circuit for the example

Conclusions

- A novel function synthesis algorithm is proposed which can implement an arbitrary *n*-variable logical function using RTD-based universal logic gates.
- If the *n*-variable logical function is a directly disjunctive decomposition one, the circuit structure will be very simple, and if the *n*-variable logical function is a non-directly disjunctive decomposition one, the circuit structure will be simpler than implement by only UTLGs.
- The proposed function synthesis algorithm is straightforward to program, and provides a new solution to implement an arbitrary *n*-variable logical function by RTD-based universal logic gates.