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Fractional-order memristive neural synaptic weighting achieved by pulse-based fracmemristor bridge circuit

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Key words: Fractional calculus; Fracmemristor; Fracmemristance; Fractional-order memristor; Fractional-order memristive synapses

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Motivation

1. The changes occurring in synaptic weight are well known as synaptic plasticity, which is the cellular mechanism that underlies learning and memory. The synaptic simulation is a hot area of research. However, due to the lack of a proper device to implement the synapses, research in this area has only had limited success practically.
2. The existing memristor bridge synapses were of the integer-order memristive neural synaptic weightings. While the concept of memristor has been generalized preliminarily from the classical integer-order memristor to the fractional-order memristor, a challenging theoretical problem would be whether the fracmemristor can be applied to achieve the fractional-order memristive synapses or not.

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Main idea

1. To implement the fractional-order memristive neural synaptic weighting, the pulse-based fracmemristor bridge circuit should be firstly designed.
2. By applying a pulse-based fracmemristor bridge circuit, the fracmemristor bridge synaptic circuit can be achieved.
3. By applying the fracmemristor bridge synaptic circuit, the fracmemristor bridge neuron circuit can be implemented. Furthermore, the architecture of the fractional-order memristive neural networks circuit can be obtained.

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Method

The pulse-based fracmemristor bridge circuit can be obtained by two *v*-order oppositely incremental capacitive fracmemristors (FM_1^1 and FM_2^1) with the same circuit parameters (Fig. 1).

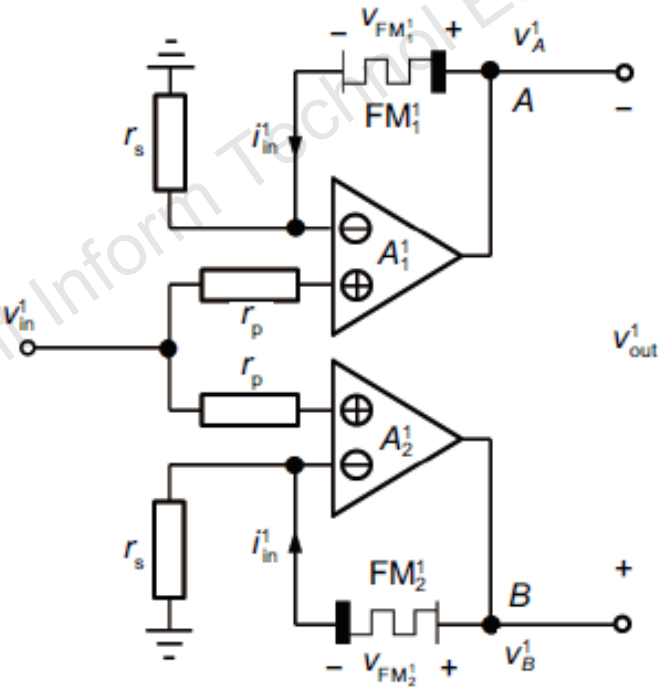


Fig. 1 Pulse-based fracmemristor bridge circuit

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Major results

Comparison of electrical characteristics between the pulse-based fracmemristor and memristor bridge circuits

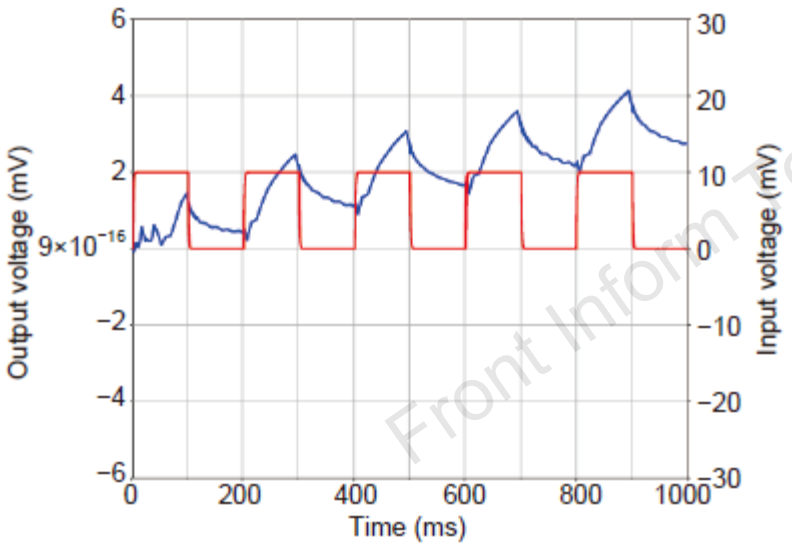


Fig. 9 Output voltage of a pulse-based fracmemristor bridge circuit with $v_{\mathrm{in}}^{1}(t) = 10$ mV, $r_{\mathrm{p}} = 1000\ \Omega$, and $r_{\mathrm{s}} = 1000\ \Omega$. Red corresponds to the right vertical axis and blue corresponds to the left vertical axis

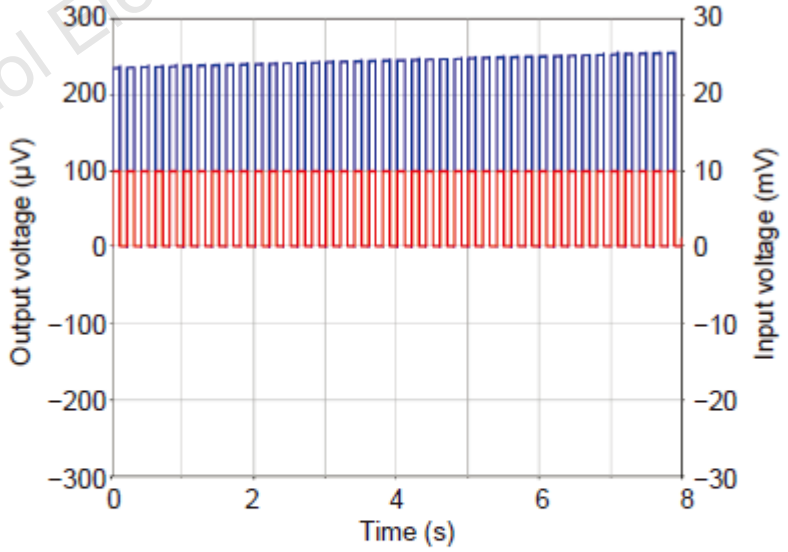


Fig. 10 Output voltage of a pulse-based memristor bridge circuit with $v_{\mathrm{in}}^{1}(t) = 10$ mV, $r_{\mathrm{p}} = 1000\ \Omega$, and $r_{\mathrm{s}} = 1000\ \Omega$. Red corresponds to the right vertical axis and blue corresponds to the left vertical axis

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Major results (Cont'd)

Simulation of LTP and LTD

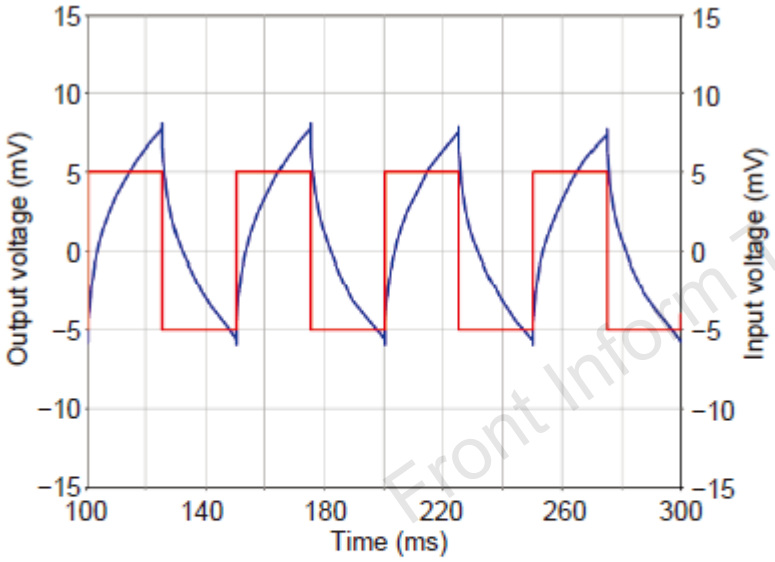


Fig. 13 Output voltage of a pulse-based fracmemristor bridge circuit with the duty cycle of the input voltage pulse equal to 50%. Red corresponds to the right vertical axis and blue corresponds to the left vertical axis.

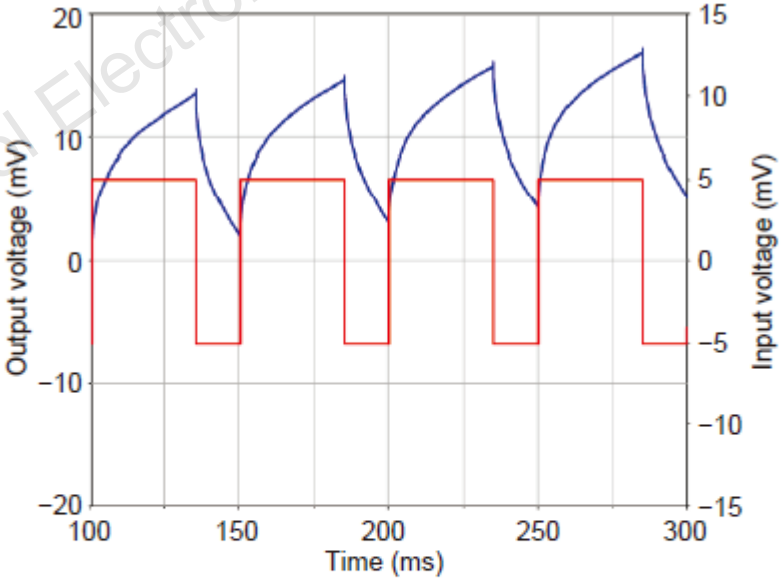


Fig. 14 Output voltage of a pulse-based fracmemristor bridge circuit with the duty cycle of the input voltage pulse equal to 70%. Red corresponds to the right vertical axis and blue corresponds to the left vertical axis

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Conclusions

1. The pulse-based memristor bridge circuit realizes linear weighting on the input signal, whereas the pulse-based fracmemristor bridge circuit yields nonlinear weighting operation, which is more appropriate for explaining the neural synaptic weighting.

2. Electrical characteristics of a pulse-based fracmemristor bridge circuit can be used to explain the cellular mechanisms that underlie learning and memory such as LTP, LTD, habituation, and sensitization.

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