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Fractional-order memristive neural synaptic weighting achieved by pulse-based fracmemristor bridge circuit

Key words: Fractional calculus; Fracmemristor; Fracmemristance; Fractional-order memristor; Fractional-order memristive synapses

Corresponding authors: Qiuyan HE and Xiao YUAN
E-mail: heqiuyan789@163.com and yuanxiao@scu.edu.cn
ORCID: https://orcid.org/0000-0002-4983-778X; https://orcid.org/0000-0003-3003-0326

Motivation

1. The changes occurring in synaptic weight are well known as synaptic plasticity, which is the cellular mechanism that underlies learning and memory. The synaptic simulation is a hot area of research. However, due to the lack of a proper device to implement the synapses, research in this area has only had limited success practically.
2. The existing memristor bridge synapses were of the integer-order memristive neural synaptic weightings. While the concept of memristor has been generalized preliminarily from the classical integer-order memristor to the fractional-order memristor, a challenging theoretical problem would be whether the fracmemristor can be applied to achieve the fractional-order memristive synapses or not.

Main idea

1. To implement the fractional-order memristive neural synaptic weighting, the pulse-based fracmemristor bridge circuit should be firstly designed.
2. By applying a pulse-based fracmemristor bridge circuit, the fracmemristor bridge synaptic circuit can be achieved.
3. By applying the fracmemristor bridge synaptic circuit, the fracmemristor bridge neuron circuit can be implemented. Furthermore, the architecture of the fractional-order memristive neural networks circuit can be obtained.

Method

The pulse-based fracmemristor bridge circuit can be obtained by two *v*-order oppositely incremental capacitive fracmemristors (FM_1^1 and FM_2^1) with the same circuit parameters (Fig. 1).

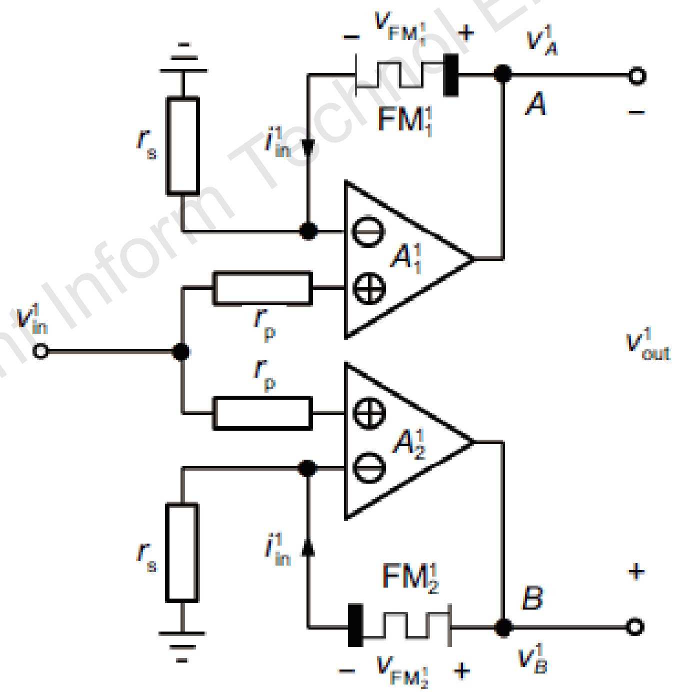

Fig. 1 Pulse-based fracmemristor bridge circuit

Major results

Comparison of electrical characteristics between the pulse-based fracmemristor and memristor bridge circuits

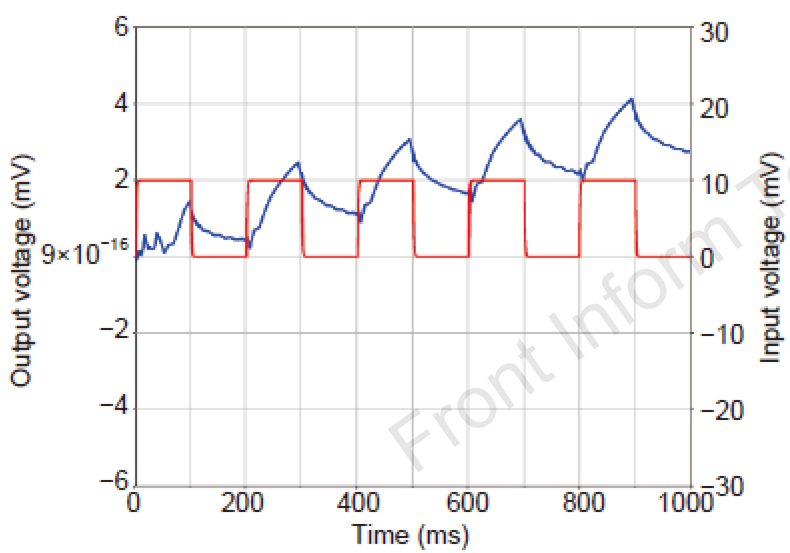

Fig. 9 Output voltage of a pulse-based fracmemristor bridge circuit with $v_{\text{in}}^{1}(t) = 10$ mV, $r_{\text{p}} = 1000\ \Omega$, and $r_{\text{s}} = 1000\ \Omega$. Red corresponds to the right vertical axis and blue corresponds to the left vertical axis

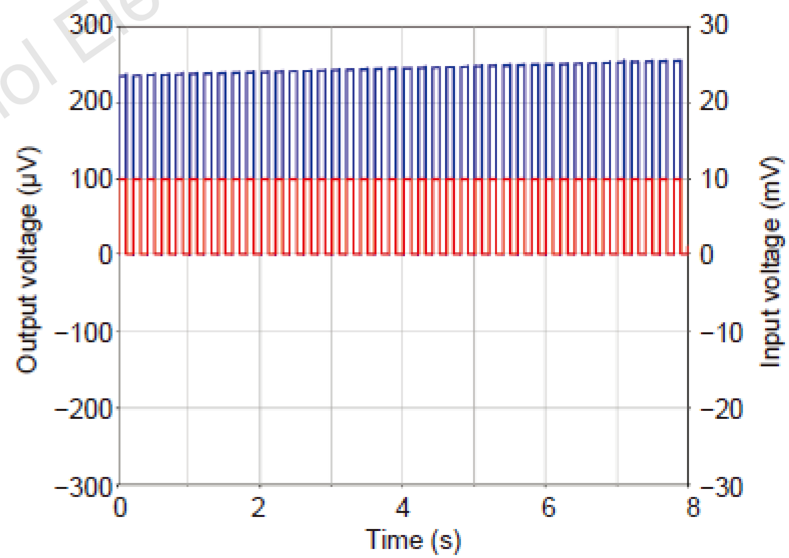

Fig. 10 Output voltage of a pulse-based memristor bridge circuit with $v_{\text{in}}^{1}(t) = 10$ mV, $r_{\text{p}} = 1000\ \Omega$, and $r_{\text{s}} = 1000\ \Omega$. Red corresponds to the right vertical axis and blue corresponds to the left vertical axis

Major results (Cont'd)

Simulation of LTP and LTD

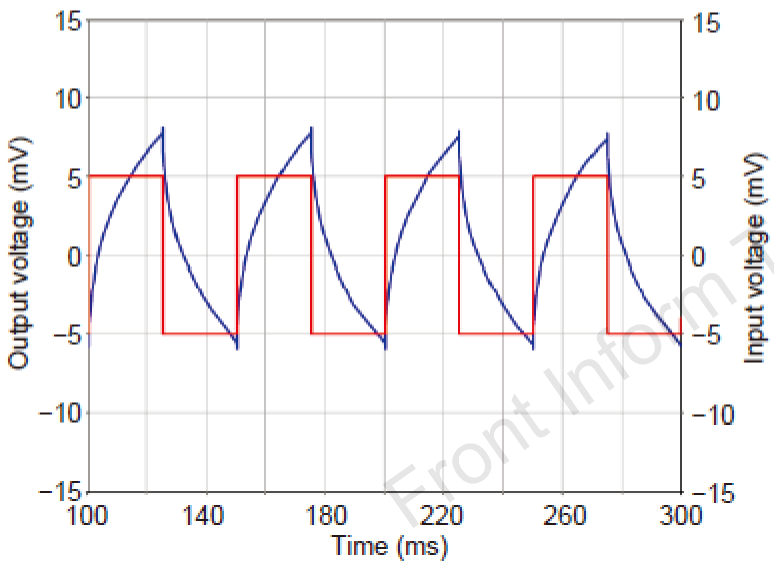

Fig. 13 Output voltage of a pulse-based fracmemristor bridge circuit with the duty cycle of the input voltage pulse equal to 50%. Red corresponds to the right vertical axis and blue corresponds to the left vertical axis

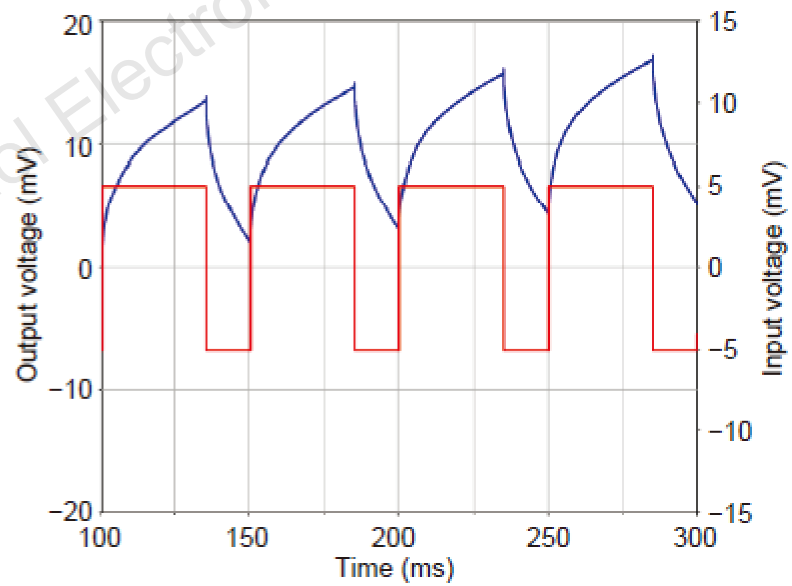

Fig. 14 Output voltage of a pulse-based fracmemristor bridge circuit with the duty cycle of the input voltage pulse equal to 70%. Red corresponds to the right vertical axis and blue corresponds to the left vertical axis

Conclusions

1. The pulse-based memristor bridge circuit realizes linear weighting on the input signal, whereas the pulse-based fracmemristor bridge circuit yields nonlinear weighting operation, which is more appropriate for explaining the neural synaptic weighting.

2. Electrical characteristics of a pulse-based fracmemristor bridge circuit can be used to explain the cellular mechanisms that underlie learning and memory such as LTP, LTD, habituation, and sensitization.

蒲亦非，四川大学计算机学院（软件学院）教授、博士生导师。研究领域：分数阶微积分理论及应用、分数阶数字图像处理、分数阶机器学习、分忆抗（分数阶忆阻）、分数阶信号处理、计算法学（人工智能+法学）。发表SCI论文40余篇，其中以第一作者在*IEEE Trans Image Process*, *IEEE Trans Neur Netw Learn Syst*, *IEEE Trans Circ Syst I Regul Pap*, *Int J Neur Syst*, *IEEE Intell Transp Syst Mag*, *IEEE Int Things J*, *Sci China Inform Sci*等期刊发表SCI论文20余篇；以第一发明人身份获授权专利14项；出版学术专著5部。以第一作者身份发表的论文“Fractional Differential Approach to Detecting Textural Features of Digital Image and Its Fractional Differential Filter Implementation”获得*Sci China Inform Sci* 2018年十年持续影响力论文奖。担任中国自动化学会分数阶系统与控制专业委员会副主任委员、中国自动化学会自适应动态规划与强化学习专业委员会委员、国际学术期刊*Metaheuristics*（启发式演算，Springer-Nature Press）编委。