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A large-current, highly integrated switched-capacitor divider with a dual-branch interleaved topology and light load efficiency improvement

Key words: Switched-capacitor converter; Dual branch; Integrated circuit; Bootstrap gate driver

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Motivation

- Because it is magnet-free and can achieve a high integration level, the switched-capacitor (SC) converter acting as a direct current transformer has many promising applications in modern electronics. However, designing an SC converter with large-current capability and high-power efficiency is still challenging.
- In this paper, we propose a dual-branch SC voltage divider and present its integrated circuit (IC) implementation. An effective on-chip gate-driving method using a capacitively coupled floating-voltage level shifter is proposed to drive the all-NMOS power train. We also use the digital frequency modulation method to improve light load efficiency.

Application scenarios of the SC converter used as a DC transformer

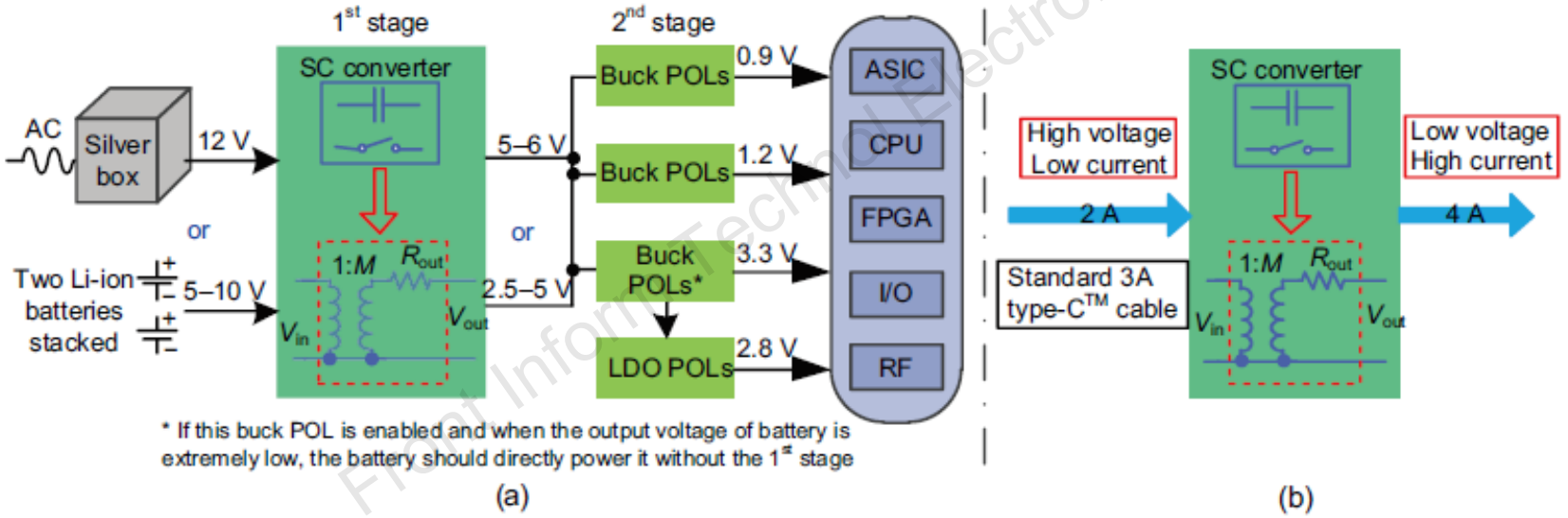


Fig. 1 Application scenarios of the SC converter used as a DC transformer: (a) SC converter used as a high efficiency first power stage in a distributed power architecture; (b) smartphone direct charging

Power stage of the proposed SC divider and its operation process

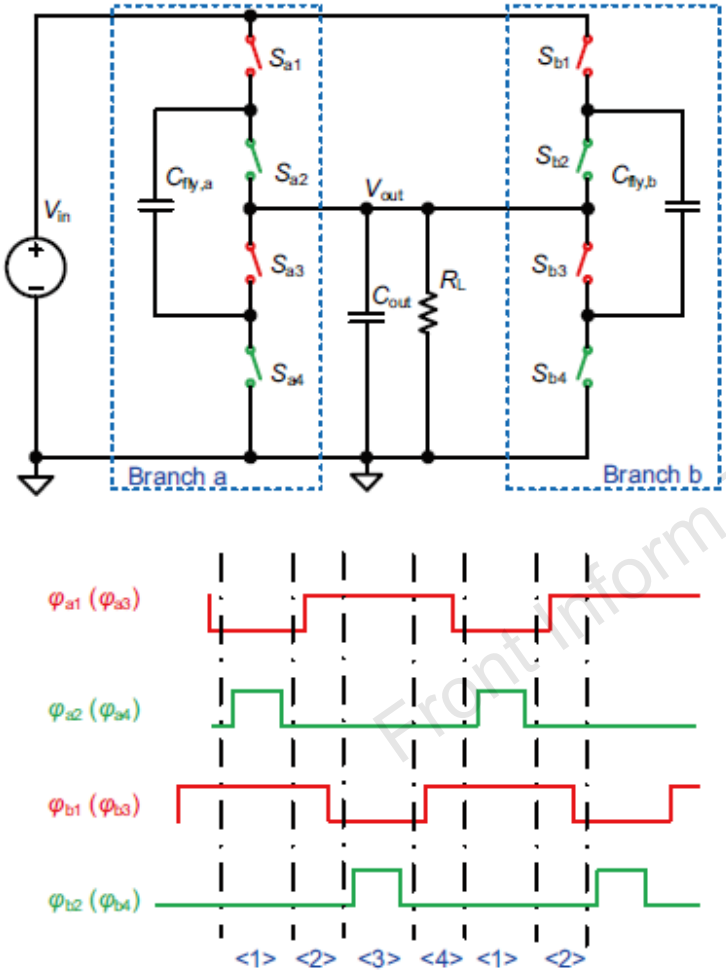


Fig. 2 Main topology of the proposed dual-branch interleaved SC divider and clock phases to drive the eight power switches

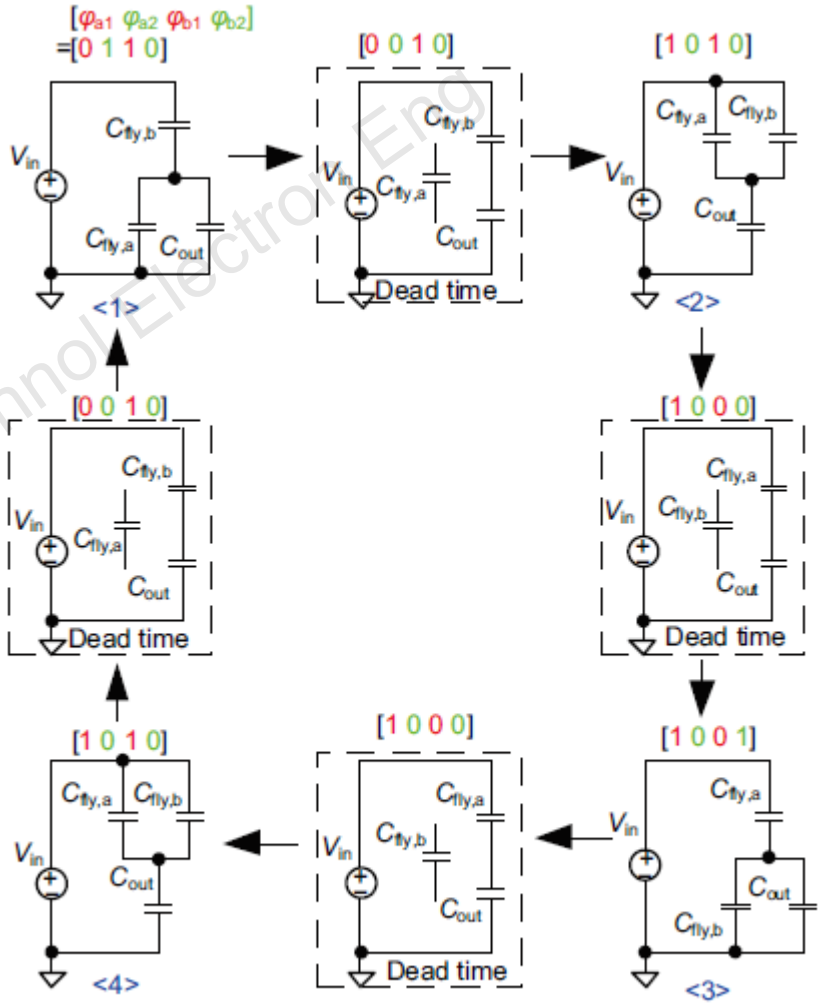


Fig. 3 Phase transition diagram of the divider

Self-powered bootstrap gate driver with the flying capacitor being reused

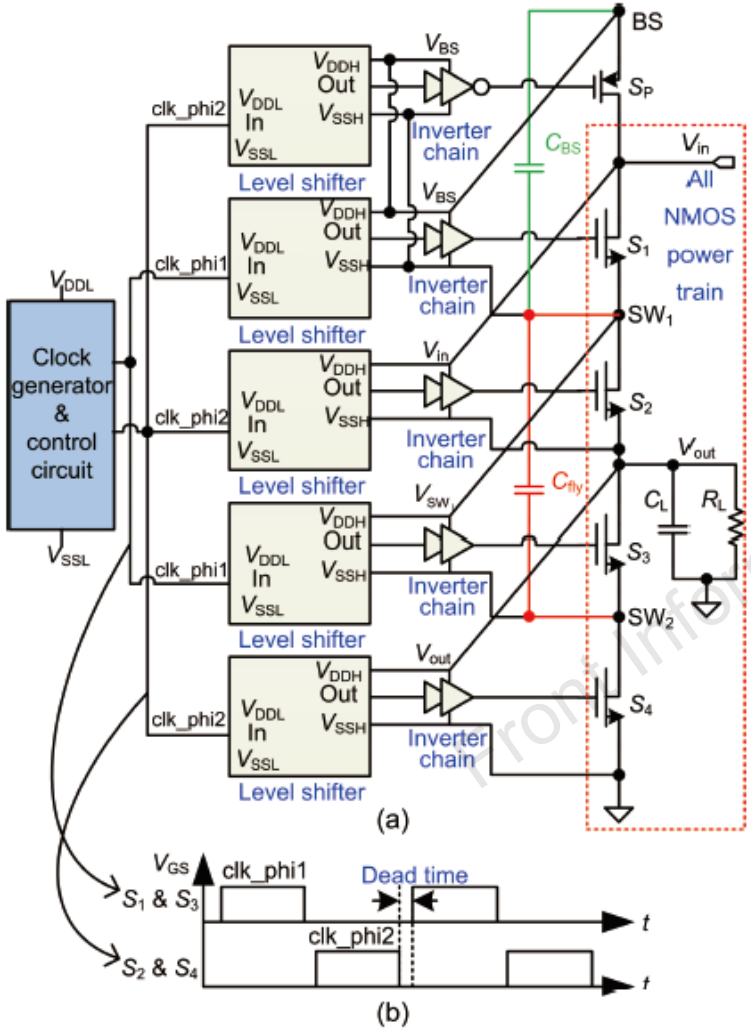


Fig. 5 Proposed C_{fly} reused bootstrap gate driver for branch a or b (a) and non-overlapping two-phase clock signals (b)

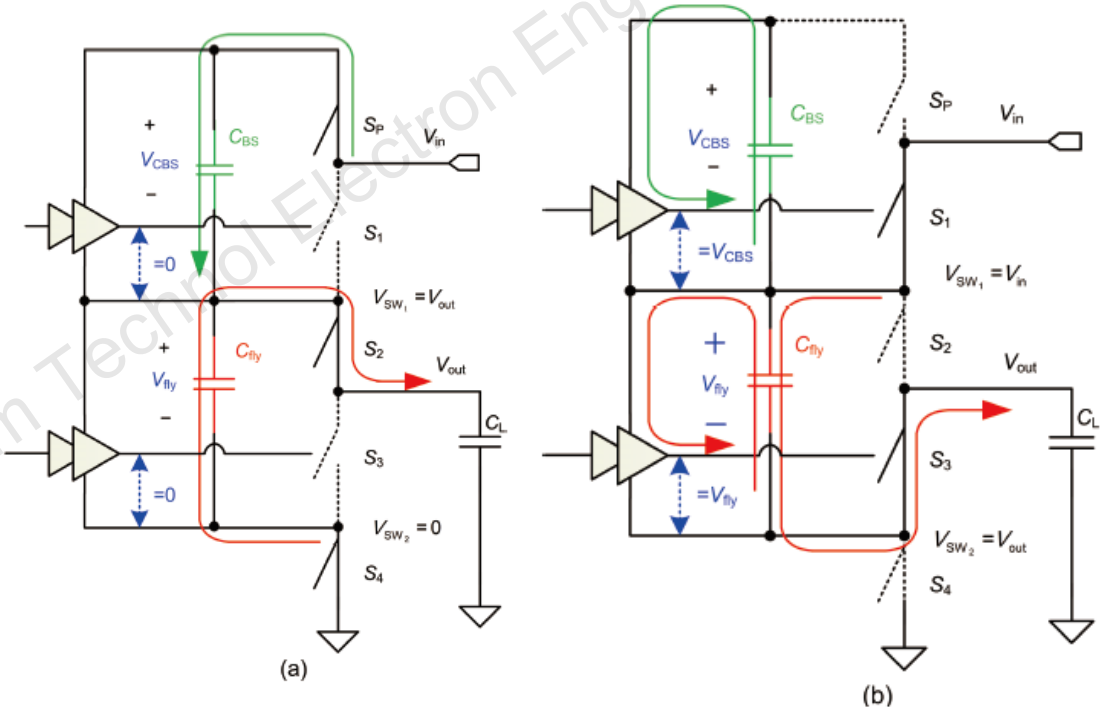


Fig. 6 Operation of the C_{fly} reused bootstrap gate driver: (a) during clk_phi2, C_{BS} is charged, whereas C_{fly} is discharged; (b) during clk_phi1, C_{BS} is the power supply for S_1, whereas C_{fly} is the power supply for S_3 and it is charged

Capacitively coupled floating-voltage level shifter used in the proposed self-powered gate driver

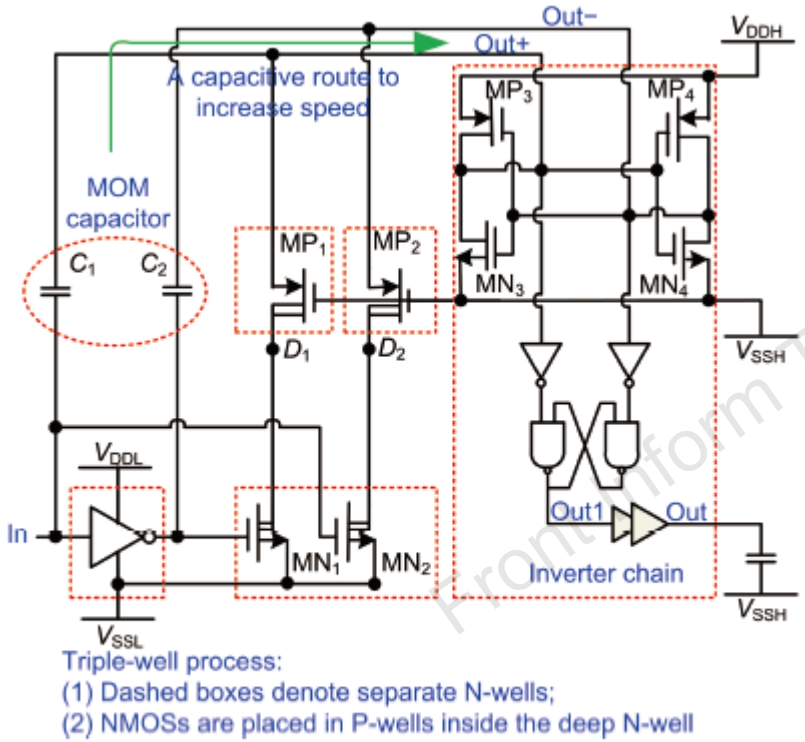


Fig. 7 Proposed capacitively coupled floating-voltage level shifter

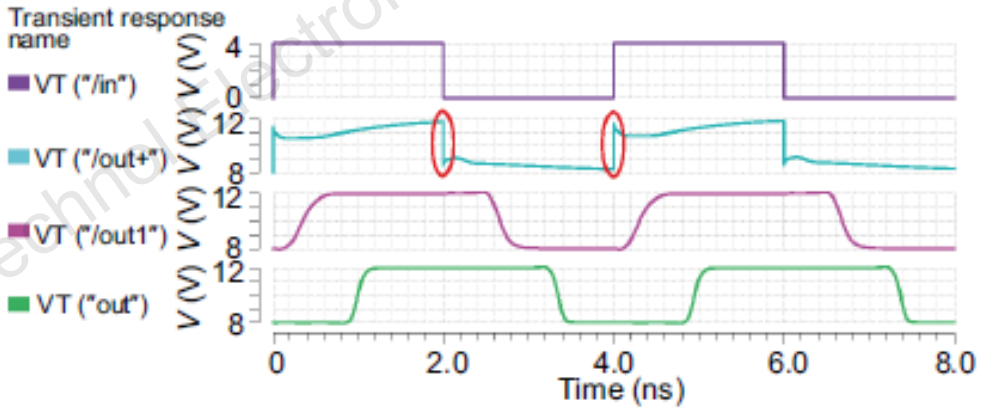


Fig. 8 Transient voltage waveforms of key nodes of the level shifter

Frequency modulation to improve light load power efficiency

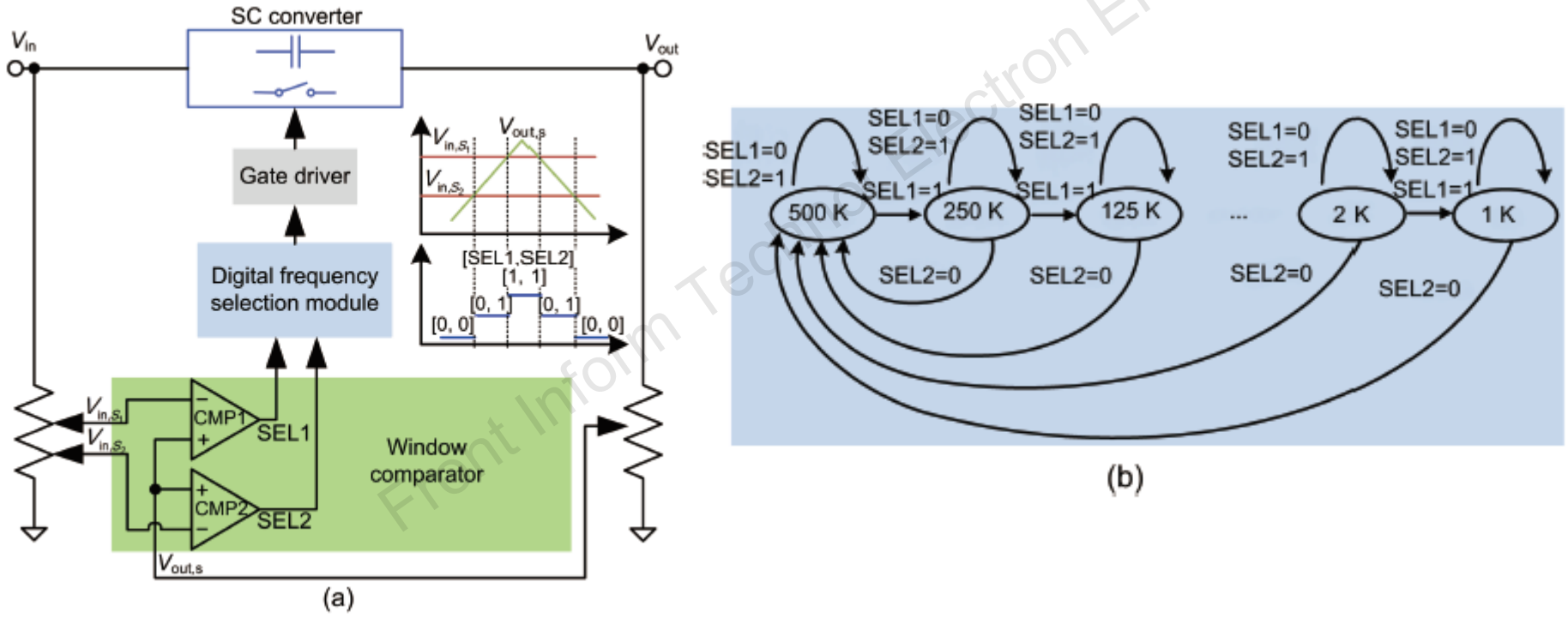
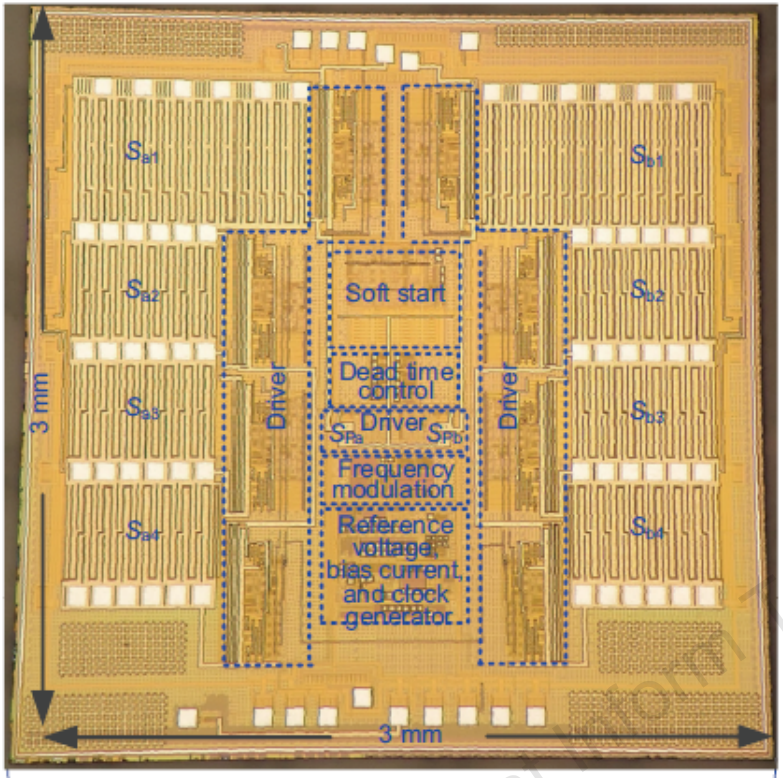
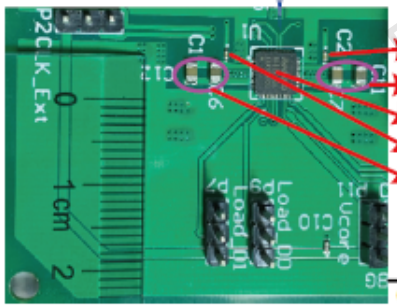


Fig. 9 Proposed digital frequency modulation method (a) and control logic of the digital frequency selection module (b)

Experimental results





Parameter	Value	No.	Package
$C_{BS,b}$	10 nF	1	0402
$C_{fly,b}$	47 μF	2	0805
Chip	N/A	1	QFN40
$C_{BS,a}$	10 nF	1	0402
$C_{fly,a}$	47 μF	2	0805
C_{in}	10 μF	2	0603
C_{out}	47 μF	1	0805

C_{in} and C_{out} are on the bottom side

Fig. 10 Chip micrograph of the designed SC voltage divider with each function block being enclosed and the evaluation PCB

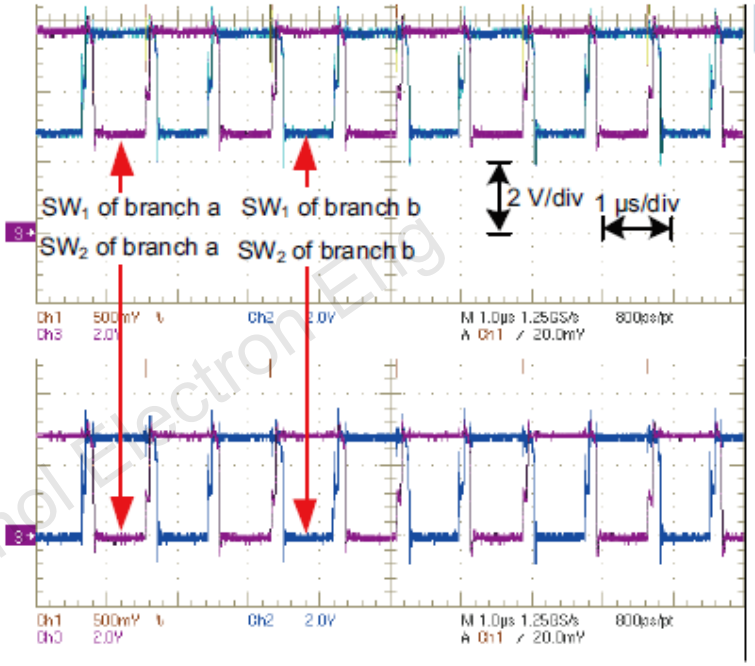


Fig. 11 Measured voltage waveforms of switching nodes (SW_1 and SW_2) of branches a and b with $I_L = 1$ A and $V_{in} = 6$ V

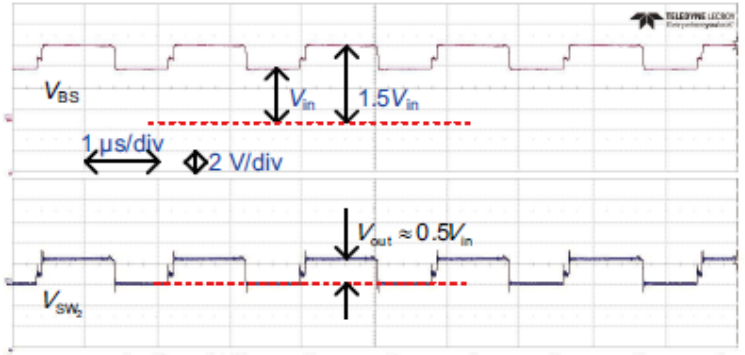


Fig. 12 Measured voltage waveforms of nodes BS and SW_2 of branch a

Experimental results

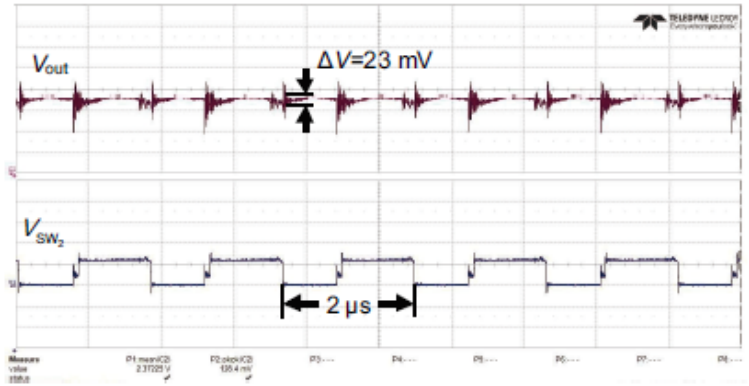


Fig. 13 Measured voltage waveforms of V_{out} and node SW_2 of branch a when $I_L = 1$ A

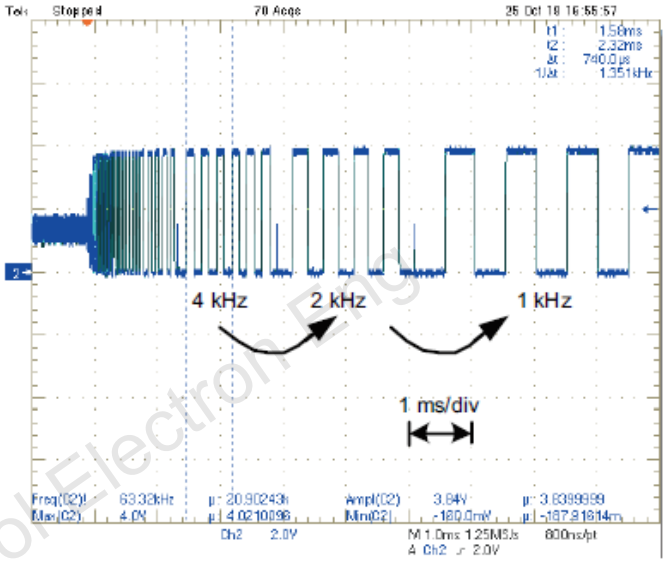


Fig. 14 Modulation process of the operation frequency at light load (observed from a test pin)

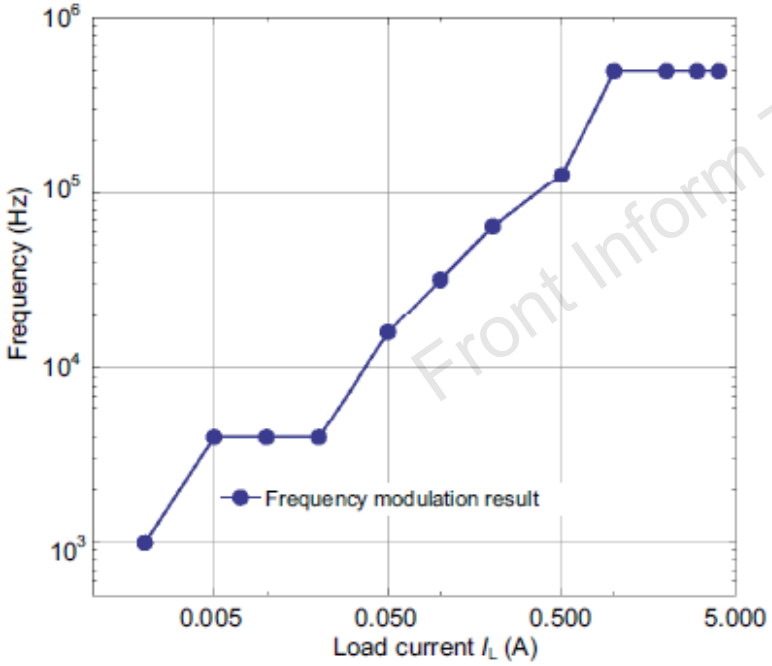


Fig. 15 Operation frequency variation with load current I_L

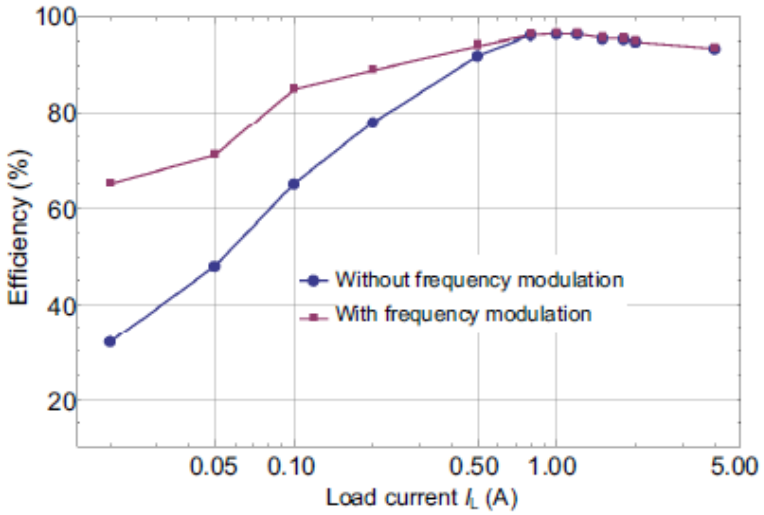


Fig. 16 Measured power efficiency with or without the frequency modulation method

Conclusions

- In this paper, we propose an SC voltage divider with dual interleaved operation and a self-powered gate driving technique for high-voltage high-power SC DC-DC converters.
- Using the proposed self-powered structure, the flying capacitor is also a bootstrap capacitor, and the number of bootstrap capacitors is reduced, hence simplifying the driving circuit and reducing the cost.
- A capacitively coupled high-speed floating-voltage level shifter is designed to implement the gate driver, and frequency modulation is also adopted to improve the light load power efficiency.
- A prototype chip using a 180-nm triple-well BCD process is designed, and the measurement results have verified the feasibility of the proposed dual-branch SC voltage divider with large current capability and high power efficiency.