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Design and optimization of a gate-controlled dual direction electro-static discharge device for an industry-level fluorescent optical fiber temperature sensor

Key words: Electric breakdown; Semiconductor device reliability; CMOS technology

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Motivation

1. The input/output (I/O) pins of an industry-level fluorescent optical fiber temperature sensor readout circuit need on-chip integrated high-performance electro-static discharge (ESD) protection devices.

2. It is difficult for the failure level of the basic N-type buried layer gate-controlled silicon controlled rectifier (NBL-GCSCR) manufactured by the 0.18 μm standard bipolar-CMOS-DMOS (BCD) process to meet this need.

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Main idea

1. We propose an on-chip integrated novel deep N-well gate-controlled silicon controlled rectifier (DNW-GCSCR) with a high failure level to effectively solve the problems based on a standard BCD process.

2. Technology computer-aided design (TCAD) simulation is used to analyze the device characteristics. Silicon controlled rectifiers (SCRs) are tested by transmission line pulses (TLPs) to obtain accurate ESD parameters.

3. The relationship among the physical structure, conduction path, and ESD parameters of the ESD device is studied based on a proposed gate-controlled principle. Two types of ESD device are analyzed and verified.

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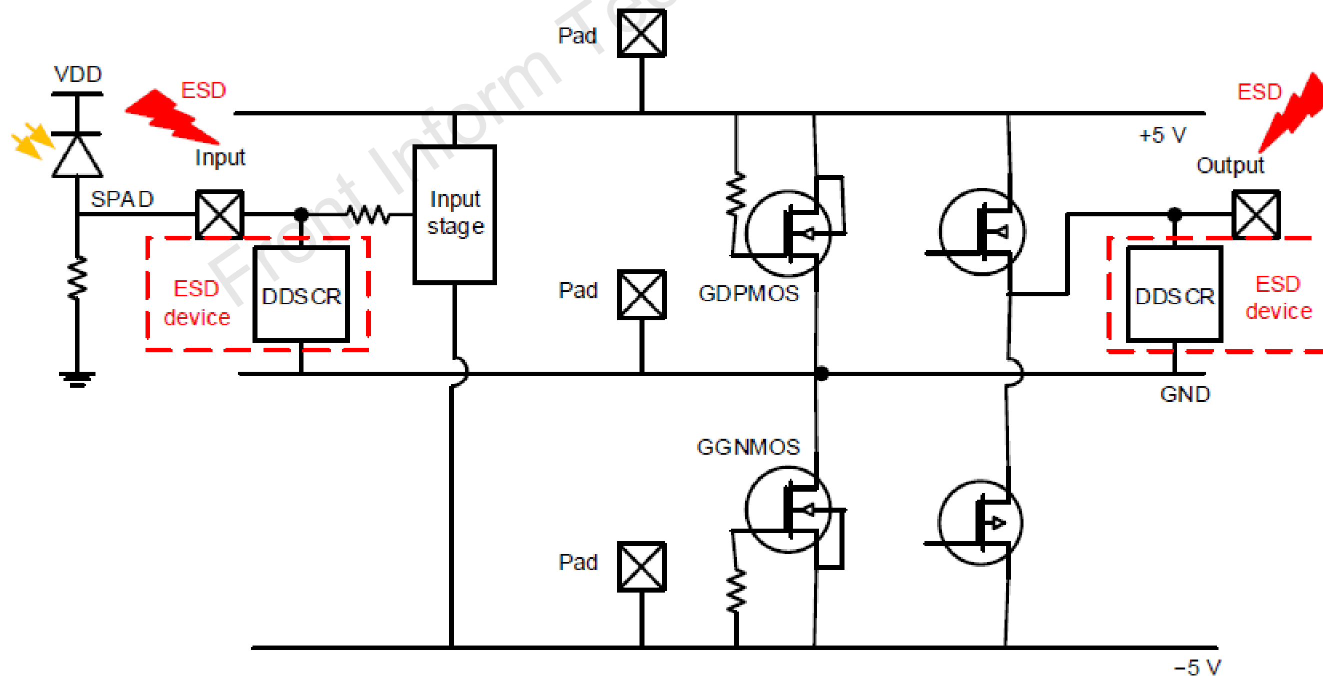
Method

1. The protection level of traditional electro-static discharge (ESD) protection devices is between 2 kV and 8 kV. When industry-grade fluorescent optical fiber temperature sensors work in extreme outdoor environments, it is difficult for traditional ESD devices to resist ESD pulses higher than 8 kV, and they cannot ensure the reliability and stability of the sensors.



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Method (Cont'd)

2. Principle analysis of NBL-GCSCR and DNW-GCSCR

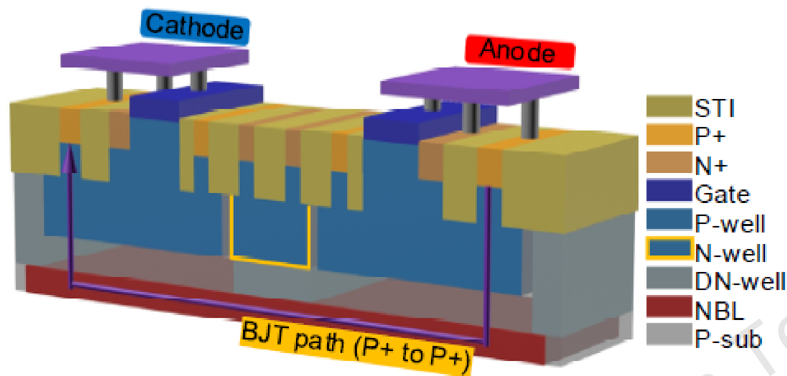
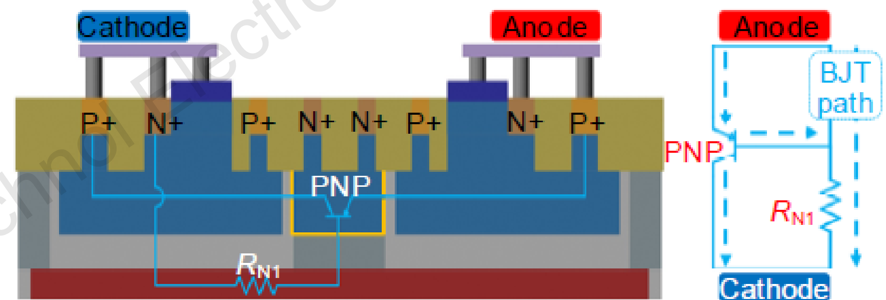


Fig. 3 Cross section of basic NBL-GCSCR



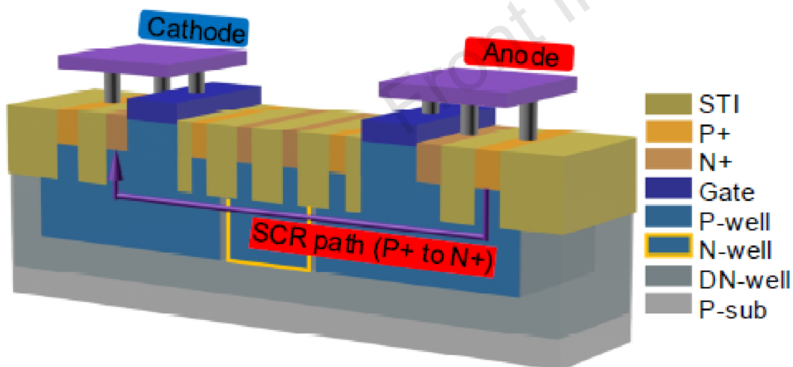


Fig. 4 Cross section of optimized DNW-GCSCR

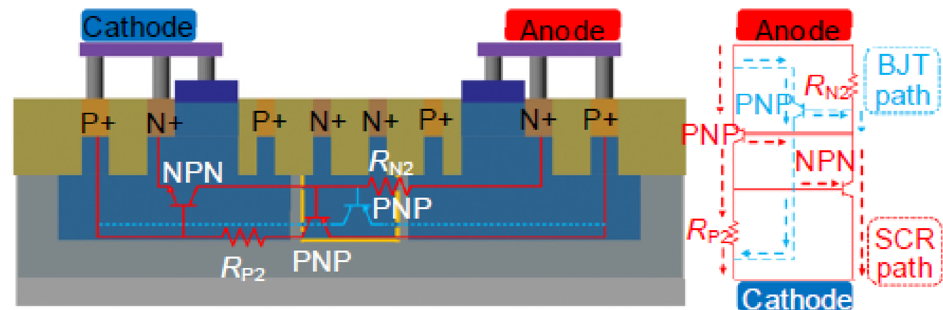


Fig. 6 The basic NBL-GCSCR actual equivalent circuit (a) and optimized DNW-GCSCR actual equivalent circuit (b)

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Method (Cont’d)

3. Technology computer-aided design (TCAD) is used to perform a DC scan of the device. The initial scan point and the progressive step size are set, and the DC simulation results of the device are obtained when the current scan is stopped to 1 mA.

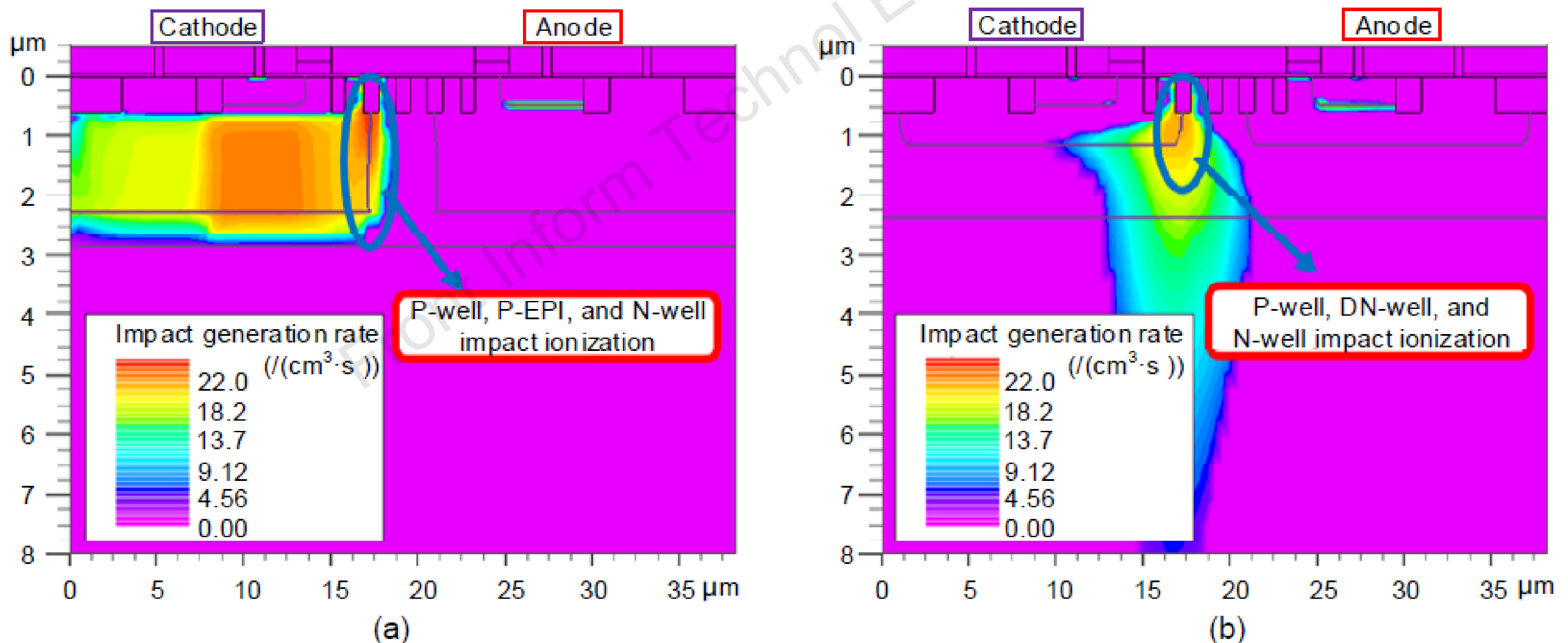

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Fig. 7 Impact ionization of NBL-GCSCR (a) and DNW-GCSCR (b)

Method (Cont'd)

4. To further verify the ESD principle of the device, TLP simulation is used to analyze its ESD behavior. A simulation of the global device temperature and time (2.0×10^{-14}–1.2×10^{-7} s) is conducted for both types of device at a transient current of 10 mA.

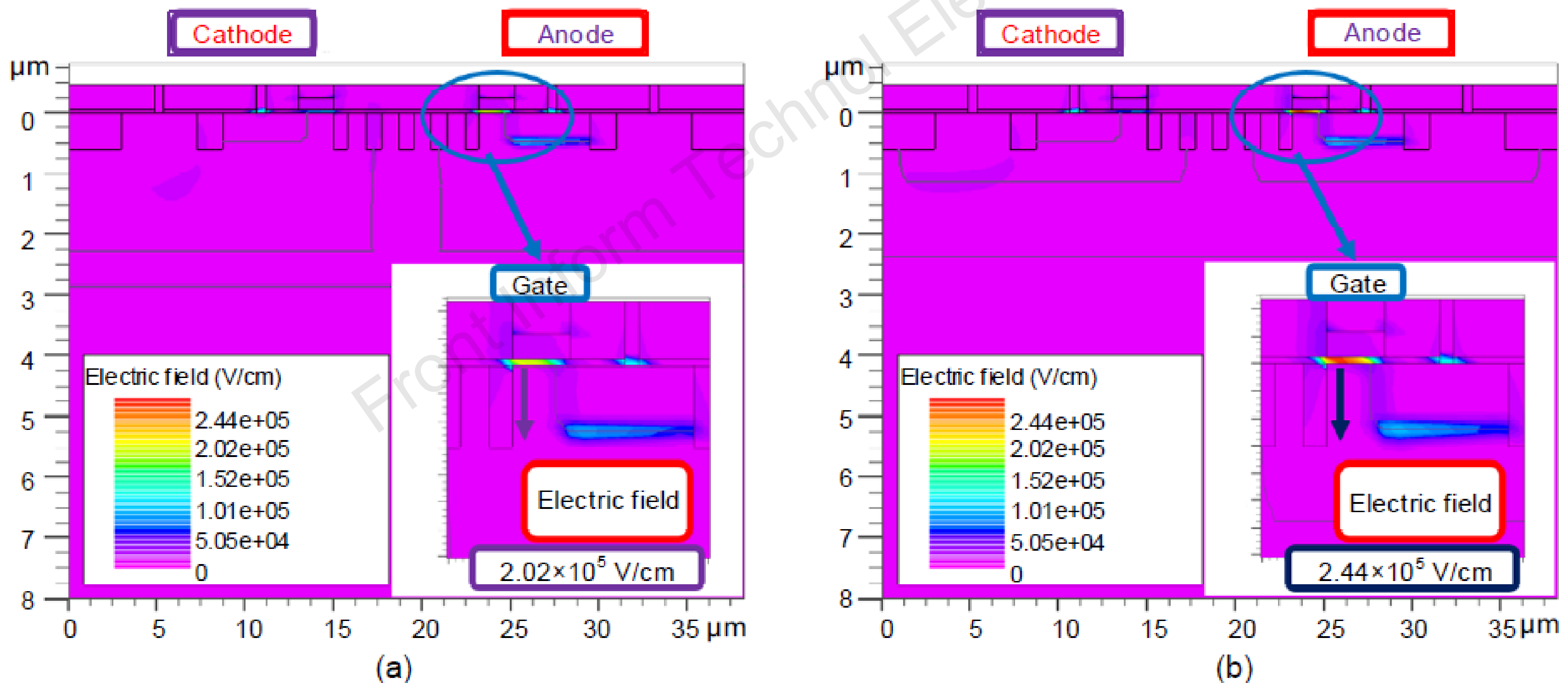

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Fig. 9 The electric field distribution when NBL-GCSCR (a) or DNW-GCSCR (b) is fully turned on

Major results

DC *I-V* curves, response time, and turn-on time curves

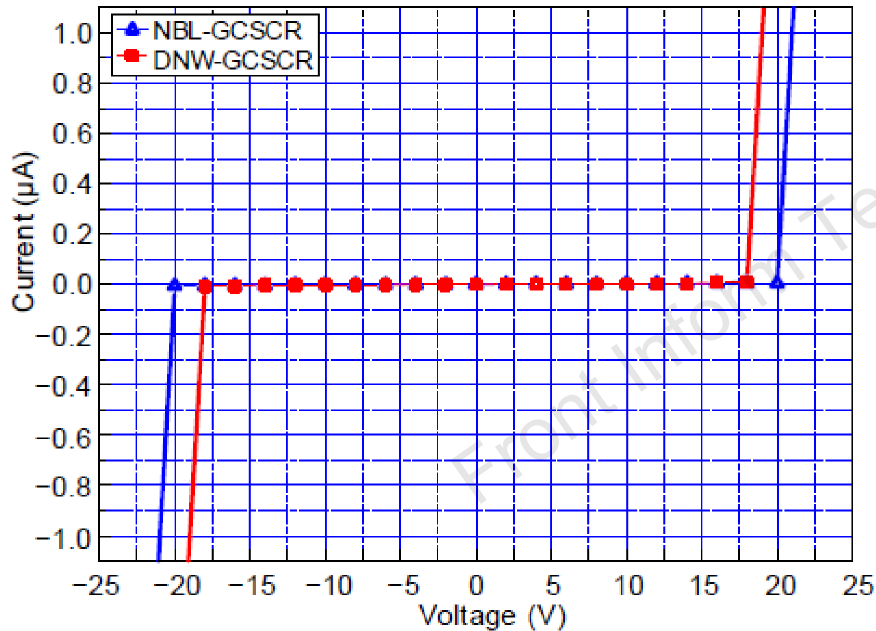

Fig. 16 DC *I-V* curves of 8-finger basic NBL-GCSCR and optimized DNW-GCSCR

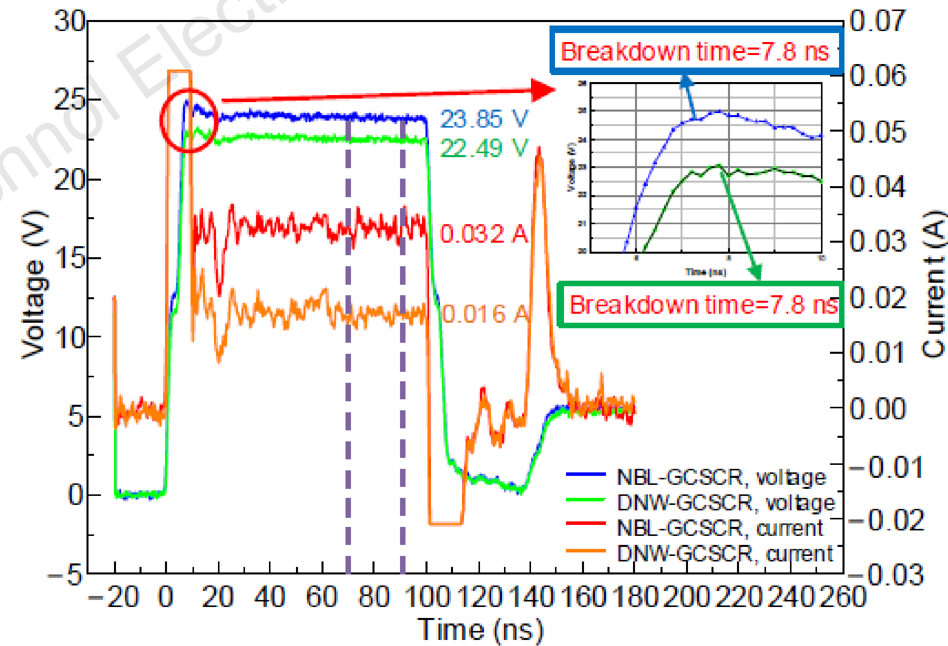

Fig. 17 Response time and turn-on time curves of 8-finger basic NBL-GCSCR and optimized DNW-GCSCR

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Major results (Cont'd)

TLP *I-V* curves

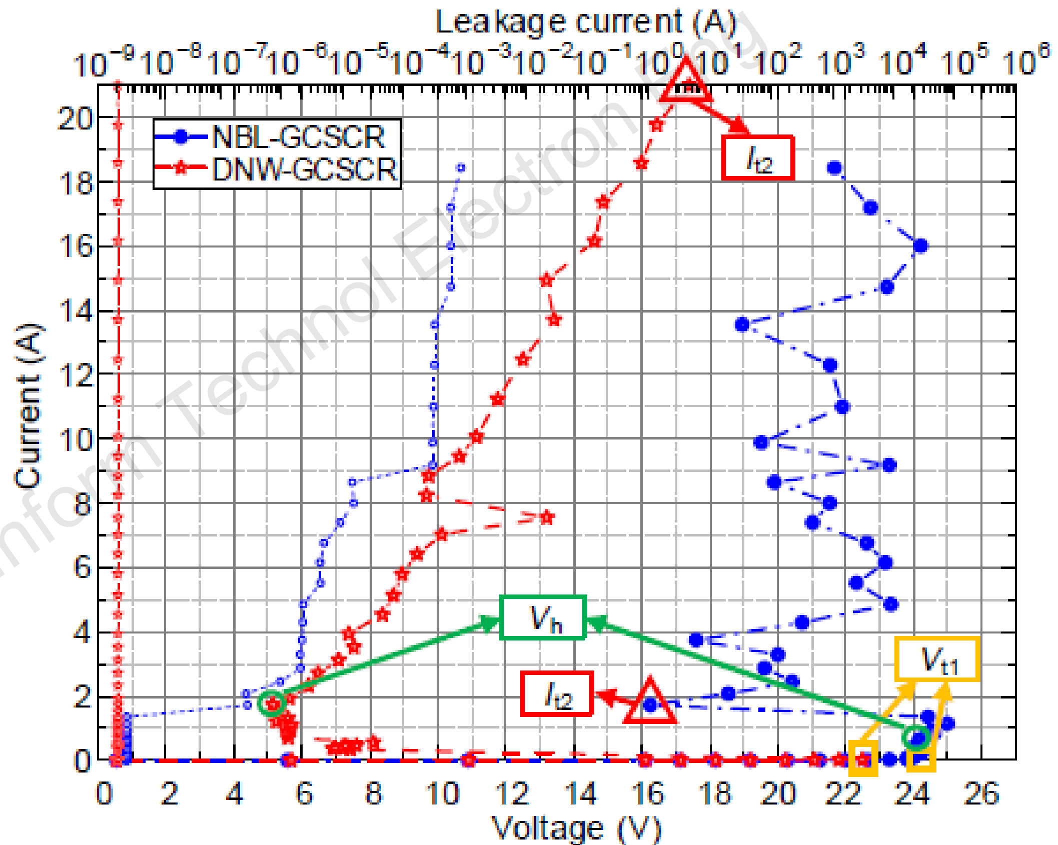

Fig. 18 TLP *I-V* curves of 8-finger basic NBL-GCSCR and optimized DNW-GCSCR

Major results (Cont'd)

TLP *I-V* curves

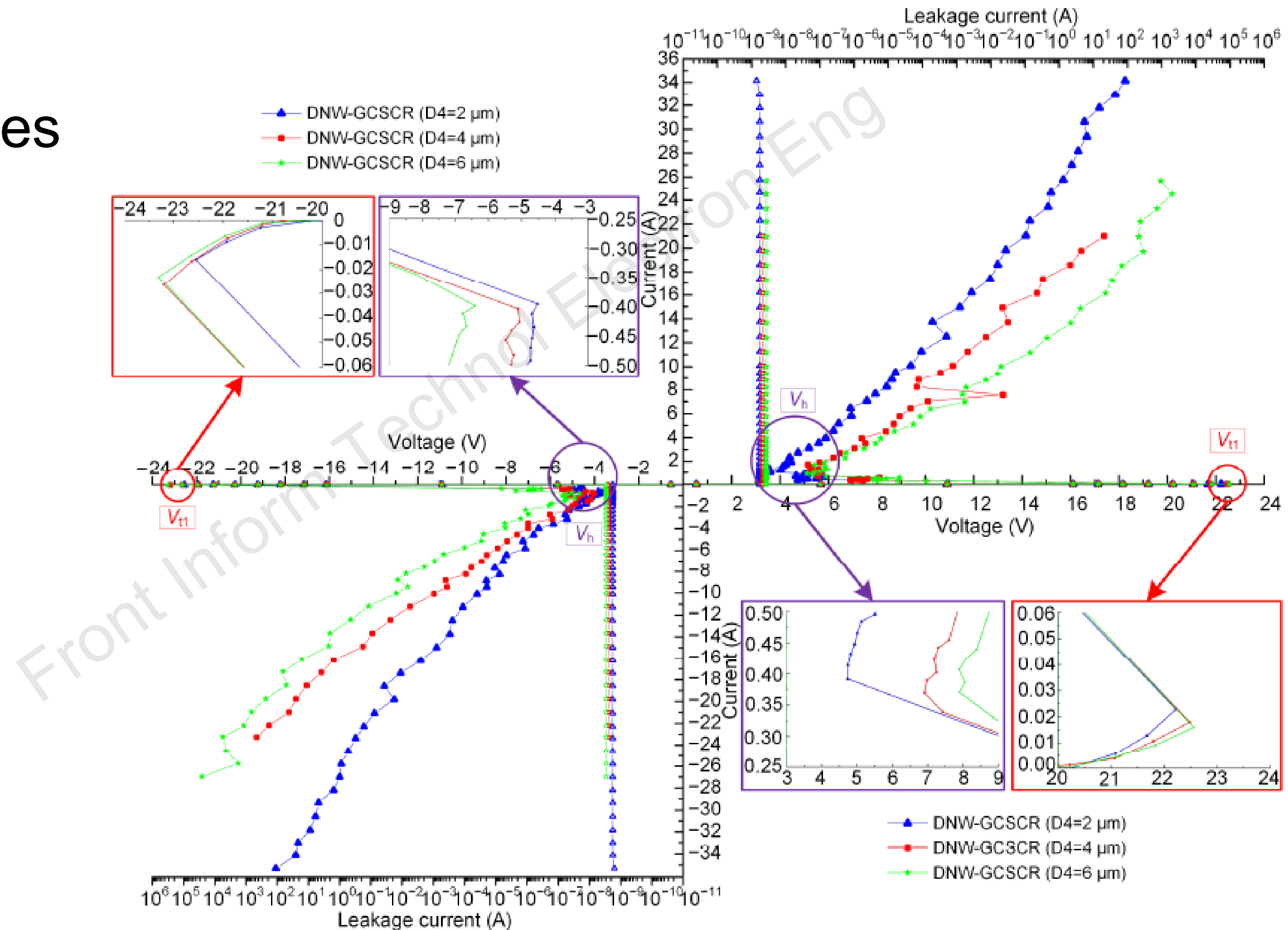

Fig. 19 TLP *I-V* curves of 8-finger optimized DNW-GCSCR (D4=2, 4, 6 μm)

Conclusions

1. The holding voltage (24.03 V) of NBL-GCSCR with the longitudinal bipolar junction transistor (BJT) path is significantly higher than the holding voltage (5.15 V) of DNW-GCSCR with the lateral SCR path of the same size.

2. When the gate size of DNW-GCSCR is increased from 2 to 6 μm, the holding voltage is increased from 3.50 to 8.38 V. The optimized DNW-GCSCR with a gate size of 6 μm can be stably applied on target readout circuits for on-chip electrostatic discharge protection.

3.The results of two-dimensional simulation and a TLP test show that the electric field effect of the gate significantly affects the ESD parameters of the device.

4. In a harsh environment with strong electrostatic interference, the DNW-GCSCR device can provide a solution to the on-chip ESD protection of the signal readout circuit of industry-level fluorescence detection technology.

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