Hongchen CHEN, Haoshen ZHU, Liang WU, Wenquan CHE, Quan XUE, 2021. A 9.8–30.1 GHz CMOS low-noise amplifier with a 3.2-dB noise figure using inductor- and transformer-based g_m-boosting techniques. *Front Inform Technol Electron Eng*, 22(4):586-598. https://doi.org/10.1631/FITEE.2000510

A 9.8–30.1 GHz CMOS low-noise amplifier with a 3.2-dB noise figure using inductor- and transformer-based g_m-boosting techniques

Key words: CMOS; g_m-boosting; Low-noise amplifier; Transformer; Common-gate

Corresponding author: Quan XUE
E-mail: eeqxue@scut.edu.cn
ORCID: https://orcid.org/0000-0002-4226-2127

Motivation

1. With the stimulation of multiband, multi-standard, and ultrawideband (UWB) radios, wideband receivers are highly required because of low cost, low power, and high flexibility.

2. In wideband receiver, wideband low-noise amplifier (LNA) is a critical block that receives small signals from the antenna and then amplifies them with a good signal-to-noise ratio (SNR).

3. CMOS is a competitive technology due to the high level of integrability and low cost. Thus, wideband CMOS LNAs with excellent performance are highly desirable.

Main idea

1. A topology based on common-gate (CG) cascading with a common-source (CS) amplifier is proposed for simultaneous wideband input matching and relatively high gain.

2. The inductor- and transformer-based g_m-boosting techniques are employed to enhance the gain and reduce the power consumption.

3. A 9.8–30.1 GHz LNA with a 3.2-dB minimum noise figure (NF) is designed and fabricated in the 65-nm CMOS process.

Method

1. In the CG stage, loading effect is used instead of the conventional feedback technique, to enable simultaneous impedance and noise matching.

2. Based on in-depth theoretical analysis, the inductor- and transformer-based g_m-boosting techniques are employed for the CG and CS stages, respectively, to enhance the gain and reduce the power consumption.

3. The floating-body method, which was originally proposed to lower NF in CS amplifiers, is adopted in the CG stage to further reduce NF.

Schematic and chip photo

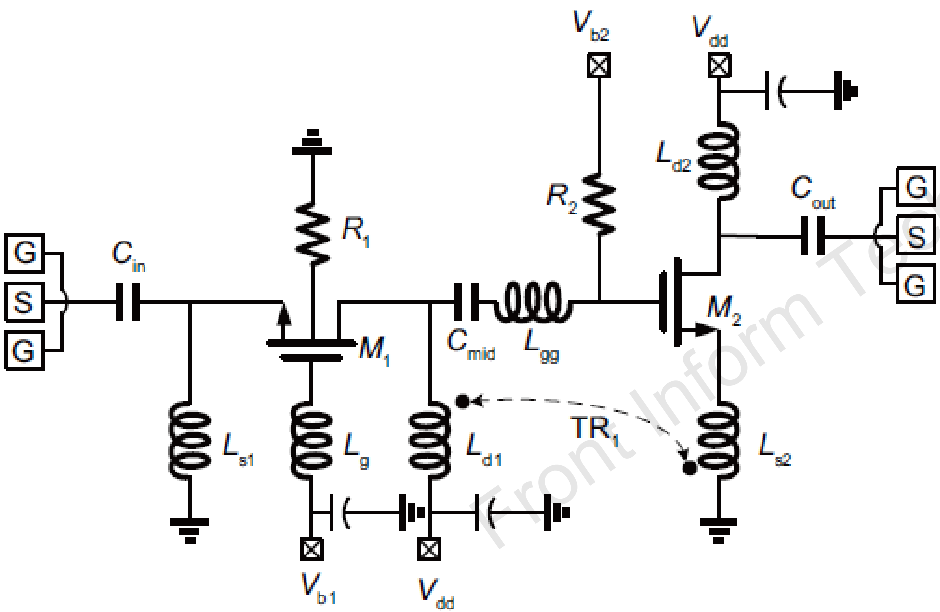

Fig. 9 Schematic of the proposed CG-CS LNA

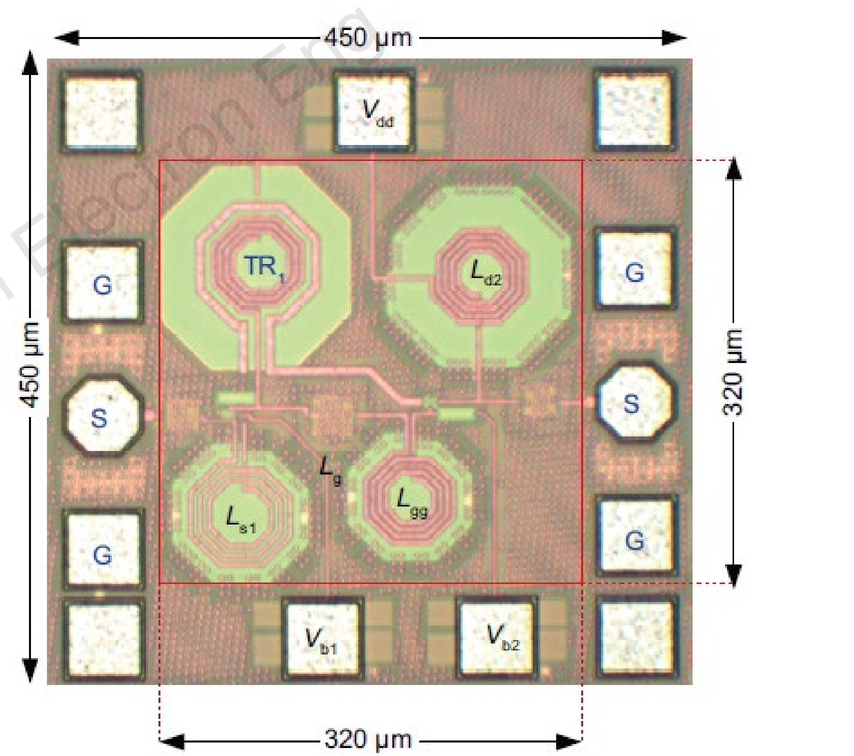

Fig. 14 Die photograph of the fabricated wideband LNA

Measurement and comparison

Table 3 Performance summary of state-of-the-art LNAs and this work

Reference	BW_1 (GHz)		BW_2 (GHz)		Peak gain (dB)	Size (mm^2)	P_{dc} (mW)	NF (dB)
Qin and Xue (2017a)	15.8–30.3	14.5	18–29.5	11.5	10.2	0.18	12.4	3.3–5.7
Qin and Xue (2017b)	7.6–29	21.4	8–12.5&20.5–24	8	10.7	0.30	12.1	4.5–5.6
Li CJ et al. (2018)	14–31	17	26–28	2	12.8	0.30	15	1.3–1.6
Cui and Long (2020)	19–36	17	22–32	10	21.5	0.17	17.3	1.7–2.2
This work	**9.8–30.1**	**20.3**	**14–40**	**26**	**10.9**	**0.20**	**15.6**	**3.2–5.7**

Reference	IIP3@freq (dBm@GHz)	BW_{eff} (GHz)		Process	FoMI	FoMII
Qin and Xue (2017a)	−0.5@22	18–29.5	11.5	65 nm CMOS	8.8	18.1
Qin and Xue (2017b)	1.4@21.5	8–12.5&20.5–24	8	65 nm CMOS	1.9	13.4
Li CJ et al. (2018)	4@24	26–28	2	45 nm CMOS SOI	4.4	21.8
Cui and Long (2020)	−13.4@22	22–32	10	22 nm FD SOI	23.1	10.2
This work	**1.39@25**	**14.1–30.1**	**26**	**65 nm CMOS**	**10.4**	**22.3**

BW_1: −3 dB gain bandwidth; BW_2: −10 dB input matching bandwidth; BW_{eff}: overlapping bandwidth of BW_1 and BW_2. P_{dc}: DC power consumption. The results of this work are in bold

Conclusions

1. A wideband LNA fabricated in 65-nm CMOS was proposed with the highest FoMII, competitive linearity, and wide bandwidth.

2. Better tradeoff among the input matching, NF, and gain in the CG stage was achieved using loading effect.

3. To enhance the gain, the inductor- and transformer-based g_m-boosting techniques were analyzed in detail and adopted in this design.

Quan XUE is a professor at South China University of Technology. He received his BS, MS, and PhD degrees in electronic engineering from the University of Electronic Science and Technology of China, Chengdu, China, in 1988, 1991, and 1993, respectively. His research interests include microwave/millimeter-wave/THz passive components, active components, antenna, microwave monolithic integrated circuits, and radio frequency integrated circuits.