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# Cellular automata based multi-bit stuck-at fault diagnosis for resistive memory

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**Key words:** Resistive memory; Cell reliability; Stuck-at fault diagnosis; Single-length-cycle single-attractor cellular automata; Single-length-cycle two-attractor cellular automata; Single-length-cycle multiple-attractor cellular automata

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# Motivation

1. Chip multiprocessors (CMPs) can be more convenient for various latency- and throughput-sensitive applications, if and only if they are well-equipped with appropriate memory subsystems. To achieve optimized performance benefits, proper speedup, and required parallelism in CMPs, architecture to memory technology must be properly tuned into the chip floor area and power budget. Large-size on-chip cache is preferred to off-chip cache of CMPs.

2. Traditional static random-access memory, dynamic random-access memory, NAND, and NOR flash memory are limited by their scalability, power, package density, and so forth. Next-generation memory types like ReRAMs are considered to have various advantages such as high package density, non-volatility, scalability, and low power consumption. They are also preferred for on-chip cache construction.

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# Motivation

3. However, cell reliability has been a problem in ReRAM. Unreliable memory operation is caused by permanent stuck-at faults due to extensive use of write- or memory-intensive workloads. An increased number of stuck-at faults also prematurely limit chip lifetime.

4. Fault-tolerant designs are proposed with the approach by which faulty cells can still be usable and exact readable data can also be obtained from the faulty cells. Cellular automaton (CA) based schemes are found in different applications of homogeneous or heterogeneous CMPs.

5. Hardware-based fault-tolerant schemes are complementary to wear-leveling schemes. Cell lifetime reliability and variability can also be addressed by an efficient fault-tolerant design.

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# Main idea

1. A cellular automaton (CA) based dynamic stuck-at fault-tolerant design is proposed here to combat unreliable cell functioning and variable cell lifetime issues. A scalable, block-level fault diagnosis and recovery scheme is introduced to ensure readable data despite multi-bit stuck-at faults.

2. The proposed scheme is based on Wolfram's null boundary and periodic boundary CA theory. Various special classes of CAs are introduced for 100% fault tolerance: single-length-cycle single-attractor cellular automata (SACAs), single-length-cycle two-attractor cellular automata (TACAs), and single-length-cycle multiple-attractor cellular automata (MACAs). The target micro-architectural unit is designed with optimal space overhead.

3. The scheme removes all the restrictions on the number and nature of stuck-at faults in general fault conditions and is proved more advantageous than the state-of-the-art fault-tolerant designs.

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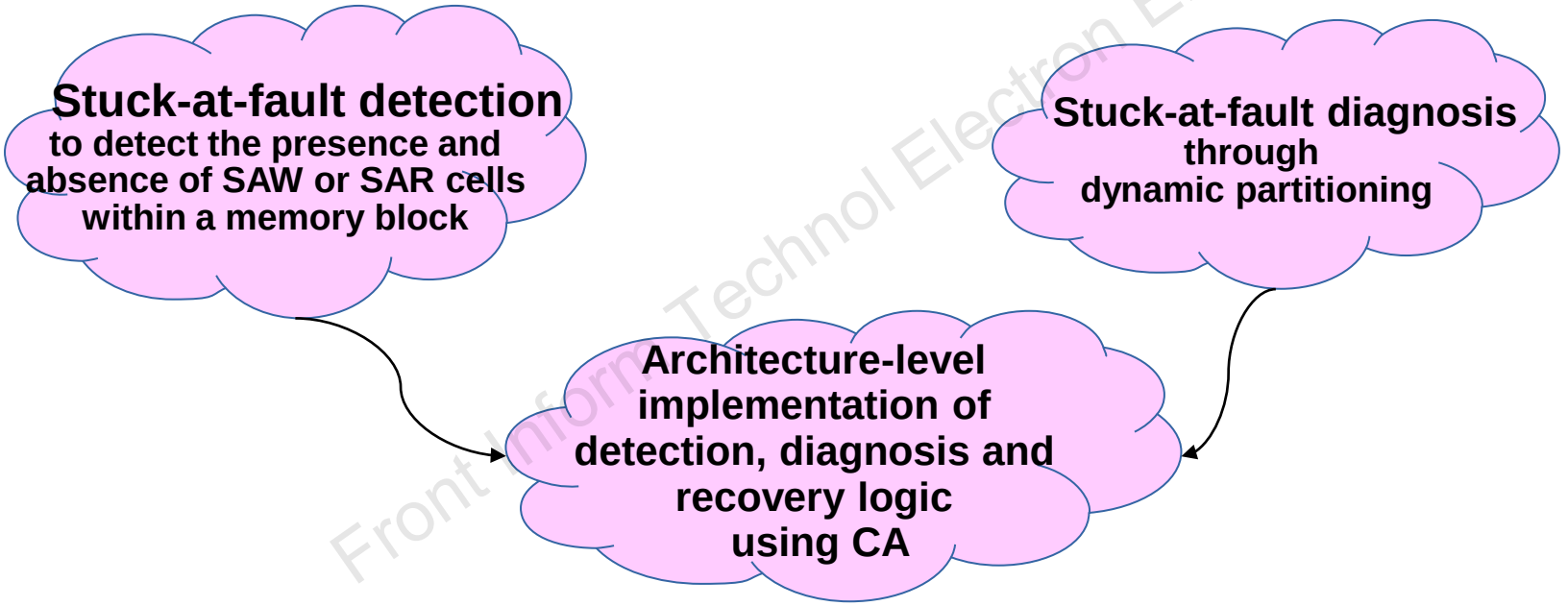
# Main idea

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**Fault-tolerant system design approach**

# Major contributions

**Contribution 1**: Nonuniform null boundary cellular automata (SACA & TACA) based fault-tolerant circuit design for resistive memory

**Contribution 2**: Uniform null boundary (TACA & MACA) and periodic boundary cellular automata (TACA) based fault-tolerant circuit design for resistive memory

**Contribution 3**: Cellular automata based multi-bit stuck-at fault diagnosis circuit design through recursive partitioning for resistive memory using nonuniform null boundary CA

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# Detailed contributions

1. A CA-based simple and efficient test architecture is designed to ensure 100% fault tolerance against permanent stuck-at faults.

2. Uniform and nonuniform SACA, TACA, and MACA rules are synthesized in alternate fault detection design solutions.

3. The presence of SAW and SAR cells in the same memory block in complex fault conditions is handled. Theoretically, it does not impose any limitation on the number or the nature of tolerable faults.

4. Unique periodic boundary TACA based and null boundary SACA based test architectures are employed in multi-bit fault diagnosis.

5. The design can diagnose a huge number of faults using recursive partitioning logic that is suitable for any block size. Space overhead is also reduced with increased block size in complete system design.

6. Simple but effective data recovery logic is used to provide readable data in spite of stuck-at faults at multiple bits within a memory block.

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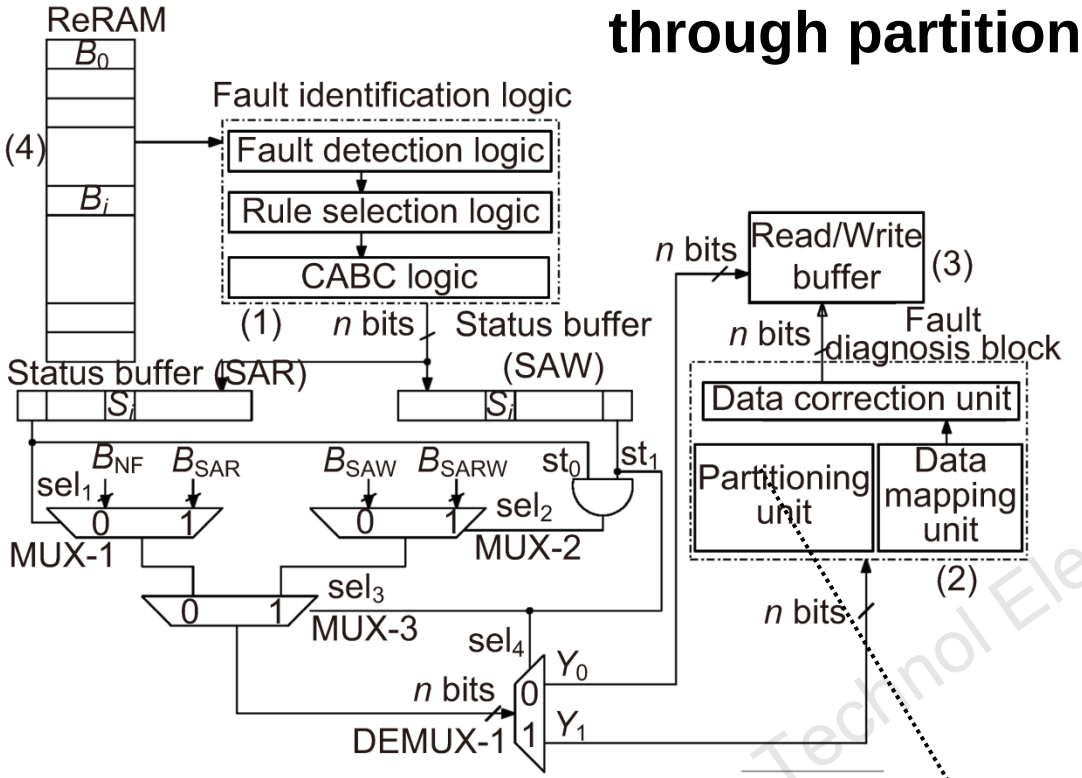
# System description of the fault diagnosis scheme through partitioning

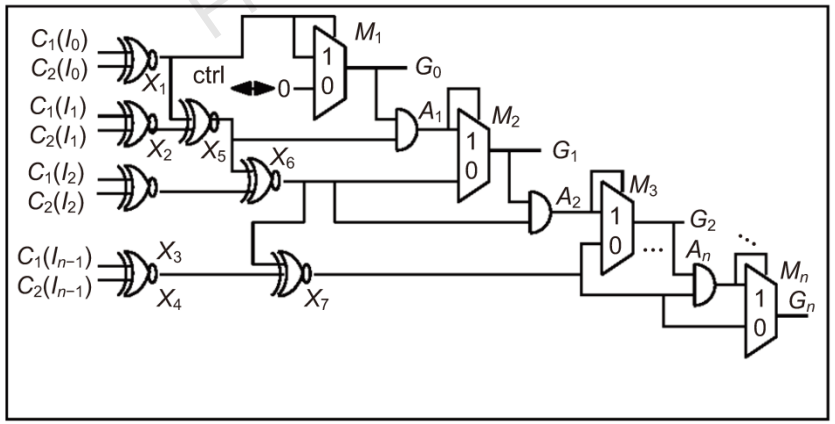



Subunits are:

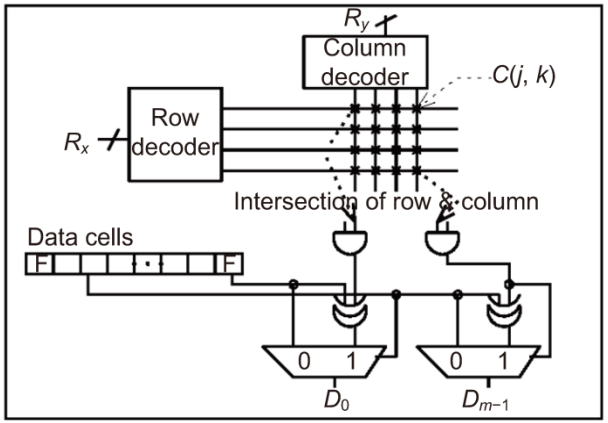
- Fault identification logic
  - Fault detection logic
  - Nonuniform rule set logic
  - Memory block categorisation
- Fault diagnosis unit
  - Recursive partitioning
- Data mapping
- Read/write buffer
- Data correction unit

Identification of the fault status of the memory block for (1) $B_{NF}$-NF cells only, (2) $B_{SAW}$-SAW/NF cells and no SAR cell, (3) $B_{SAR}$-SAR & NF cells and no SAW cell, and (4) $B_{SARW}$-SAW/SAR/NF cells

Block diagram of multi-bit stuck-at fault-tolerant design using the partitioning technique




(a) Group discriminator logic




(b) Data correction logic

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# Fault detection logic

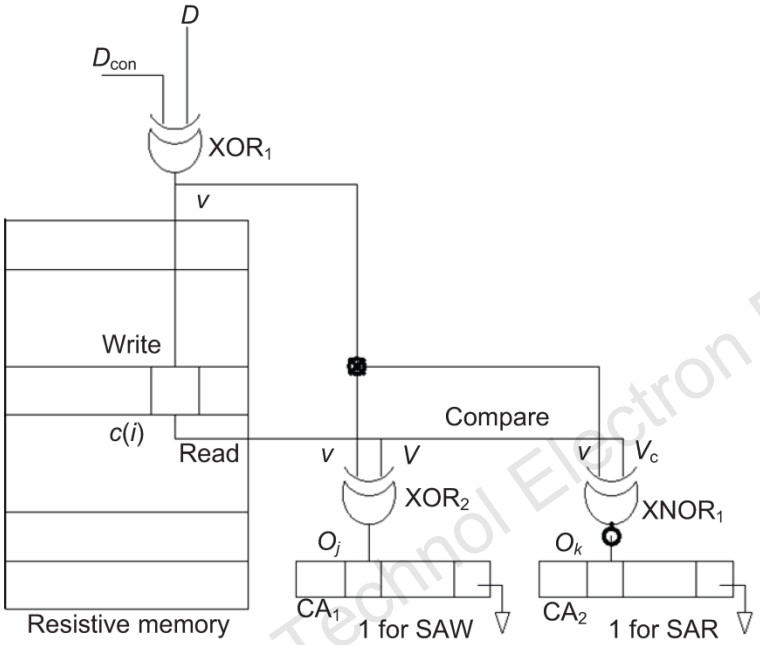


**Fig. 4 Identification of the fault status of the memory block (Sarkar et al., 2017)**

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**Table 2 Tabular representation of fault-tolerant design steps**

| Input data | | | Cell status | Retrieved data | | Comparative result | | Decision | |
|---|---|---|---|---|---|---|---|---|---|
| $D$ | $D_{\text{con}}$ | $v$ | $c(i)$ | $V$ | $V_{\text{c}}$ | $\text{XOR}_2$ $(O_j)$ | $\text{XNOR}_1$ $(O_k)$ | SAR/NF | SAW |
| 0 | 0 | 0 | S-A-0 & NF | 0 | – | 0 | – | SAR/NF | – |
| 0 | 0 | 0 | S-A-1 | 1 | – | 1 | – | – | SAW |
| 0 | 1 | 1 | S-A-0 | – | 0 | – | 0 | SAR | – |
| 0 | 1 | 1 | NF | – | 1 | – | 1 | NF | – |
| 1 | 0 | 1 | S-A-1 & NF | 1 | – | 0 | – | SAR/NF | – |
| 1 | 0 | 1 | S-A-0 | 0 | – | 1 | – | – | SAW |
| 1 | 1 | 0 | S-A-1 | – | 1 | – | 0 | SAR | – |
| 1 | 1 | 0 | NF | – | 0 | – | 1 | NF | – |

# Major results

**Table 4 Tabular representation of fault detection with a nonuniform NBCA rule pair (254, 255)**

| Status register | | Rule vector | | T state | | st | | Block state |
|---|---|---|---|---|---|---|---|---|
| Status word 1 | Status word 2 | $RCA_1$ | $RCA_2$ | $t_1$ | $t_2$ | (0) | (1) | |
| 0 0 0 0 | 0 0 0 0 | 254 254 254 254 | 254 254 254 254 | 1 | 1 | 0 | 0 | $B_{NF}$ |
| 0 0 0 0 | 1 0 0 1 | 254 254 254 254 | 255 254 254 255 | 1 | 2 | 0 | 1 | $B_{SAR}$ |
| 1 0 0 1 | 0 0 0 0 | 255 254 254 255 | 254 254 254 254 | 2 | 1 | 1 | 0 | $B_{SAW}$ |
| 1 1 0 0 | 0 1 1 0 | 255 255 254 254 | 254 255 255 254 | 2 | 2 | 1 | 1 | $B_{SARW}$ |

**Table 6 Comparative state analysis report of fault detection with various uniform CA rules**

| CA type | Rule | CA attractors | | State | | Status bit | | Depth | $M_p$ (%) |
|---|---|---|---|---|---|---|---|---|---|
| | TACA, MACA | $A_{ttr1}$ | $A_{ttr2,3,4}$ | Other basins | basin-0 | $st_0$ | $st_1$ | | |
| PBCA | $R_{238}$ | 0→0 | 15→15 | 1–15 | 0 | 0 | 1 | 3 | 0 |
| PBCA | $R_{252}$ | 0→0 | 15→15 | 1–15 | 0 | 0 | 1 | 3 | 0 |
| NBCA | $R_{116}$ | 0→0 | 1→1 | 1–15 | 0 | 0 | 1 | 3 | 0 |
| NBCA | $R_{244}$ | 0→0 | 1→1 | 1–15 | 0 | 0 | 1 | 4 | 0 |
| NBCA | $R_{212}$ | 0→0 | 1→1, 5→5 | 1–15 | 0 | 0 | 1 | 4 | 0 |
| NBCA | $R_{222}$ | 0→0 | 11→11, 13→13, 15→15 | 1–15 | 0 | 0 | 1 | 3 | 0 |

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# Performance analysis

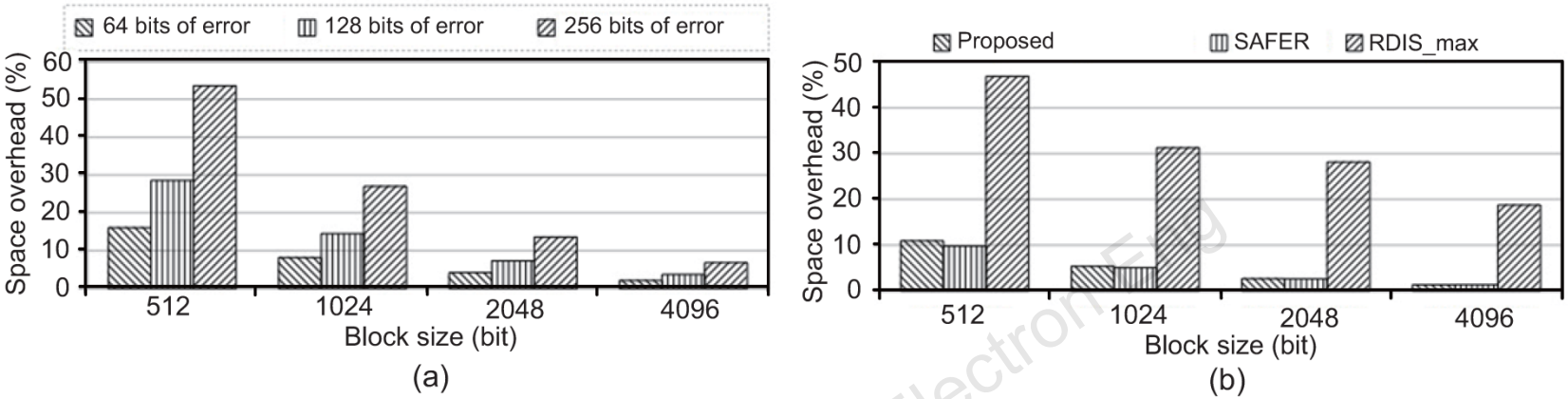


**Fig. 14** Space overhead vs. the number of tolerable faults (a) and comparison with RDIS and SAFER (b)

Overhead is sensitive to the **number of faults** and **block size**. It is compared with state-of-the-art designs based on dynamic partitioning schemes **RDIS and SAFER**.

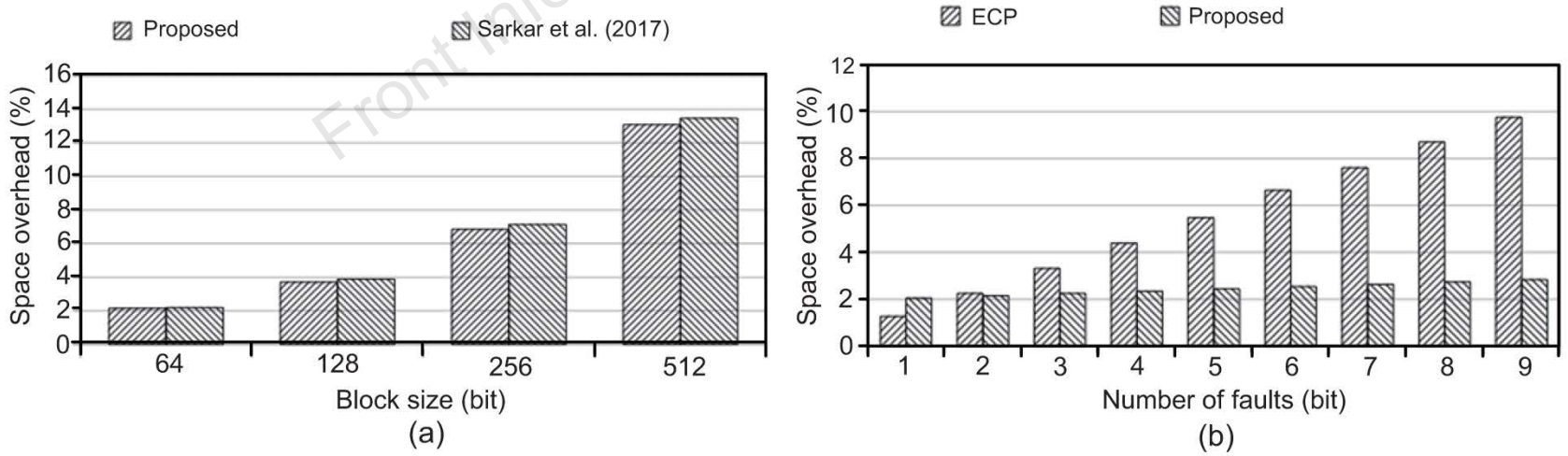


**Fig. 15** Space overhead comparison with Sarkar et al. (2017)'s scheme (a) and ECP-based scheme (b)

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# Conclusions

1. Unreliable cell operation due to multi-bit stuck-at faults limits the application of ReRAMs in CMPs. The proposed scheme assures 100% fault tolerance in spite of spatially scattered complex multi-bit stuck-at faults.

2. Because it is a runtime strategy, it can also cope with the variable cell lifetime issue.

3. The recursive partitioning technique is used to diagnose SAW or SAR cells at block-level granularity. It is effective for general fault conditions and for any number of tolerable faults.

4. The unique CA based test architecture increases the simplicity and flexibility in the design and implementation stages of detection and/or diagnosis.

5. An optimized design solution using alternate CA rules reduces the space overhead in spite of increasing the block size.

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