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Introducing scalable 1-bit full adders for designing quantum-dot cellular automata arithmetic circuits

Key words: Quantum-dot cellular automata (QCA); Full adder; Ripple carry adder (RCA); Add/sub circuit; Multiplier

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Motivation

1. Nanotechnology has made a lot of progress in the field of integrated circuit fabrication. Many innovative methods and technologies have been engendered. The process of scaling down the feature size of transistors in standard complementary metal-oxide-semiconductor (CMOS) technology has become more arduous in the last few years. Deep sub-micron undesirable responses in CMOS make alternative solutions more attractive.

2. Quantum-dot cellular automata (QCA) is of great renown. The remarkable energy consumption compared to the standard CMOS is of great interest. The QCA's superiorities are the operating speed at the order of THz, high device density, ultra-low energy dissipation, and considerable flexibility for scaling down the minimum cell size to the dimensions of atoms.

Motivation (Cont’d)

3. A full adder is a rudimentary element of arithmetic systems. Designing an optimized full adder structure is essential for designing related intricate circuits because full adders are used extensively in larger circuits, such as multipliers. Also, adder and subtractor circuits with more entry bits need more full adder blocks in their structures.

Main idea

1. The full adder is a digital arithmetic block with three input variables (A, B, C_{in}) and two outputs (Sum, C_{out}).

2. A half subtractor can be constructed from a full adder if the second operand (second input's digits) are inverted and the carry input is set to 1.

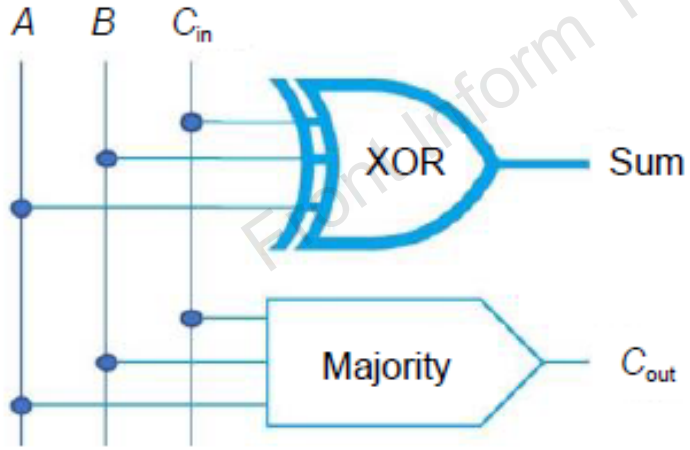


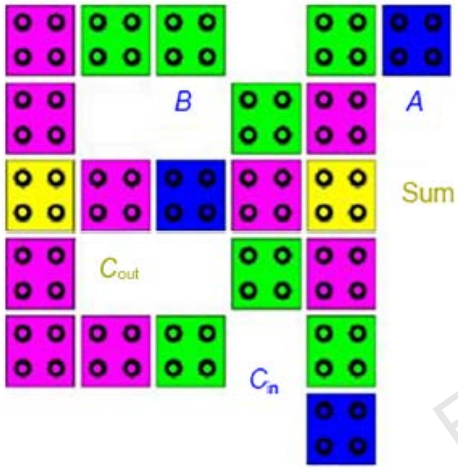
Fig. 6 Logical diagram of a 1-bit full adder block

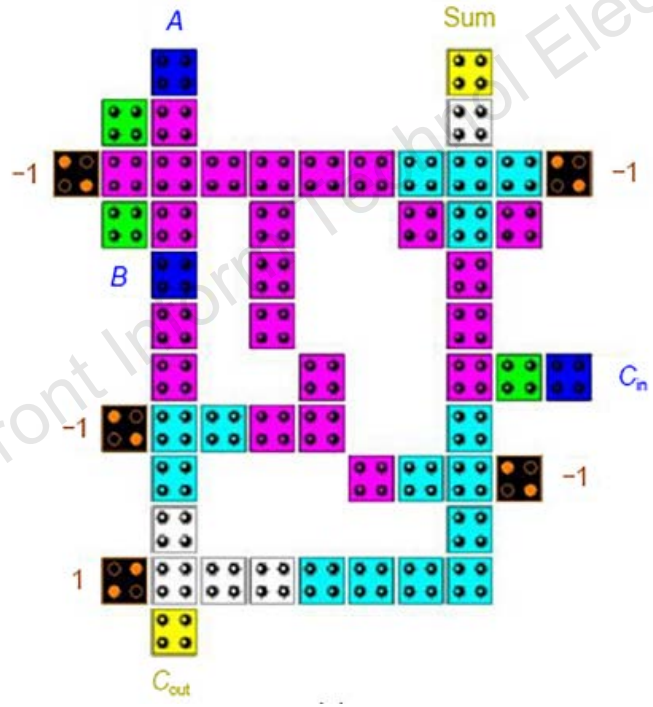
$$\text{Sum} = A \oplus B \oplus C_{in}, \quad (2)$$

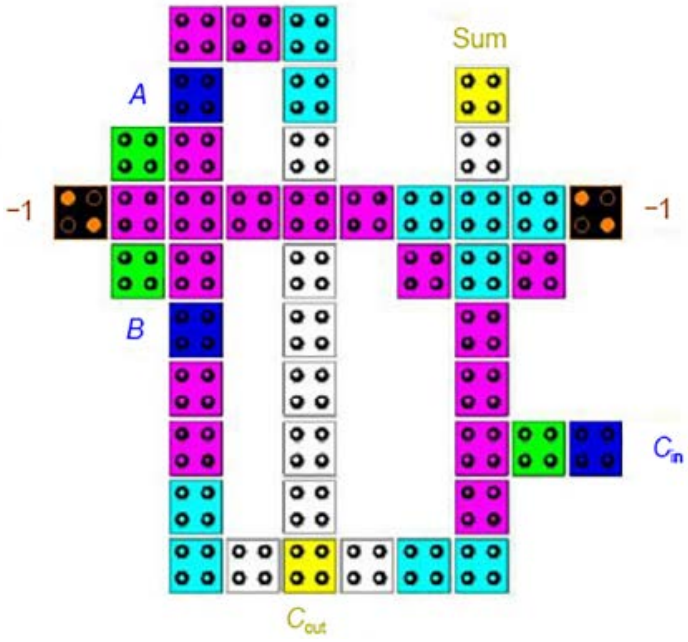
$$C_{out} = AB + C_{in}(A \oplus B) = \mathbb{M}(A,B,C_{in}). \quad (3)$$

Main idea (Cont'd)

3. We have proposed three different 1-bit full adder architectures. These structures are designed on a single layer. In these designs, no coplanar crossovers were used, and none of the cells were shifted (translated).

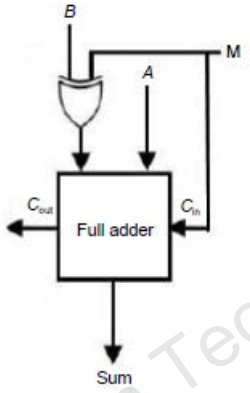




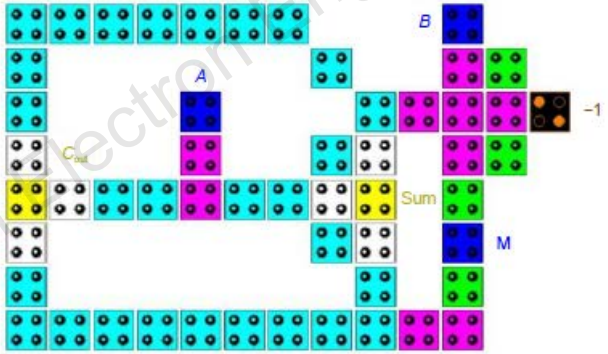


Proposed circuits

Add/Sub circuit: The add/sub circuit is a combinational logic circuit that can sum or subtract two *n*-bit numbers by setting a value (0 or 1) for the selector pin.

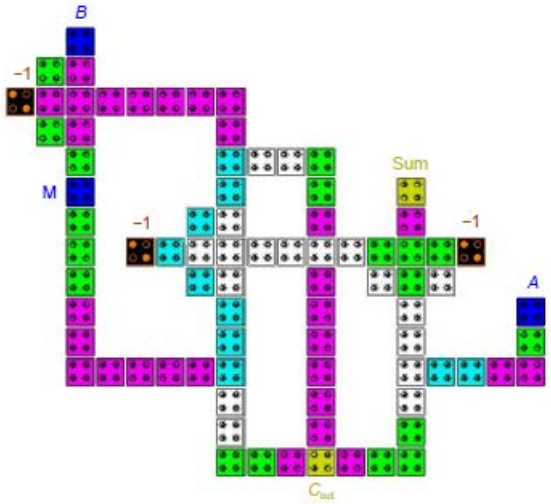


(a)



(b)

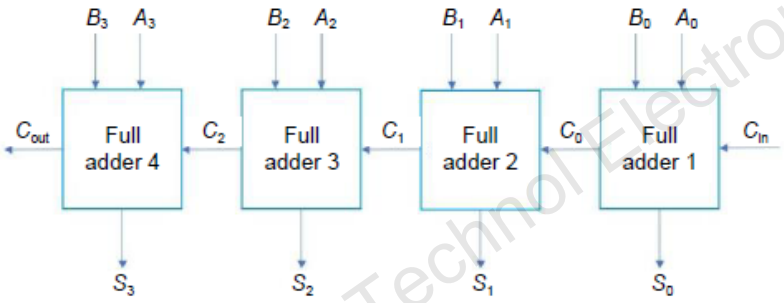
(c)



(d)

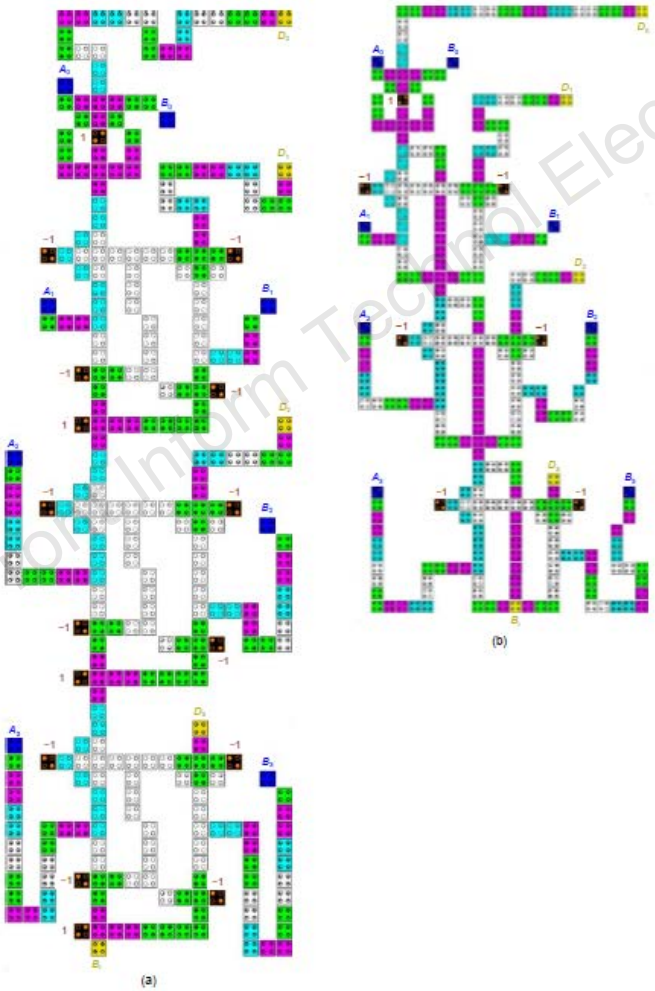
Proposed circuits (Cont'd)

4-bit ripple carry adder: The structure of the ripple carry adder is based on cascading multiple 1-bit full adders. So, an adder with a higher number of input bits will be acquired.



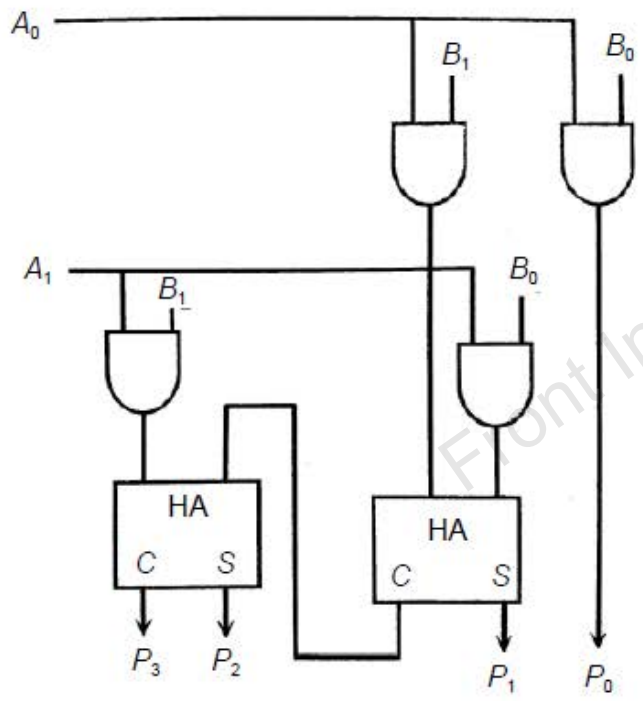
Proposed circuits (Cont'd)

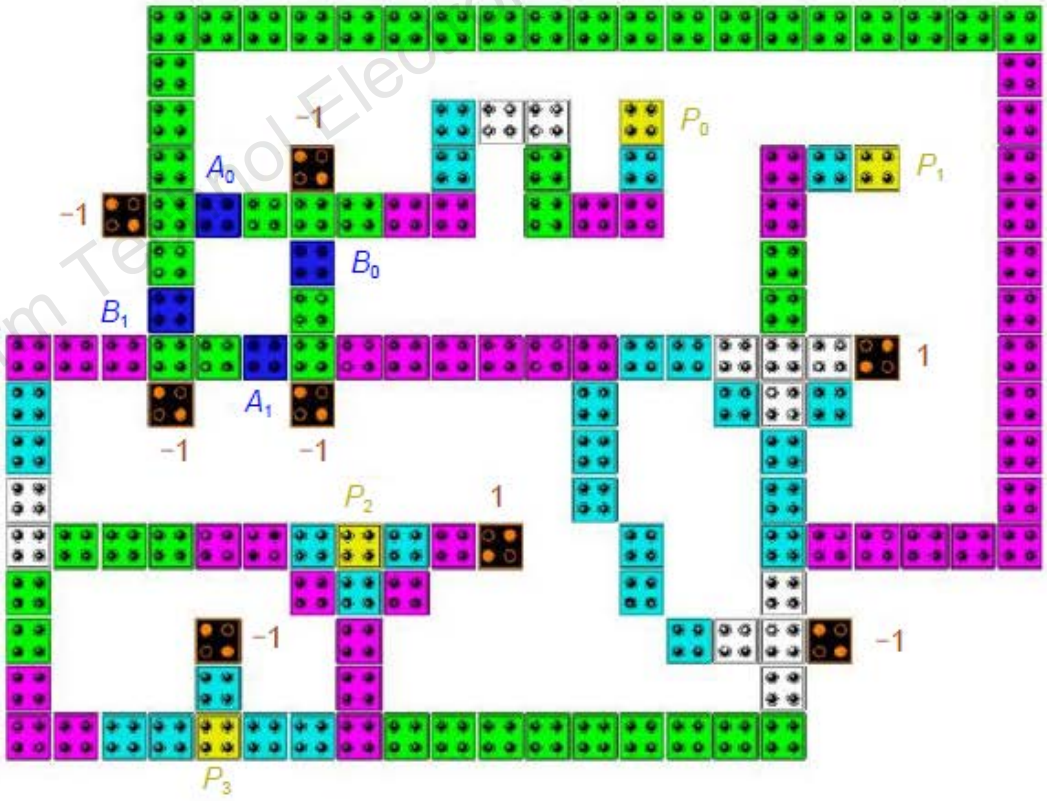
4-bit borrow subtractor: The structure base of the ripple borrow subtractor is the same as the ripple carry adder. A full adder block and a NOT gate are used to construct a subtractor



Proposed circuits (Cont'd)

2-bit array multiplier: An array multiplier is a combinational logic circuit used for multiplying two binary numbers by employing an array of AND gates and adders.





Major results

1. Simulation results of our proposed designs with QCA Designer-E version 2.2

Table 3 Performance evaluation of the proposed designs

Desgin	Number of cells	Delay (c.c)	Area (μm^2)	Sum_bath (eV)	Avg_bath (eV)	Sum_clk (eV)	Avg_clk (eV)
1-bit full adder 1	21	0.5	0.01	2.06e−2	1.87e−3	7.52e−4	6.83e−5
1-bit full adder 2	55	1	0.05	3.39e−2	3.09e−3	−1.72e−2	−1.60e−3
1-bit full adder 3	46	1	0.04	2.73e−2	2.48e−3	−2.80e−3	−2.55e−4
1-bit add/sub 1	53	1	0.04	3.15e−2	2.86e−3	−8.70e−3	−7.90e−4
1-bit add/sub 2	93	1.5	0.13	4.93e−2	4.48e−3	−2.96e−2	−2.70e−3
1-bit add/sub 3	83	1.5	0.11	3.90e−2	3.55e−3	−1.71e−2	−1.60e−3
4-bit RCA 1	331	3.5	0.38	1.44e−1	1.31e−2	−1.01e−1	−9.20e−3
4-bit RCA 2	309	3.5	0.44	1.14e−1	1.03e−2	−6.79e−2	−6.20e−3
4-bit RBS 1	332	3.5	0.38	9.83e−2	8.93e−3	−7.32e−2	−6.70e−3
4-bit RBS 2	310	3.5	0.44	9.02e−2	8.20e−3	−5.23e−2	−4.80e−3
2-bit array multiplier	145	1.75	0.14	6.28e−2	5.71e−3	−2.53e−2	−2.30e−3

RCA: ripple carry addrer; RBS: ripple borrow subtractor; (c.c): clock cycles

Major results (Cont'd)

2. Comparison results of our 1-bit full adders vs other designs

Table 4 Comparison of 1-bit QCA full adder designs

Reference	Number of cells	Delay (c.c)	Area (μm^2)	Total energy dissipation (eV)	Crossover	Scalability	Connectivity	Cost Eq. (7)	Cost Eq. (8)
Abdullah-Al-Shafi and Bahar, 2018	28	0.5	0.02	2.10e−2	Not required	×	√	0.005	3.25
Balali and Rezai, 2018	39	1	0.04	3.51e−2	Logical crossing	√	×	0.04	11
Heikalabad et al., 2018	41	1	0.03	3.48e−2	Not required	√	×	0.03	51
Babaie et al., 2019	26	0.5	0.03	2.45e−2	Not required	×	√	0.007	3.25
Mosleh, 2019	30	0.75	0.03	2.20e−2	Not required	×	×	0.016	7.312
Wang and Xie, 2019	45	1	0.05	2.53e−2	Not required	×	×	0.05	27
Majeed et al., 2020	37	0.75	0.04	2.23e−2	Not required	×	√	0.022	6.178
Safoev and Jeon, 2020	56	1	0.05	2.72e−2	Logical crossing	×	√	0.05	14
Wang and Xie, 2020	60	1	0.06	2.60e−2	Not required	×	×	0.06	53
Joy et al., 2021	61	1	0.06	2.93e−2	Not required	×	×	0.06	8
This paper (Proposed 1)	21	0.5	0.01	2.06e−2	Not required	×	√	0.002	3.25
This paper (Proposed 2)	55	1	0.05	3.39e−2	Not required	√	√	0.05	55
This paper (Proposed 3)	46	1	0.04	2.73e−2	Logical crossing	√	√	0.04	30

Conclusions

1. In this research, several optimal 1-bit QCA full adders were presented. The proposed full adders are designed on a single layer with no rotated or shifted cells.

2. One of our proposed 1-bit full adders is designed by mere 21 QCA cells with 0.5 clock cycle latency. The total occupied area and the energy dissipation are 0.01 μm^2 and 2.06e−2 eV, respectively.

3. Also, other relevant arithmetic circuits were designed, including 1-bit add/sub, 4-bit ripple carry adder, 4-bit ripple borrow subtractor, and 2-bit array multiplier.

4. The scalable full adders are compared with the most recent ones, and the results indicate their superiority.

Hamideh KHAJEHNASIR-JAHROMI was born in Tehran, Iran, in 1991. She received BS degree and MS degree in electrical and electronic engineering. She defended her thesis (with honors) on designing QCA circuits in 2020 at Islamic Azad University, Science and Research Branch. Her research interests include quantum-dot cellular automata circuits, Multiple-Valued Logic (MVL) digital integrated circuits, logic gates, Nano-systems design, field-programmable gate array, and quantum computing. She is currently doing research work on the mentioned topics.

Pooya TORKZADEH was born in Isfahan, in 1980. He received the BS degree from Isfahan University of Technology (IUT), Iran, in 2002 and the MS and PhD degrees from the Sharif University of Technology (SUT), Iran, in 2004 and 2011 respectively both in electrical engineering. He is currently faculty member of Islamic Azad University, Science and Research Branch. Since 2003 he has joined in Sharif Integrated Circuit and System Group (SICAS) working on continuous/discrete time sigma-delta modulators with low power consumption for low power appliances. He has received many patents in the field of sigma-delta modulator designing and optimizing. He is the author and coauthor of more than 25 published international journal and conference papers on analog and digital integrated circuits. His research interests include ADC signal converters, low power phase locked loops (PLLs) with ultra-low phase noise amount for broad-band applications.

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