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An efficient counter-based Wallace-tree multiplier with a hybrid full adder core for image blending

Key words: Full adder; Transmission gate; Counter; Multiplier; Three-dimensional layout; Image blending

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Motivation

1. Due to the importance of digital counter circuits in the implementation of computational circuits, including multipliers systems, achieving the best counter cell structure with different input bits is inevitable. In this regard, full adder circuits have received less attention as fundamental cells for the configuration of counter circuits in recent years, and more attention has been paid to the implementation of such circuits based on numerous gate-level implementations. Accordingly, the most important goal of this research is to achieve the best performance of counter cells based on a remarkable full adder structure.

2. Subsequently, evaluating the performance of the structure provided in a real environment like an image blending application can provide more appropriate insights regarding the use of full adders in the implementation of counter cells.

Main idea

1. Designing a new full adder circuit based on a significant block diagram with special features is the first step in achieving the desired goal.

2. It is possible to evaluate the performance and improve the electrical performance of the proposed full adder circuit by relying on the hybrid structure, using modern design techniques.

3. Implementing counter cells with the number of input bits 4:3, 5:3, 6:3, and 7:3 by combining the proposed full adder and a reliable half adder can be a notable achievement compared to the designs in the literature.

4. Designing and implementing a new 8-bit counter-based Wallace-tree (CBW) multiplier using the proposed circuits to achieve low area consumption, ultra-low power dissipation, and appropriate speed, is another idea of this research.

5. Providing a new approach regarding the use of digital circuits in image processing applications is also one of the aims of this research.

Method

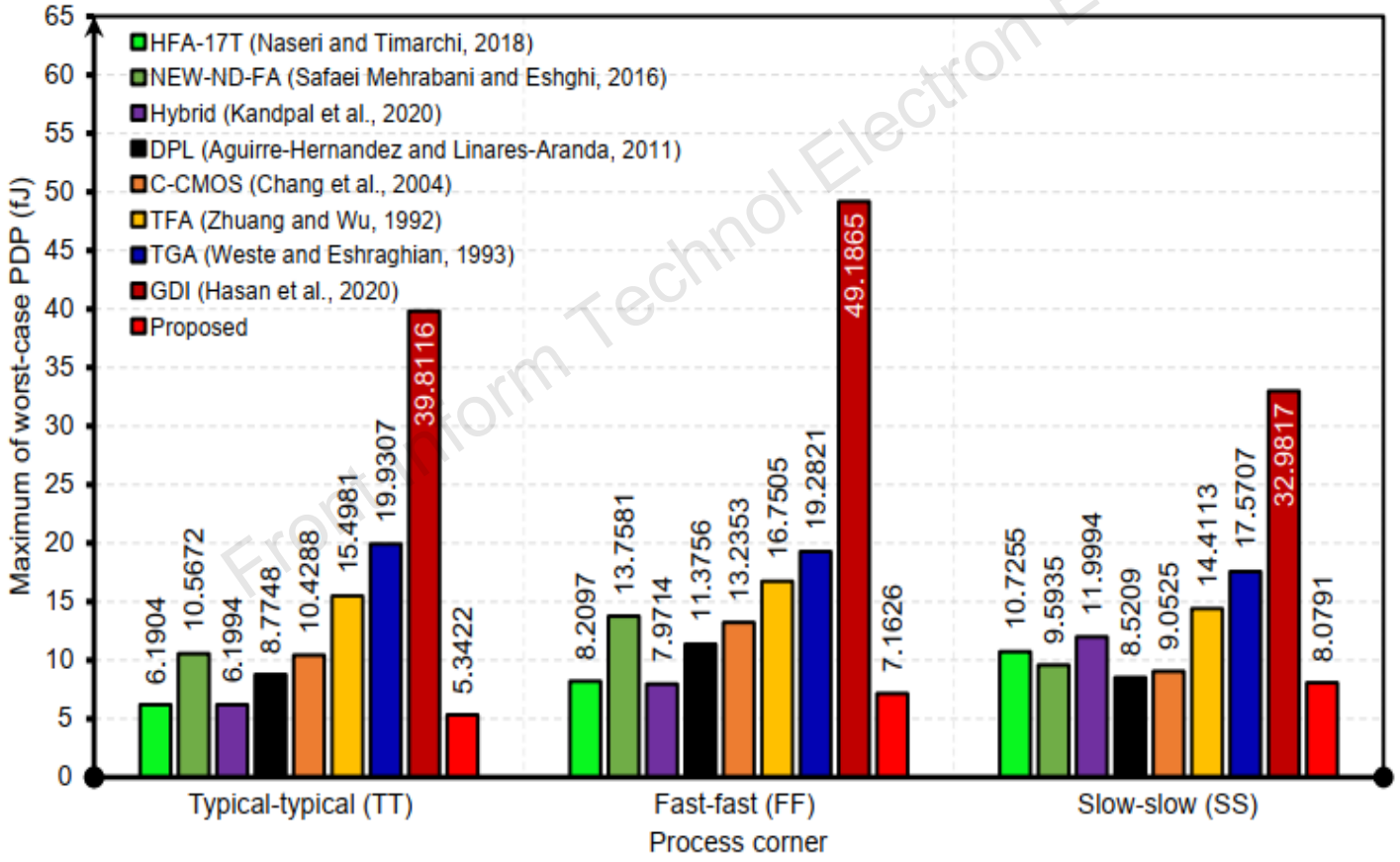
1. A new approach to achieving high efficient digital counter circuits is proposed by designing a full adder based on a hybrid structure.

2. Combining this full adder with a high performance half adder has been suggested as the main effort to achieve efficient digital counter cells.

3. The designed circuits are practically used in the design of a new CBW circuit and have improved the performance of these highly sensitive circuits so that they can be used in image processing applications.

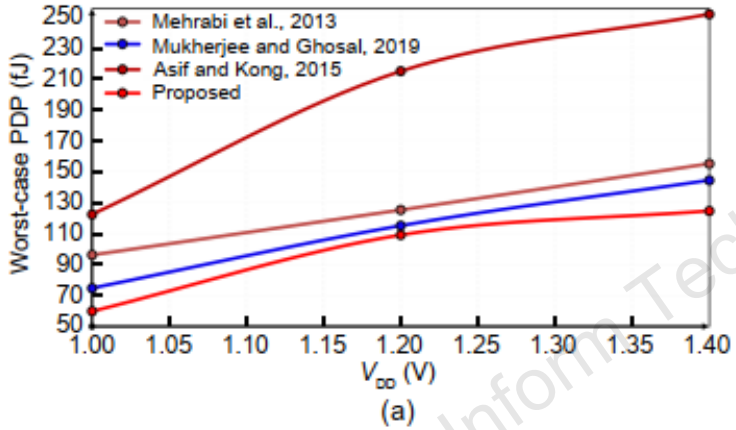
Major results

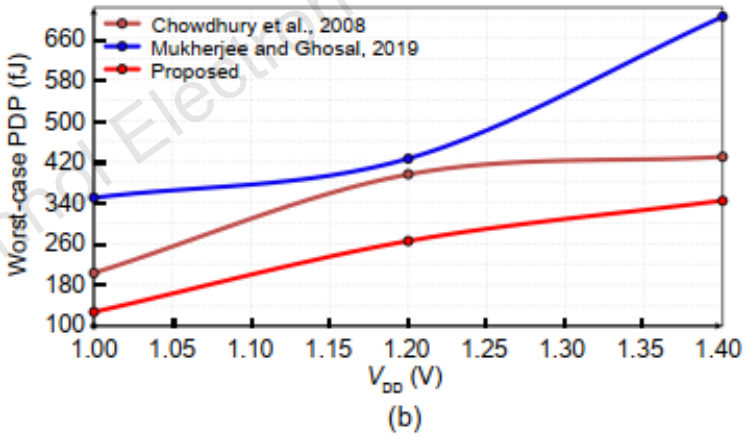
1. Simulation results of proposed hybrid full adder and related designs versus process-voltage-temperature (PVT) variations

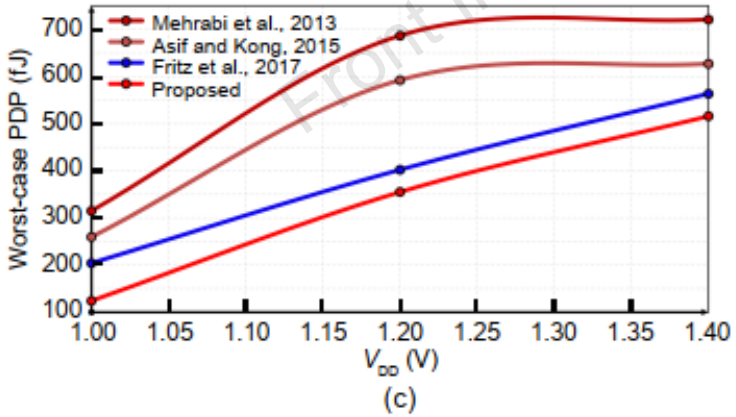


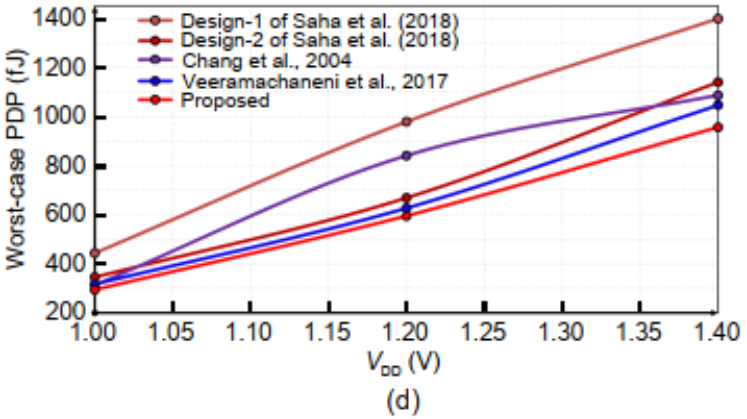
Major results (Cont'd)

2. Simulation results of proposed circuits when embedded in digital counter circuits with different input bits



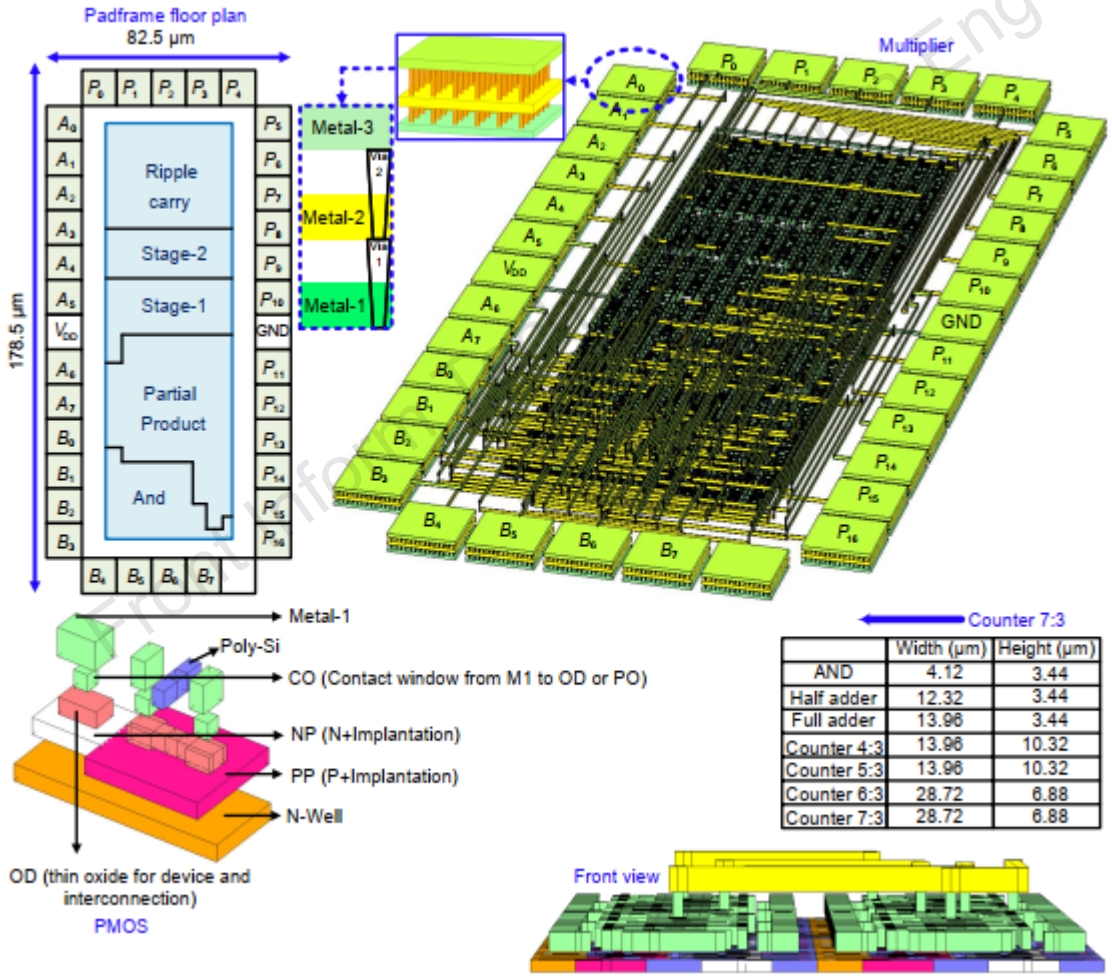






Major results (Cont'd)

3. Practical implementation of the proposed high efficient CBW



	Width (μm)	Height (μm)
AND	4.12	3.44
Half adder	12.32	3.44
Full adder	13.96	3.44
Counter 4:3	13.96	10.32
Counter 5:3	13.96	10.32
Counter 6:3	28.72	6.88
Counter 7:3	28.72	6.88

Conclusions

1. In this research, a new high efficient full adder cell with considerable characteristics is proposed and tested under different circumstances.

2. Using the hybrid technique in the proposed full adder circuit, a new approach has been developed to implement digital counters.

3. The results of the image blending application demonstrate the superiority of the proposed approach regarding the design of high performance CBWs for next-generation computers.

Ayoub Sadeghi received his BS degree in Electronic Engineering from Islamic Azad University, Shiraz, Iran, in 2016, where he finished his MS degree in VLSI design engineering in 2019. His research interests include high efficient arithmetic circuit design, approximate computing, digital image processing, bioelectronics design, and circuit optimization methods.

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