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Efficient and optimized approximate GDI full adders based on dynamic threshold CNTFETs for specific least significant bits

Key words: Carbon nanotube field-effect transistor (CNTFET); Optimization algorithm; Nondominated sorting based genetic algorithm II (NSGA-II); Gate diffusion input (GDI); Approximate computing

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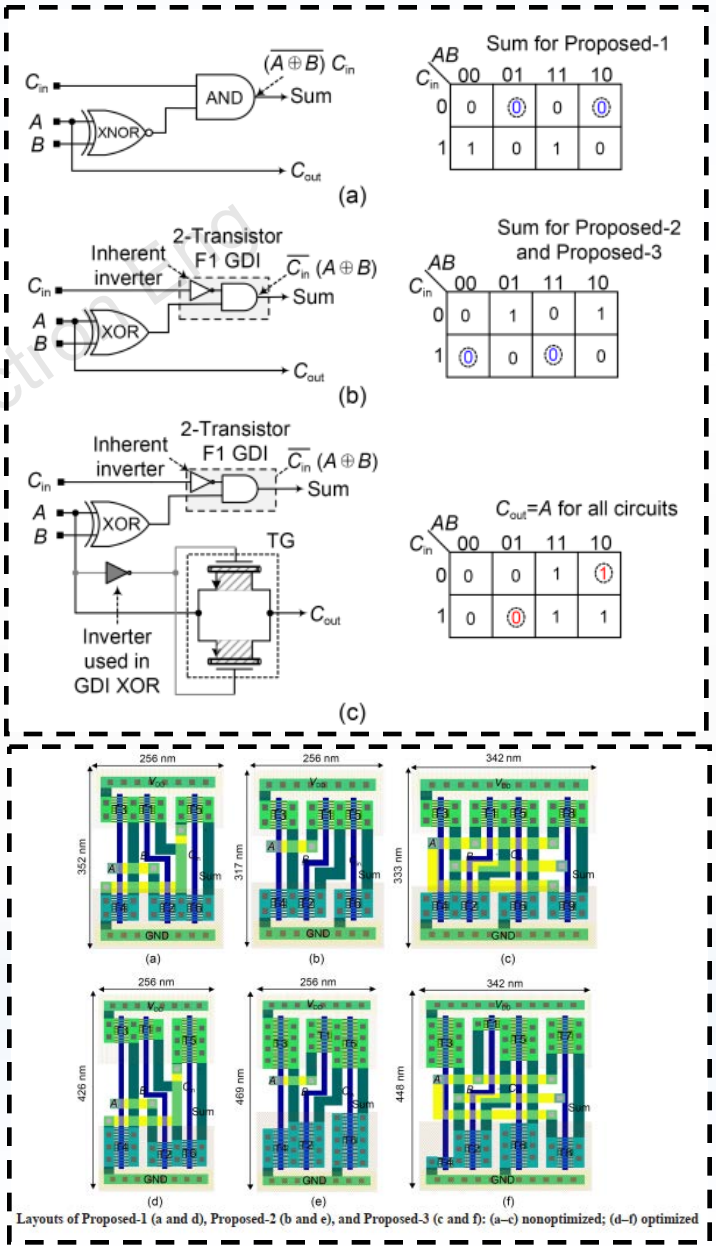
Motivation

- Considering the importance of energy efficiency in the design of digital circuits used in image processing applications, the use of the emerging technique of approximate computing has been seriously considered. Although different approaches have been established by researchers, it can be mentioned that the most important drawback of existing achievements is their lack of efficiency in various types of approximate computing circuits and numerous related applications.

- In this research, a reliable approach based on multi-faceted consideration of the design technique and optimization methods is discussed, so that a suitable mechanism can be found to consider different tradeoffs concerned with the issue of approximate computing circuits.

Main idea

- Designing three new approximate full adder circuits based on the integration of gate diffusion input (GDI) and dynamic threshold (DT) techniques using CNTFET technology.
- Features including low power consumption and high speed can be observed in the proposed circuits due to the use of the GDI technique and outputs with full swing voltages by the DT technique and considering the minimum V_{th} in CNTFETs.
- Using the NSGA-II optimization method to attain the best performance of the proposed circuits in terms of power, delay, PDP, and output swing to be able to use them in approximate ripple carry adders (RCAs) with different numbers of approximate bits (NABs).
- Using approximate RCAs in image addition processing by a direct interface between HSPICE and MATLAB.



Layouts of Proposed-1 (a and d), Proposed-2 (b and e), and Proposed-3 (c and f): (a–c) nonoptimized; (d–f) optimized

Methods

- Using CNTFET technology with 32 nm channel length for circuit simulations by HSPICE and extracting error metrics by MATLAB.
- Applying NSGA-II as an optimization method to the proposed circuits by considering parameters like the number of tubes and chirality vectors as objectives by creating a direct interface between HSPICE and MATLAB.
- Applying the equivalent voltage matrices extracted from the pixels of the images to the proposed circuits by a direct interface between HSPICE and MATLAB to verify the correctness and efficiency of the proposed approximate circuits.

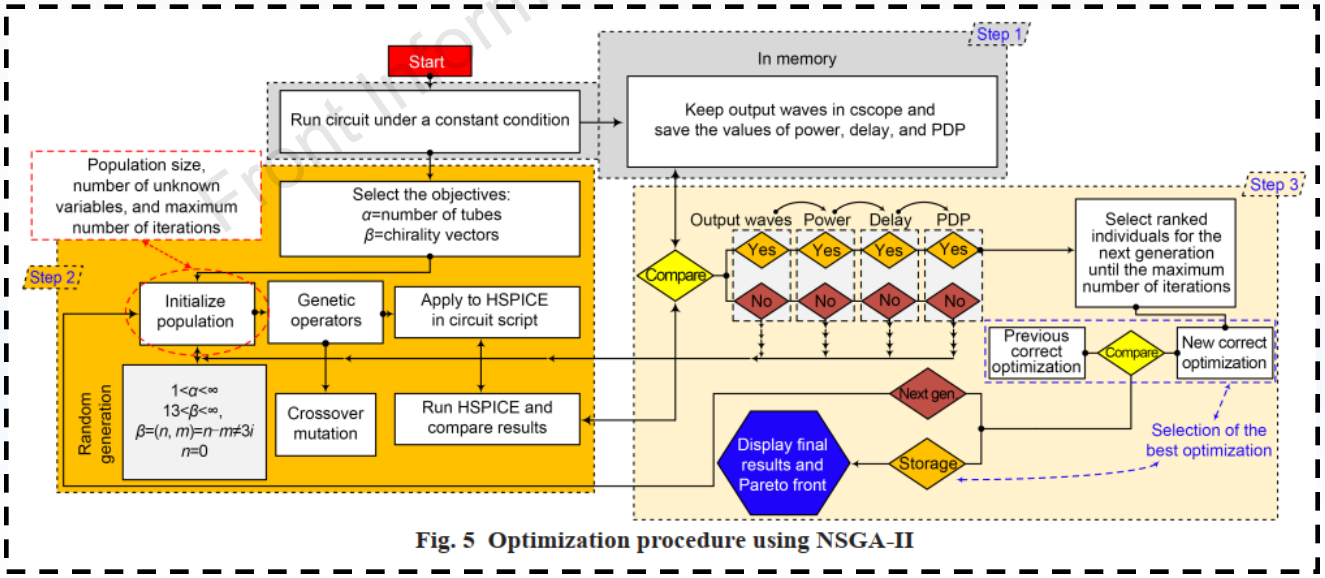
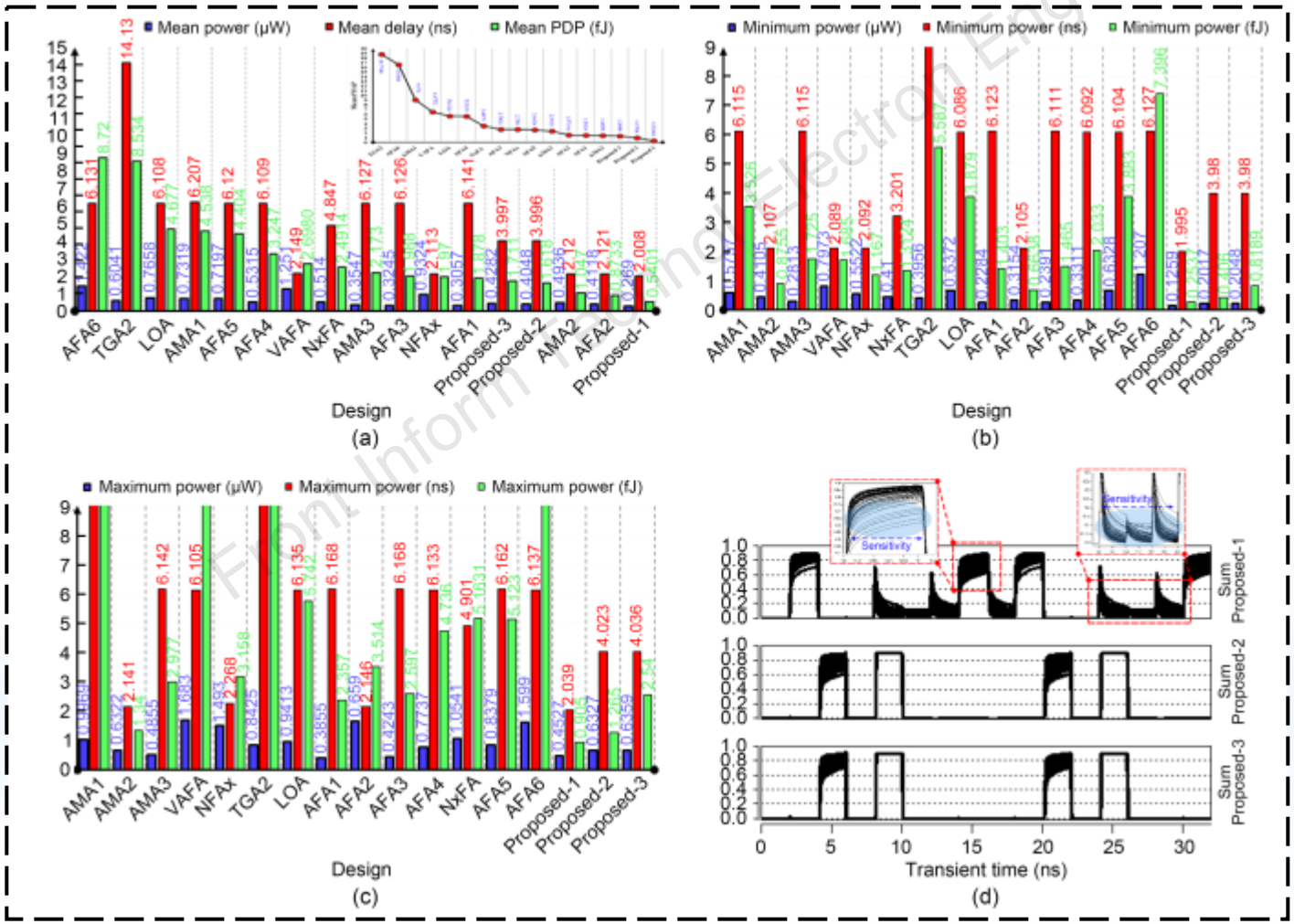


Fig. 5 Optimization procedure using NSGA-II

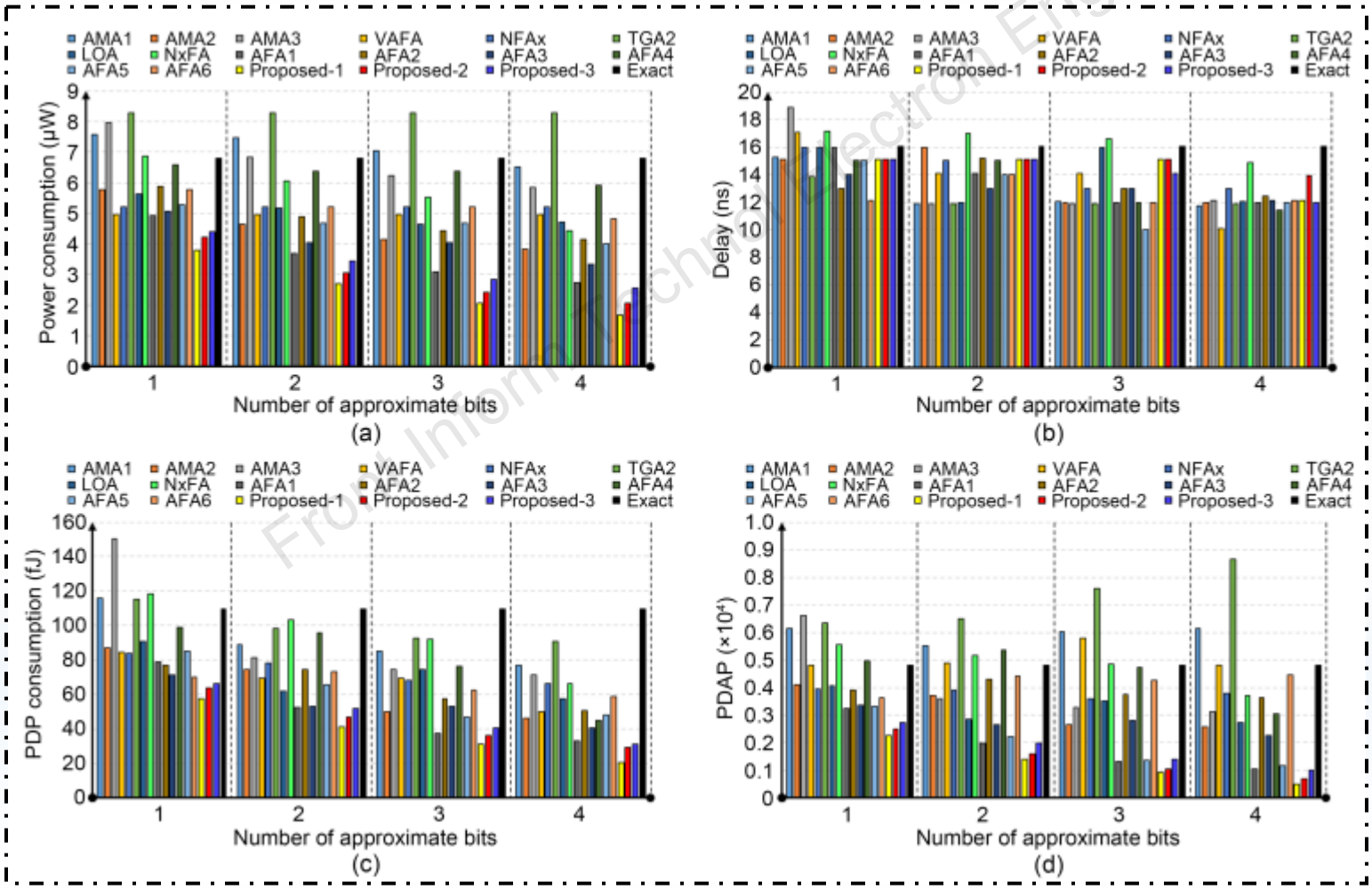
Major results

1. Simulation results of the proposed approximate full adders versus lithographic variation results by the Monte Carlo Method



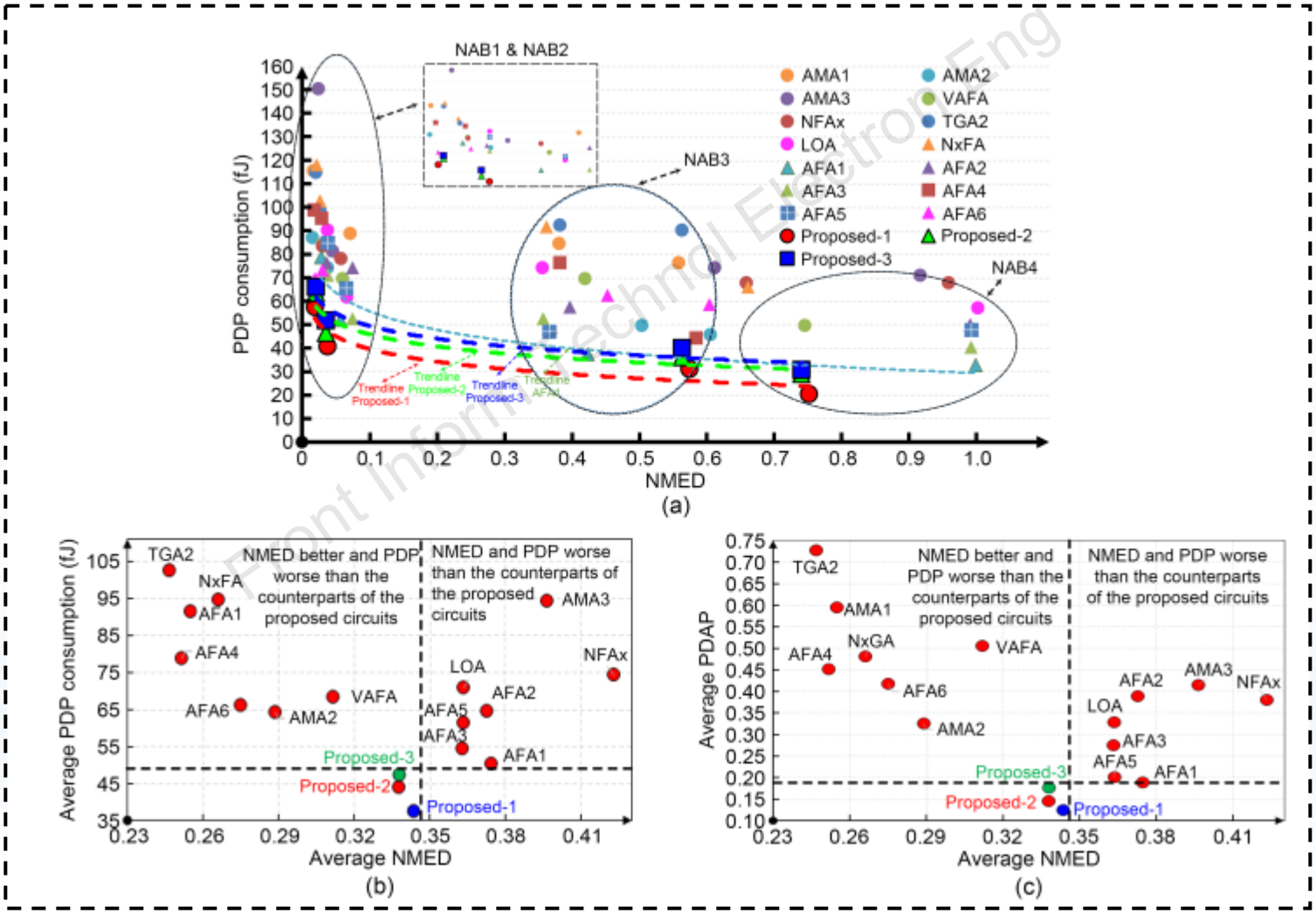
Major results (Cont'd)

2. Performance of the optimized approximate RCAs versus different numbers of approximate bits



Major results (Cont'd)

3. Comparison of the optimized approximate RCAs for different numbers of approximate bits



Conclusions

- In this research, three new high-efficient approximate full adder cells with considerable characteristics are proposed and tested under different circumstances.

- The integration of GDI and the DT design technique along with CNTFET technology is introduced as an efficient approach.

- Using NSGA-II as an optimization method to achieve the best performance of the proposed effective circuits is a special achievement, especially in terms of power and area of the layout.

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