

Jie CUI, Peipei LI, Weixing SHENG. 2023. High linearity U-band power amplifier design: a novel intermodulation point analysis method. *Frontiers of Information Technology & Electronic Engineering*, 24(1):176-186.

<https://doi.org/10.1631/FITEE.2200082>

# High linearity U-band power amplifier design: a novel intermodulation point analysis method

**Key words:** CMOS silicon-on-insulator (SOI); Linearity analysis; Millimeter wave (mm-Wave); Power amplifier

Corresponding author: Jie CUI

E-mail: [cuijie@njust.edu.cn](mailto:cuijie@njust.edu.cn)

 ORCID: <https://orcid.org/0000-0003-3393-8559>

# Motivation

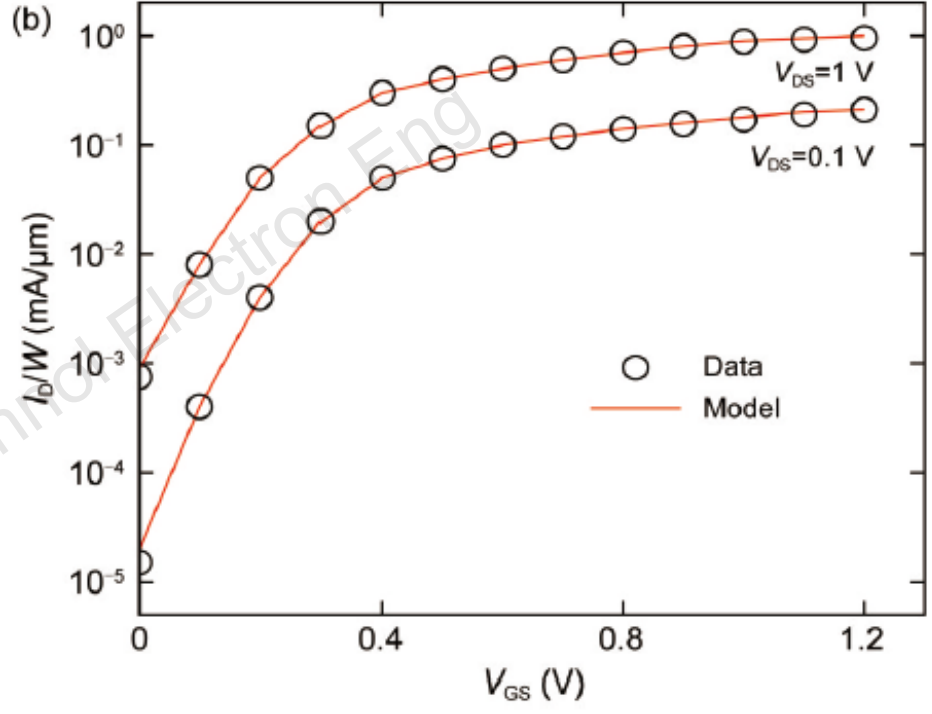
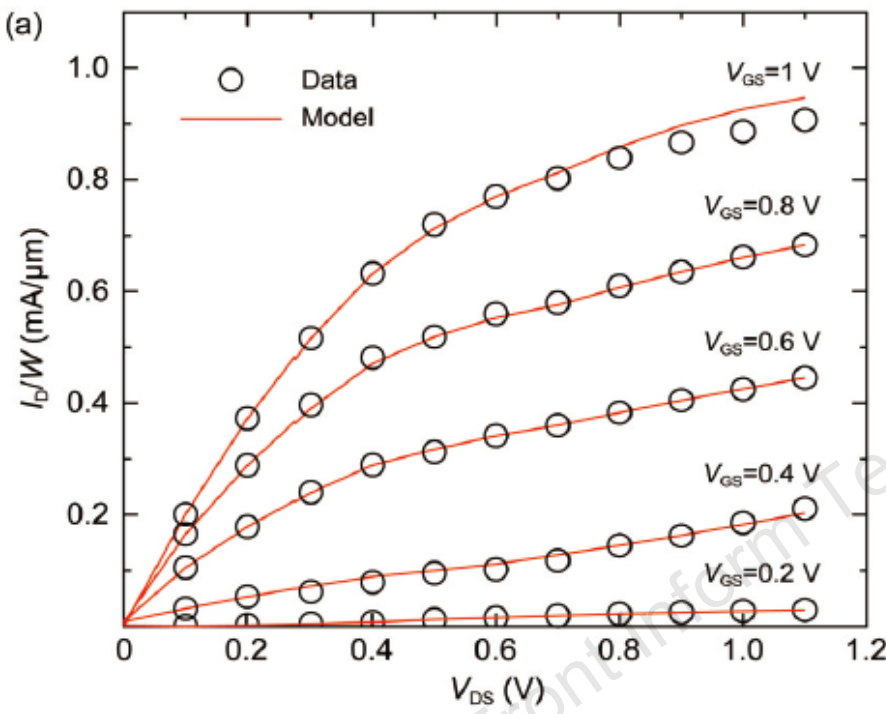
- CMOS technology offers low fabrication cost, high integration capability, and process consistency for implementing wireless transceivers for communication, radar, and other applications.
- CMOS power amplifiers (PAs) are notoriously difficult to implement, especially two main drawbacks of poor linearity and low efficiency in scaled CMOS technology.
- A theoretical analysis of the linearity of CMOS stacked cell PAs with multiple demonstration is presented.

# Main idea

A intermodulation point analysis method is introduced to predict and improve mm-Wave CMOS power amplifier's linearity:

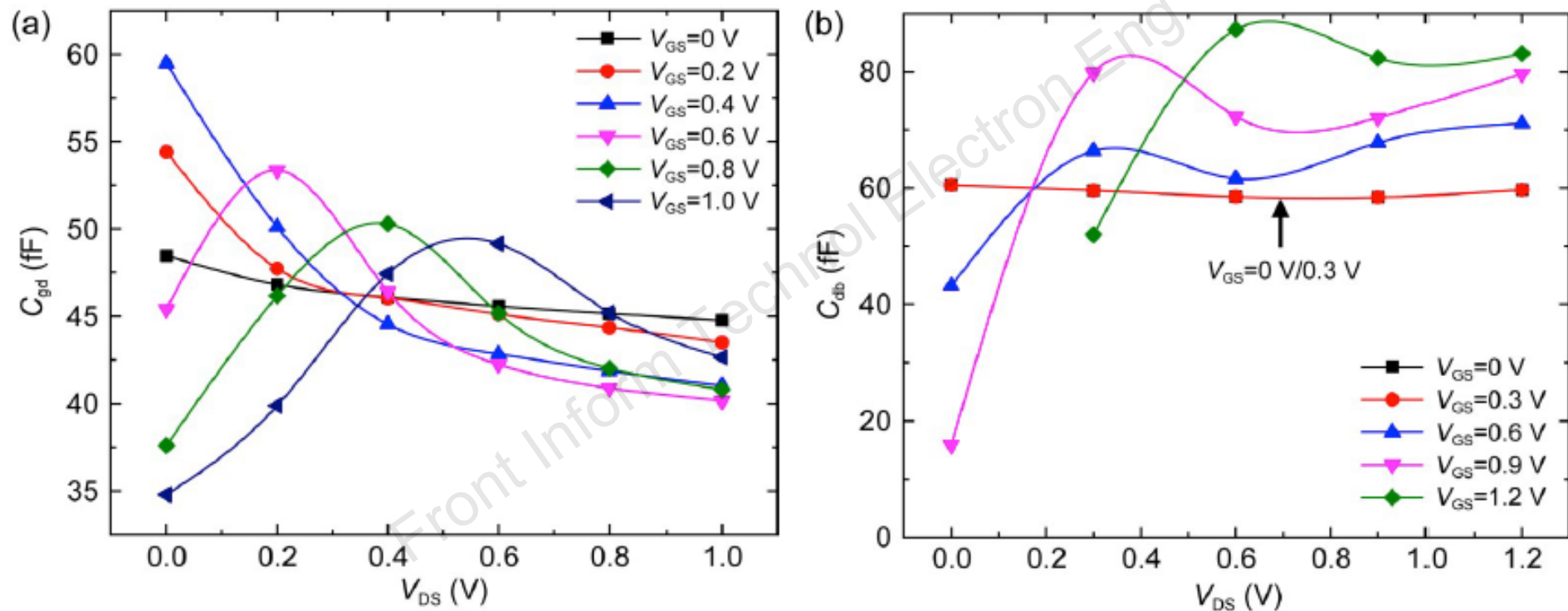
- Theoretical analysis of transistor parasitic parameters and its effect on linearity and demonstration
- Stacked PA power cell equivalent circuit model extraction and intermodulation point linearity analysis
- A demonstration of mm-Wave CMOS PA design with linearity boost technology by the help of intermodulation point analysis method

# Transistor virtual source model linearity analysis by normalized current with different voltage supply



$$I_D = g_m V_{gs} \frac{V_{DS}/V_{Dsat}}{\left[ 1 + (V_{DS}/V_{Dsat})^\beta \right]^{\frac{1}{\beta}}},$$

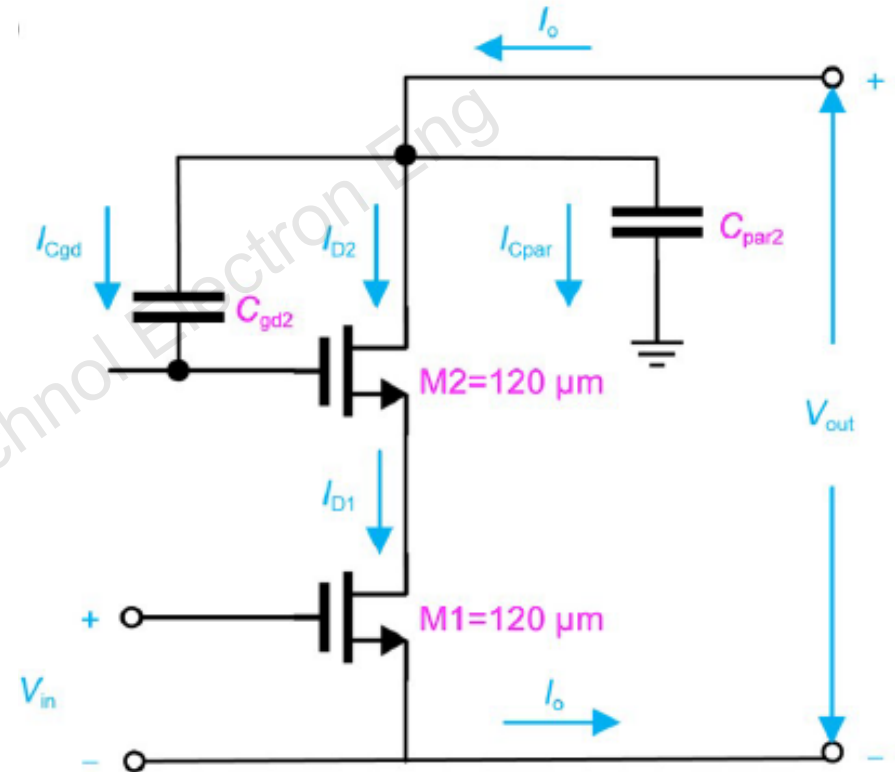
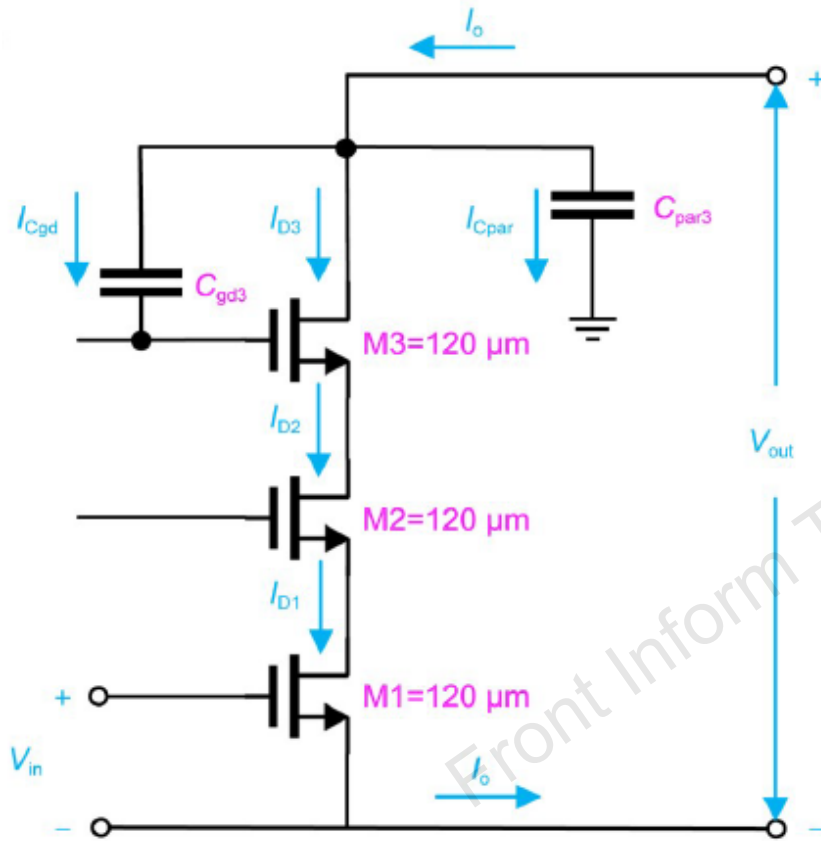
# Transistor nonlinearity due to nonlinear capacitance extracted using bias-dependent S-parameters



$$I_D = a_0 + a_1 V_{DS} + a_2 V_{DS}^2 + a_3 V_{DS}^3,$$

$$C_{gd} = c_0 + c_1 V_{DS} + c_2 V_{DS}^2 + c_3 V_{DS}^3,$$

# Triple cascode cell and cascode cell equivalent circuit model



$$C_{gd2} = c_0 + \frac{c_1}{2} V_o + \frac{c_2}{4} V_o^2 + \frac{c_3}{8} V_o^3.$$

$$I_{Cgd2} = j\omega C_{gd2} \left( \frac{V_o(2 + g_m R_L)}{2g_m R_L} + \frac{V_{oQ}}{g_m R_L} \right),$$

# Stacked cells OIP<sub>3</sub> formula

$$\text{OIP}_{3\text{casc}} = 10\lg \left( \frac{8}{3R_L} \left| \frac{a_1 g_m R_L + j\omega (2iC_{\text{par}3} g_m R_L + c_0 (2 + g_m R_L) - c_1 V_{\text{oQ}})}{a_3 g_m R_L + j\omega (c_2 (2 + g_m R_L) - c_3 V_{\text{oQ}})} \right| \right)$$

$$I_D = a_0 + \frac{a_1}{3} V_o + \frac{a_2}{9} V_o^2 + \frac{a_3}{27} V_o^3,$$

$$I_{\text{Cgd}3} = j\omega C_{\text{gd}3} \left( \frac{V_o (3 + g_m R_L)}{3g_m R_L} + \frac{V_{\text{oQ}}}{g_m R_L} \right),$$

$$I_o = I_D + I_{\text{Cgd}3} + I_{\text{Cpar}3},$$

$$\text{OIP}_{3\text{triple\_casc}} = 10\lg \left( \frac{6}{R_L} \left| \frac{a_1 g_m R_L + j\omega (3iC_{\text{par}3} g_m R_L + c_0 (3 + g_m R_L) - c_1 V_{\text{oQ}})}{a_3 g_m R_L + j\omega (c_2 (3 + g_m R_L) - c_3 V_{\text{oQ}})} \right| \right)$$

# Extracted parameters of cascode and triple cascode cells based on measurement

Parameter	Triple Cascode	Cascode
$V_{oQ}$ (V)	3	2
$V_{Dsat}$ (V)	0.2	
$\beta$	1.8	
$c_0$ (F)	6.00E-14	
$c_1$ (F/V)	-6.45E-14	
$c_2$ (F/V <sup>2</sup> )	7.81E-14	
$c_3$ (F/V <sup>3</sup> )	-3.26E-14	
$a_0$ (A)	0.005562	
$a_1$ (A/V)	0.03061	
$a_2$ (A/V <sup>2</sup> )	-0.0221	
$a_3$ (A/V <sup>3</sup> )	0.00575	
$C_{par}$ (F)	2.00E-14	6.00E-14
$g_m$ (A/V)	0.18	
$R_l$ ( $\Omega$ )	50	

# Calculated $OIP_3$ and measured $P_{1dB}$ for stacked cells and PA demonstration

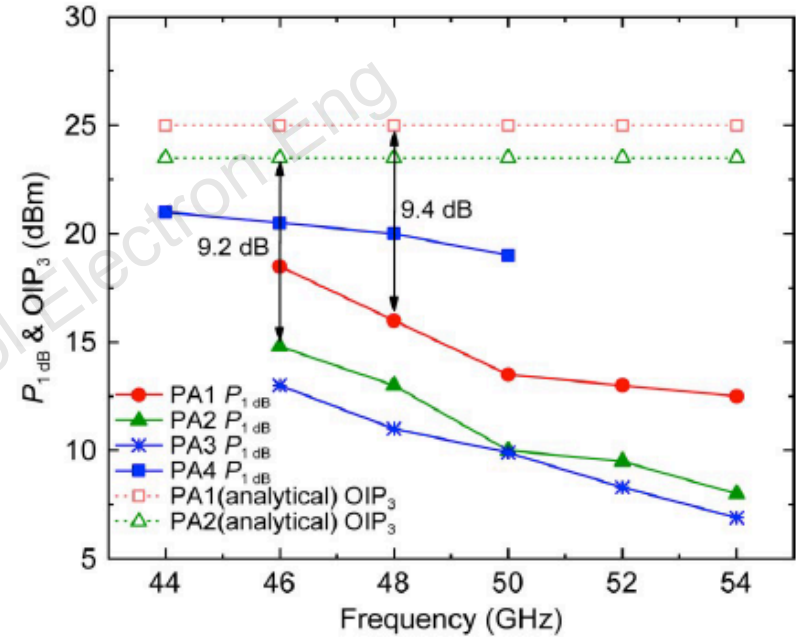
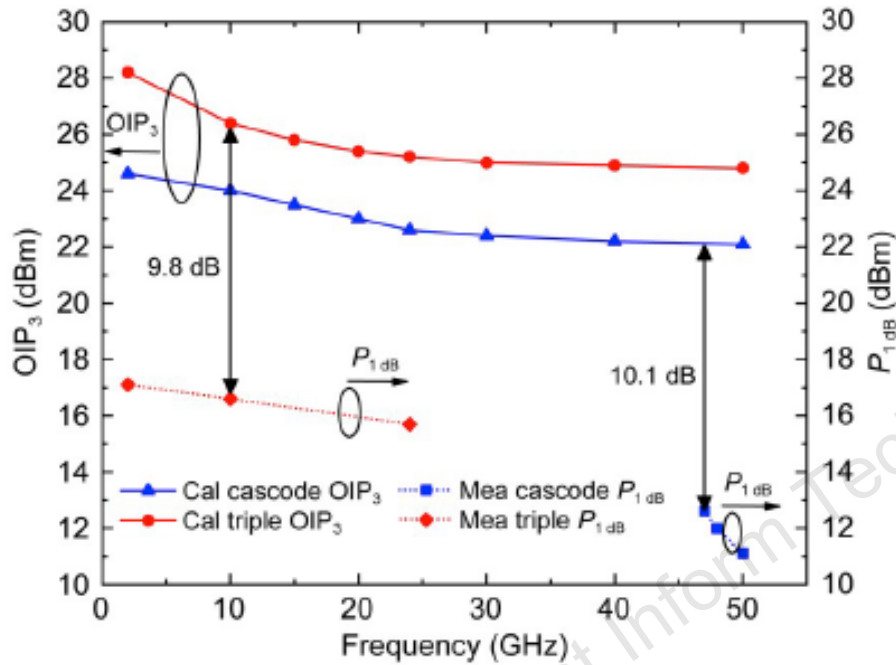
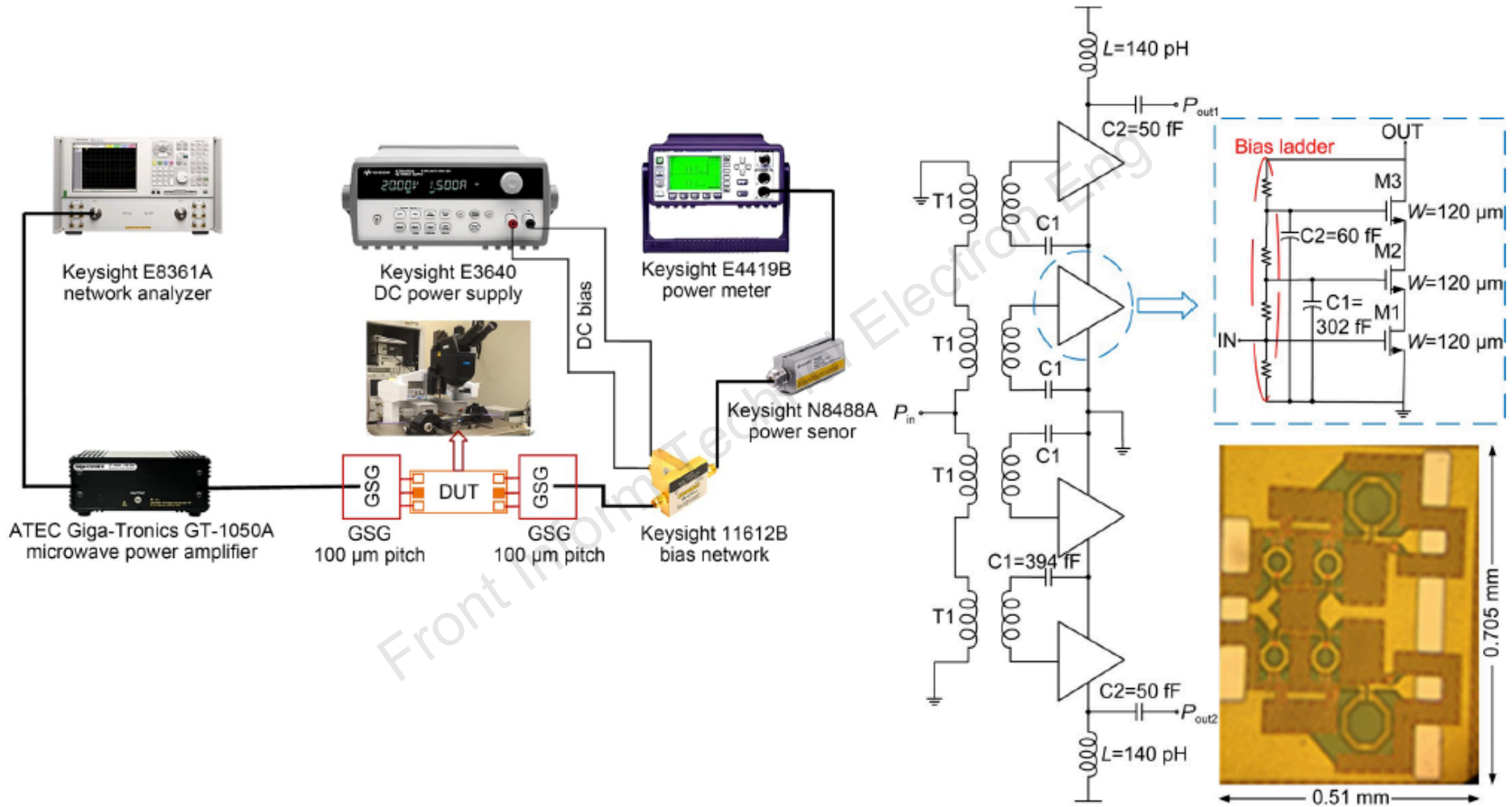


Fig. 4 Calculated  $OIP_3$  and measured  $P_{1dB}$  for cascode and triple cascode cells as functions of frequency using the analytical approach (Eqs. (11) and (18))

Fig. 5 Measured  $P_{1dB}$  values for PA1 to PA4 as functions of frequency and analytical  $OIP_3$  values for PA1 and PA2 vs. frequency for comparison

# Differential mm-Wave CMOS PA design and demonstration



# Differential mm-Wave CMOS PA design and demonstration

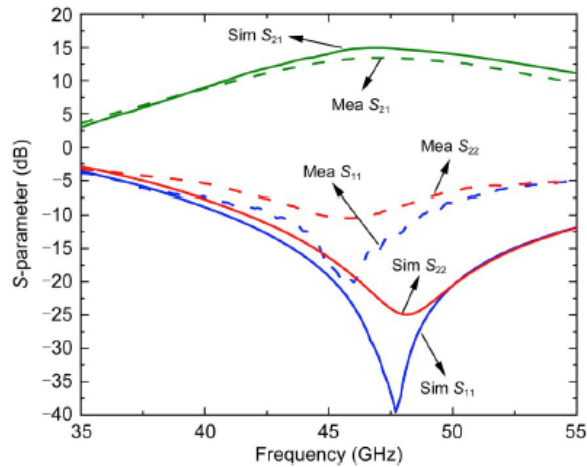


Fig. 9 Simulated (solid line) and measured (dashed line)  $S$ -parameters of the fabricated differential PA4 chip under 6 V supply

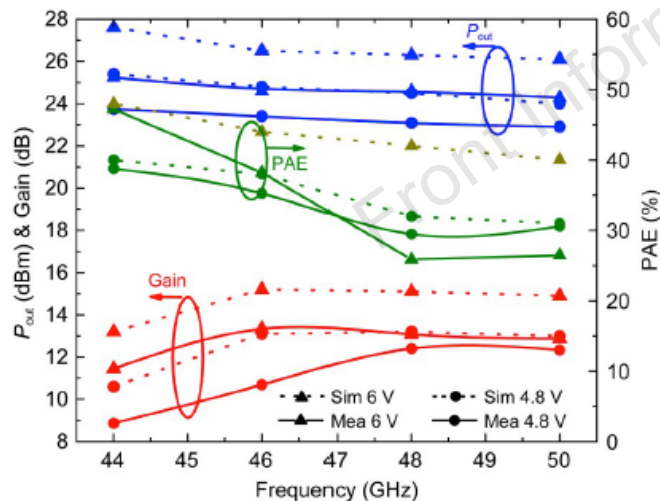


Fig. 11 Simulated and measured power  $P_{out}$ , Gain, and PAE vs. frequency for the differential PA (PA4) under two bias conditions (4.8 V and 6 V)

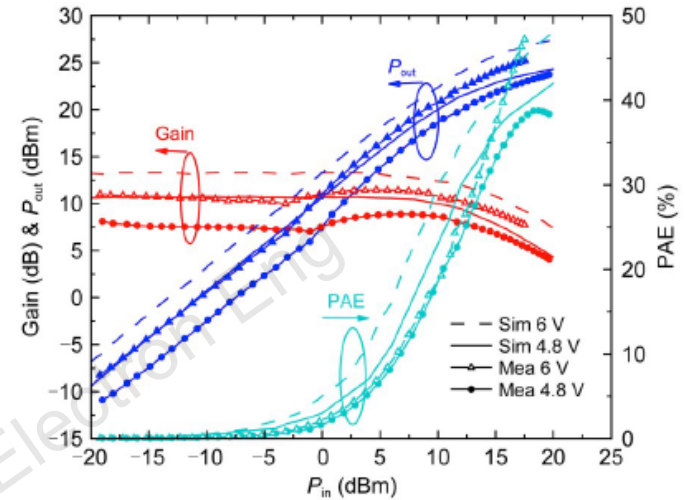


Fig. 10 Simulated and measured power for the differential PA (PA4) at 44 GHz under two bias conditions (4.8 V and 6 V)

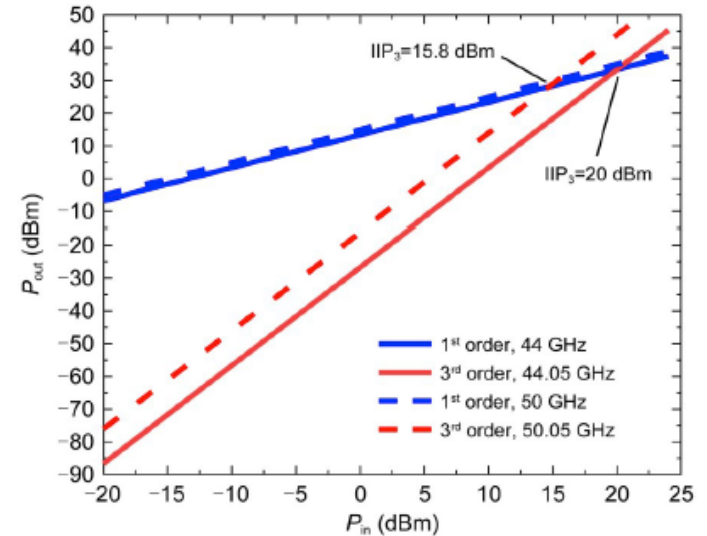


Fig. 12 IIP<sub>3</sub> simulation results of the differential PA4

# Conclusions

- For mm-Wave amplifiers, CMOS SOI shows its advantages in power and efficiency. To improve the linearity of the circuit, the parasitic parameters that affect are derived and analyzed.
- A linearity analysis that takes into account the nonlinearities of the transistor current and capacitances is introduced.
- A state-of-art U-band high linearity and efficiency CMOS PA is proposed and demonstrated in 45 nm CMOS SOI technology.