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High linearity U-band power amplifier design: a novel intermodulation point analysis method

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Key words: CMOS silicon-on-insulator (SOI); Linearity analysis; Milimeter wave (mm-Wave); Power amplifier

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Motivation

- CMOS technology offers low fabrication cost, high integration capability, and process consistency for implementing wireless transceivers for communication, radar, and other applications.
- CMOS power amplifiers (PAs) are notoriously difficult to implement, especially two main drawbacks of poor linearity and low efficiency in scaled CMOS technology.
- A theoretical analysis of the linearity of CMOS stacked cell PAs with multiple demonstration is presented.

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Main idea

A intermodulation point analysis method is introduced to predict and improve mm-Wave CMOS power amplifier's linearity:

- Theoretical analysis of transistor parasitic parameters and its effect on linearity and demonstration
- Stacked PA power cell equivalent circuit model extraction and intermodulation point linearity analysis
- A demonstration of mm-Wave CMOS PA design with linearity boost technology by the help of intermodulation point analysis method

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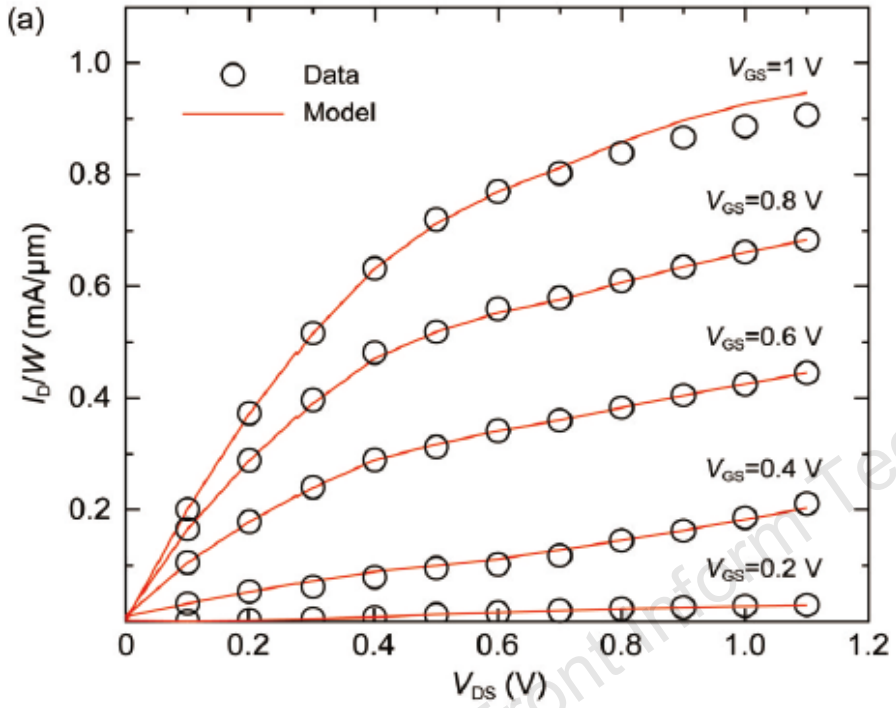
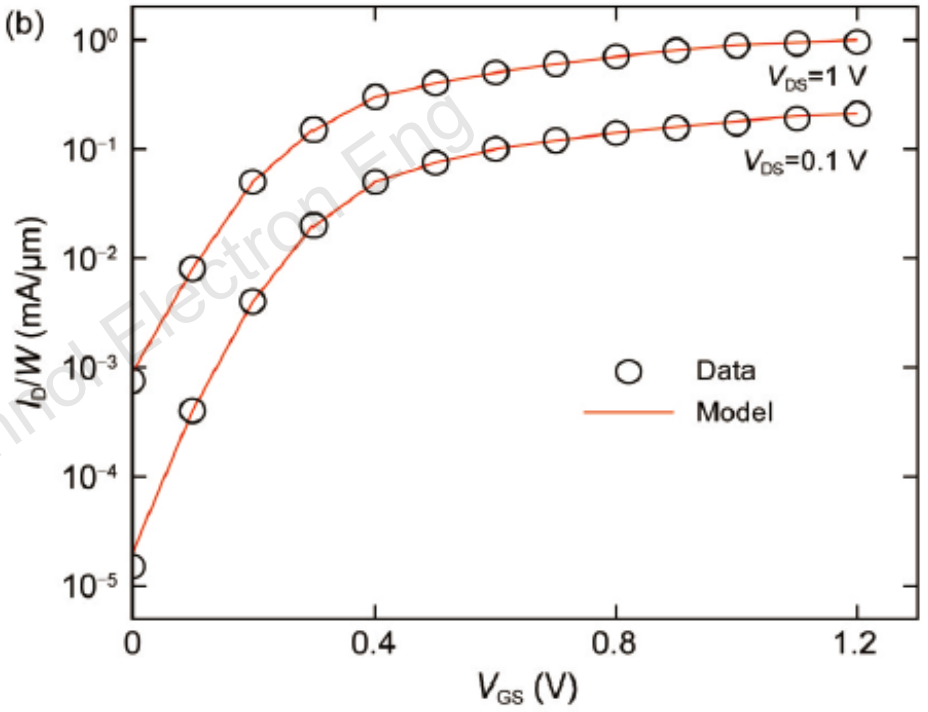
Transistor virtual source model linearity analysis by normalized current with different voltage supply





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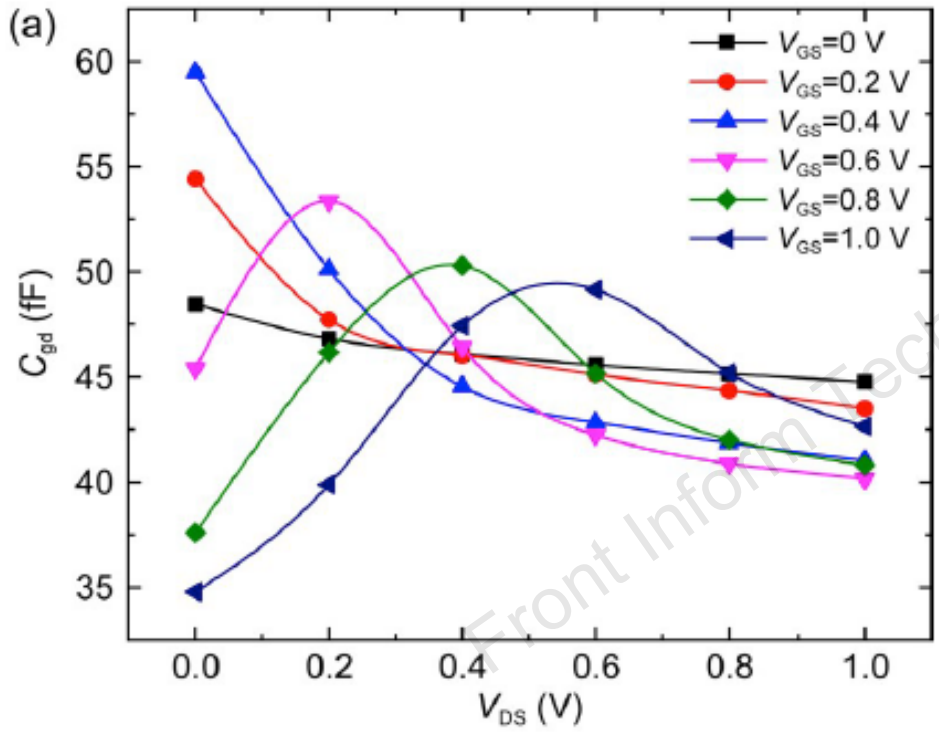
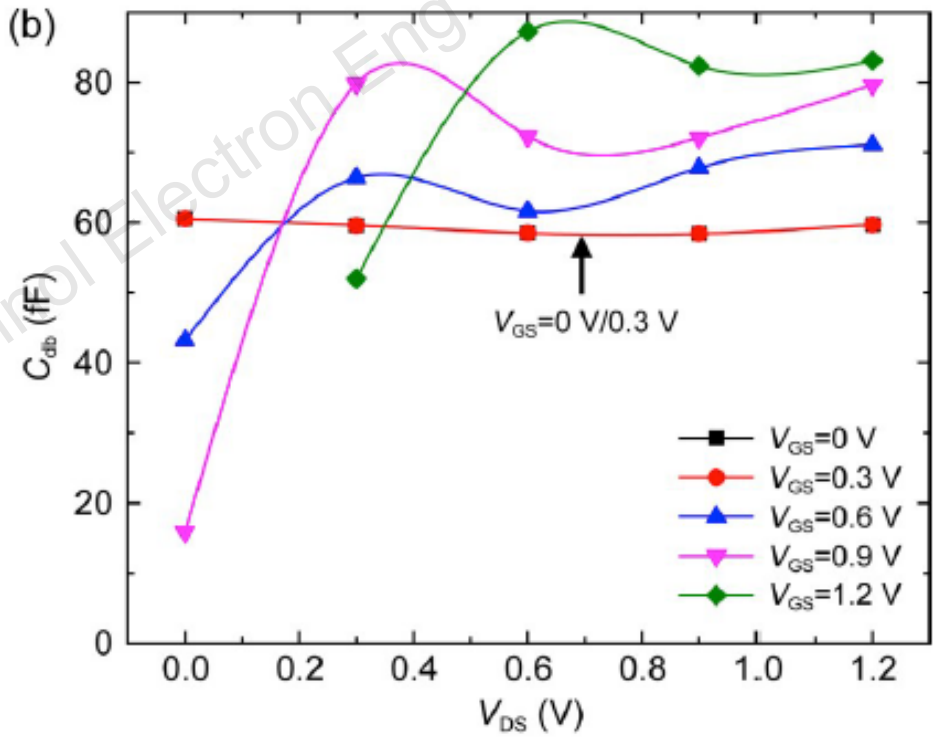
$$I_D = g_m V_{gs} \frac{V_{DS}/V_{Dsat}}{\left[1 + \left(V_{DS}/V_{Dsat}\right)^{\beta}\right]^{\frac{1}{\beta}}},$$

Transistor nonlinearity due to nonlinear capacitance extracted using bias-dependent *S*-parameters





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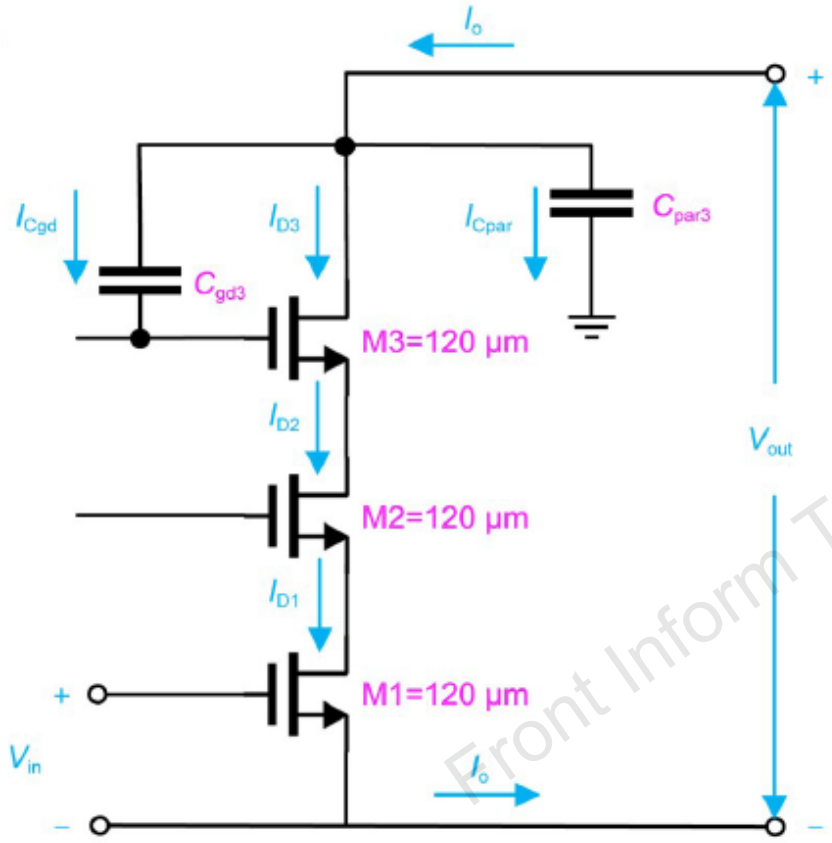
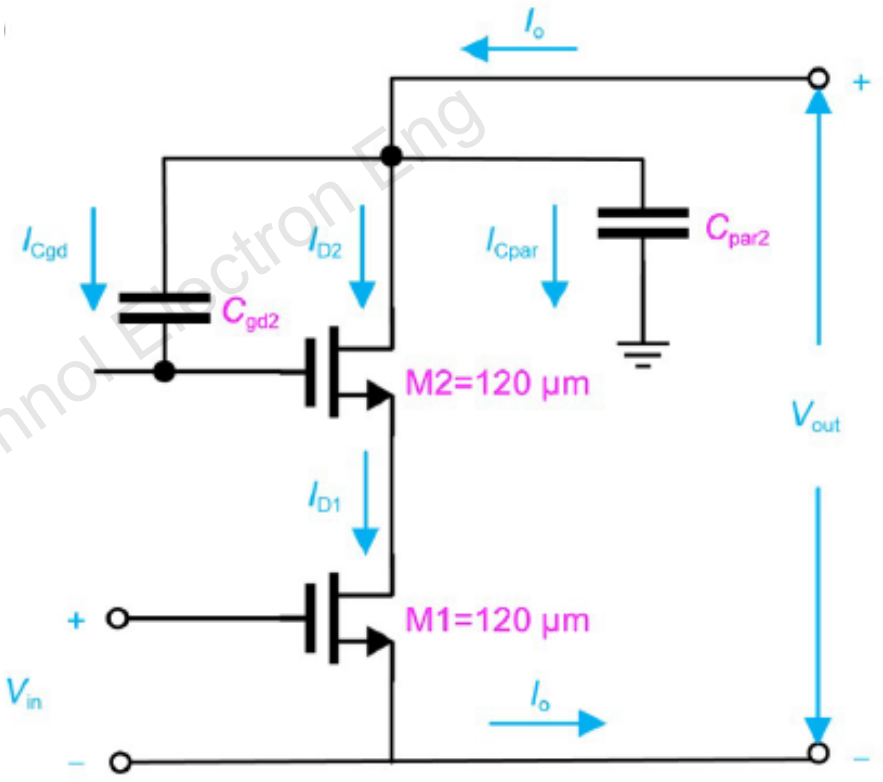
$$I_D = a_0 + a_1 V_{DS} + a_2 V_{DS}^2 + a_3 V_{DS}^3 ,$$

$$C_{gd} = c_0 + c_1 V_{DS} + c_2 V_{DS}^2 + c_3 V_{DS}^3 ,$$

Triple cascode cell and cascode cell equivalent circuit model





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$$C_{gd2} = c_0 + \frac{c_1}{2}V_o + \frac{c_2}{4}{V_o}^2 + \frac{c_3}{8}{V_o}^3 .$$

$$I_{Cgd2} = j\omega C_{gd2}\left(\frac{V_o\left(2 + g_m R_L\right)}{2g_m R_L} + \frac{V_{oQ}}{g_m R_L}\right),$$

Stacked cells OIP_3 formula

$$\mathrm{OIP}_{3\mathrm{casc}} = 10\lg\left(\frac{8}{3R_{\mathrm{L}}}\left|\frac{a_1 g_{\mathrm{m}} R_{\mathrm{L}} + \mathrm{j}\omega\left(2iC_{\mathrm{par3}} g_{\mathrm{m}} R_{\mathrm{L}} + c_0\left(2 + g_{\mathrm{m}} R_{\mathrm{L}}\right) - c_1 V_{\mathrm{oQ}}\right)}{a_3 g_{\mathrm{m}} R_{\mathrm{L}} + \mathrm{j}\omega\left(c_2\left(2 + g_{\mathrm{m}} R_{\mathrm{L}}\right) - c_3 V_{\mathrm{oQ}}\right)}\right|\right)$$

$$I_{\mathrm{D}} = a_0 + \frac{a_1}{3} V_{\mathrm{o}} + \frac{a_2}{9} V_{\mathrm{o}}^{\,2} + \frac{a_3}{27} V_{\mathrm{o}}^{\,3},$$

$$I_{\mathrm{Cgd3}} = \mathrm{j}\omega C_{\mathrm{gd3}}\left(\frac{V_{\mathrm{o}}\left(3 + g_{\mathrm{m}} R_{\mathrm{L}}\right)}{3 g_{\mathrm{m}} R_{\mathrm{L}}} + \frac{V_{\mathrm{oQ}}}{g_{\mathrm{m}} R_{\mathrm{L}}}\right),$$

$$I_{\mathrm{o}} = I_{\mathrm{D}} + I_{\mathrm{Cgd3}} + I_{\mathrm{Cpar3}},$$

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$$\mathrm{OIP}_{3\mathrm{triple_casc}} = 10\lg\left(\frac{6}{R_{\mathrm{L}}}\left|\frac{a_1 g_{\mathrm{m}} R_{\mathrm{L}} + \mathrm{j}\omega\left(3iC_{\mathrm{par3}} g_{\mathrm{m}} R_{\mathrm{L}} + c_0(3 + g_{\mathrm{m}} R_{\mathrm{L}}) - c_1 V_{\mathrm{oQ}}\right)}{a_3 g_{\mathrm{m}} R_{\mathrm{L}} + \mathrm{j}\omega\left(c_2(3 + g_{\mathrm{m}} R_{\mathrm{L}}) - c_3 V_{\mathrm{oQ}}\right)}\right|\right)$$

Extracted parameters of cascode and triple cascode cells based on measurement

Parameter	Triple Cascode	Cascode
V_{oQ} (V)	3	2
V_{Dsat} (V)	0.2	
β	1.8	
c_0 (F)	6.00E-14	
c_1 (F/V)	-6.45E-14	
c_2 (F/V^2)	7.81E-14	
c_3 (F/V^3)	-3.26E-14	
a_0 (A)	0.005562	
a_1 (A/V)	0.03061	
a_2 (A/V^2)	-0.0221	
a_3 (A/V^3)	0.00575	
C_{par} (F)	2.00E-14	6.00E-14
g_m (A/V)	0.18	
R_L (Ω)	50	

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Calculated OIP_3 and measured P_{1dB} for stacked cells and PA demonstration

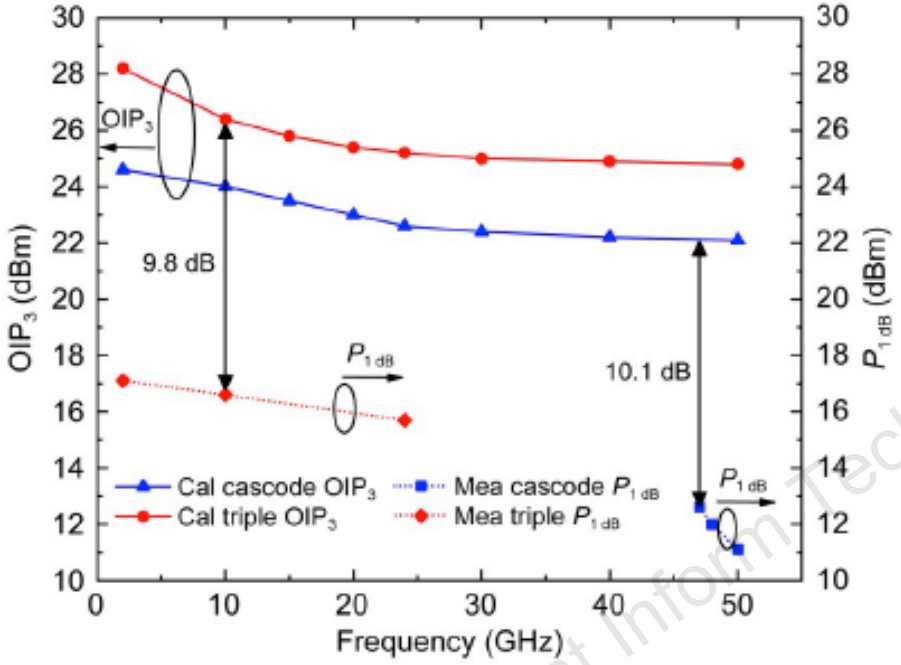

Fig. 4 Calculated OIP_3 and measured $P_{1\,dB}$ for cascode and triple cascode cells as functions of frequency using the analytical approach (Eqs. (11) and (18))

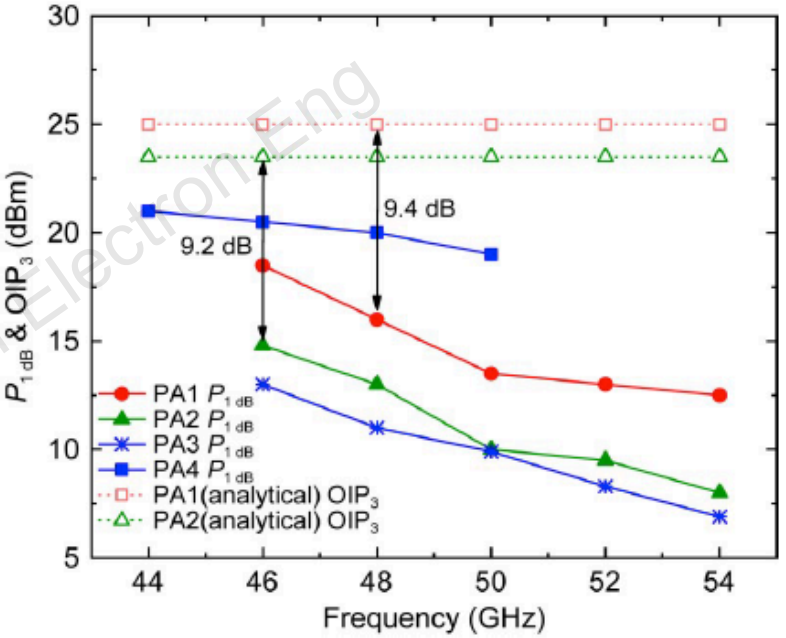

Fig. 5 Measured $P_{1\,dB}$ values for PA1 to PA4 as functions of frequency and analytical OIP_3 values for PA1 and PA2 vs. frequency for comparison

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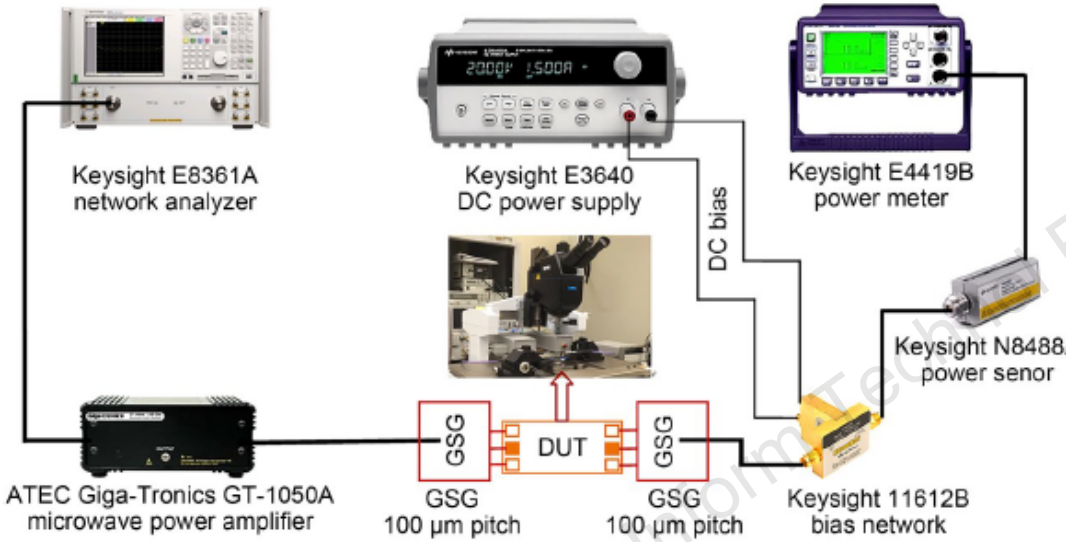
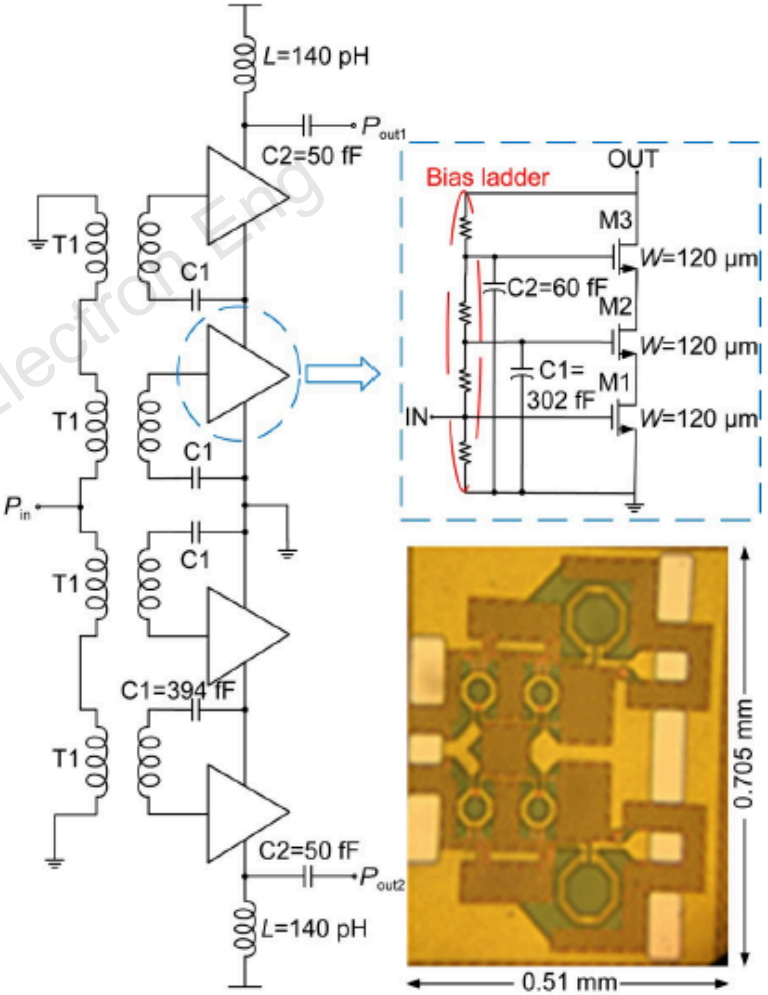
Differential mm-Wave CMOS PA design and demonstration





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Differential mm-Wave CMOS PA design and demonstration

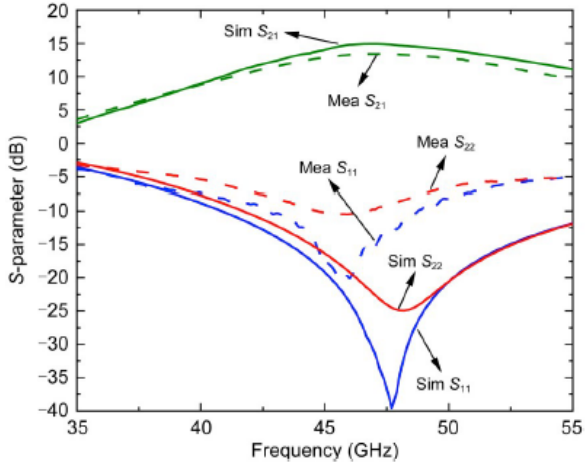

Fig. 9 Simulated (solid line) and measured (dashed line) *S*-parameters of the fabricated differential PA4 chip under 6 V supply

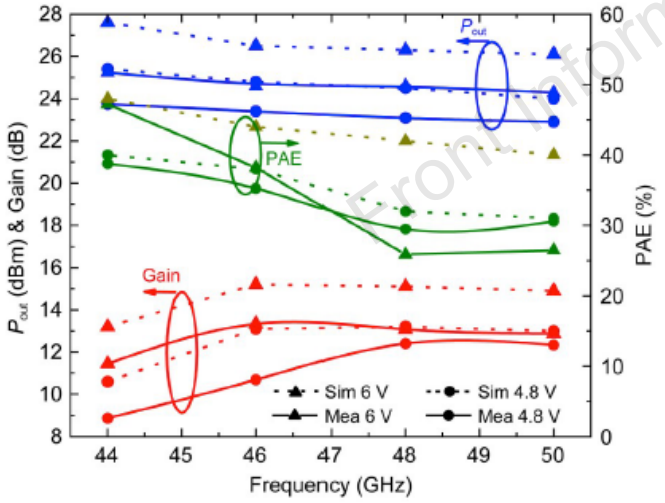

Fig. 11 Simulated and measured power P_{out}, Gain, and PAE vs. frequency for the differential PA (PA4) under two bias conditions (4.8 V and 6 V)

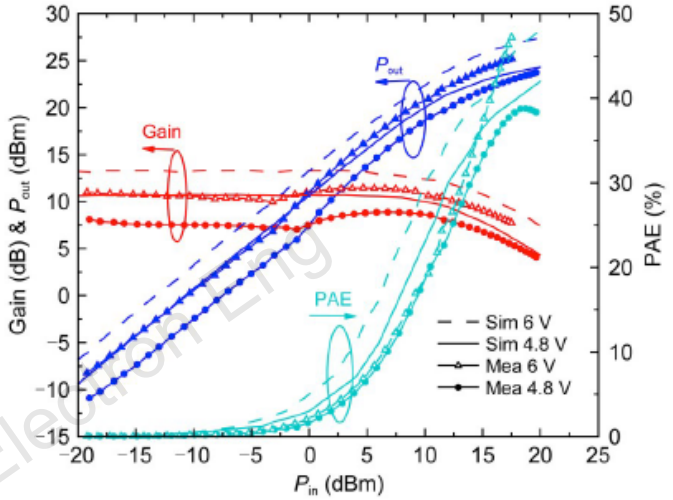

Fig. 10 Simulated and measured power for the differential PA (PA4) at 44 GHz under two bias conditions (4.8 V and 6 V)

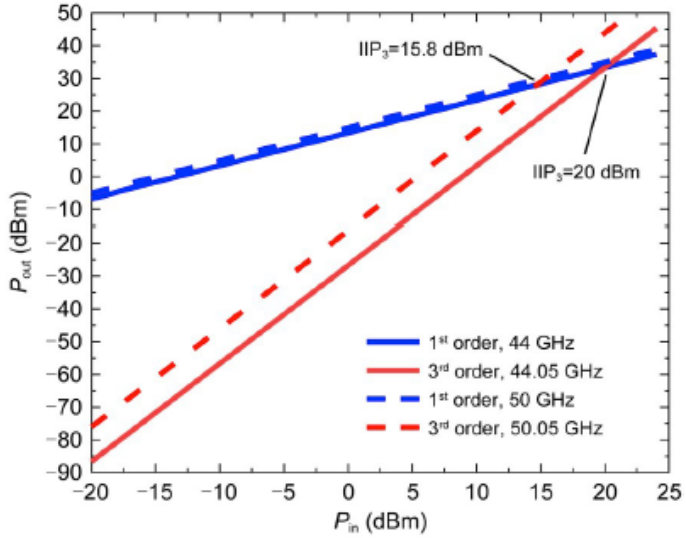

Fig. 12 IIP$_3$ simulation results of the differential PA4

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Conclusions

- For mm-Wave amplifiers, CMOS SOI shows its advantages in power and efficiency. To improve the linearity of the circuit, the parasitic parameters that affect are derived and analyzed.
- A linearity analysis that takes into account the nonlinearities of the transistor current and capacitances is introduced.
- A state-of-art U-band high linearity and efficiency CMOS PA is proposed and demonstrated in 45 nm CMOS SOI technology.

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