Seyed Sajad AHMADPOUR, Nima Jafari NAVIMIPOUR, Mohammad MOSLEH, Senay YALCIN, 2023. Nano-design of ultra-efficient reversible block based on quantum-dot cellular automata. *Frontiers of Information Technology & Electronic Engineering*. 24(3):447-456. https://doi.org/10.1631/FITEE.2200095

Nano-design of ultra-efficient reversible block based on quantum-dot cellular automata

Key words: Nanotechnology; Reversible logic; Energy dissipation; Quantum-dot cellular automata (QCA); Reversible gate; Miller algorithm

Corresponding author: Nima Jafari NAVIMIPOUR
E-mail: Nima.navimipour@khas.edu.tr
ORCID:https://orcid.org/0000-0002-5514-5536

Motivation

1. A reversible block structure with a low quantum cost is conservative if the EXOR of the inputs and the EXOR of the outputs are equivalent.

2. Quantum synthesis of the proposed block is performed using the Miller's algorithm.

3. Two non-resistant QCA reversible block and fault-tolerant reversible block structures are implemented in QCA technology. Afterward, fault-tolerant reversible ANG (Ahmadpour Navimpour Gate) is implemented by the 2DW clocking scheme. Then, the proper function of the proposed structure is verified by a physical investigation. Furthermore, the power consumption of the suggested ANG block is assessed under different energy ranges (0.5Ek, 1Ek, and 1.5Ek).

Main idea

1. Suggesting a reversible gate called ANG based on a worthwhile method like the Miller algorithm to emphasize low quantum cost.
2. Proposing an ANG based on QCA technology with a low occupied area and low energy consumption.
3. Suggesting an ANG using two non-resistant QCA ANG and fault-tolerant reversible ANG structures in QCA technology focusing on low energy consumption.
4. Verifying the proposed fault-tolerant ANG design using physical proofs.
5. Investigating the proposed QCA designs in terms of the number of cells, clock cycles (latency), and area.

Method

1. We used the Miller synthesis to calculate the proposed block's optimal quantum cost.
2. Steps were taken to implement the proposed block based on the Miller synthesis:

- Stage 1: Identify TF2(***P***, ***Q***);
- Stage 2: Identify TF3(***R***, ***Q***, ***P***);
- Stage 3: Identify TF2(***P***, ***Q***);
- Stage 4: Identify TF3(***P***, ***Q***, ***R***);
- Stage 5: Identify TF3(***P***, ***R***, ***Q***);
- Stage 6: Identify TF3(***P***, ***Q***, ***R***).

Major results

1. Power consumption analysis of the suggested reversible gates

Table 2 Power consumption analysis of reversible gates

Design	Average leakage energy dissipation (eV)			Average switching energy dissipation (eV)			Total energy dissipation (eV)		
	0.5Ek	1.0Ek	1.5Ek	0.5Ek	1.0Ek	1.5Ek	0.5Ek	1.0Ek	1.5Ek
DFG (Feynman, 1986)	270.58	758.27	1001.41	658.25	518.67	491.01	928.83	1276.94	1492.42
FRG (Fredkin and Toffoli, 1982)	101.53	283.69	482.40	213.78	175.64	143.28	315.31	459.33	625.68
NFT (Haghparast and Navi, 2008a)	60.58	178.31	299.54	154.35	125.36	107.94	214.93	303.67	407.48
PPRG (Roohi et al., 2018)	58.04	168.07	294.34	193.07	166.15	141.80	251.11	334.22	436.14
PNM1 (Noorallahzadeh and Mosleh, 2020)	100.25	301.57	599.35	611.71	519.69	421.15	711.96	821.26	1020.50
PNM2 (Noorallahzadeh and Mosleh, 2020)	105.46	333.26	606.10	624.61	538.28	453.59	730.07	871.54	1059.38
NMG4 (Noorallahzadeh and Mosleh, 2019)	59.44	171.07	274.34	198.77	167.85	162.90	258.21	338.92	437.24
SCV (Kundu et al., 2022)	56.05	166.41	279.27	168.01	124.70	110.45	224.06	291.11	389.72
Non-resistant QCA ANG	58.78	168.81	268.52	147.14	114.39	104.24	205.92	283.20	372.76
Fault-tolerant QCA ANG	199.49	341.97	516.34	364.81	295.13	242.30	564.30	637.10	758.64

Major results (Cont'd)

2. Evaluation of proposed QCA-based circuits cost indicates significant superiority.

Table 3 Cost comparison of the QCA-reversible blocks

Design	M	I	T^*	C	Cost function
DFG (Feynman, 1986)	$8n$	$3n$	1.50 (6)	$4n$	498
FRG (Fredkin and Toffoli, 1982)	$6n$	$2n$	1.50 (6)	$5n$	378
NFT (Haghparast and Navi, 2008b)	$8n$	$5n$	1.25 (8)	$4n$	680
PPRG (Roohi et al., 2018)	$6n$	$6n$	1.25 (5)	$3n$	255
PNM1 (Noorallahzadeh and Mosleh, 2020)	$7n$	$3n$	2.75 (11)	$6n$	968
PNM2 (Noorallahzadeh and Mosleh, 2020)	$6n$	$2n$	2.50 (10)	$6n$	740
Non-resistant QCA ANG	$9n$	$3n$	1.75 (7)	$3n$	651
Fault-tolerant QCA ANG	$9n$	$3n$	1.25 (5)	$3n$	465

M, I, and C represent the numbers of majority voters, inverters, and crossings, respectively, and T represents the delay. * The number in the brackets represents the number of clock cycles

Conclusions

1. This paper first presented a conservative reversible gate called ANG. Then, the gate was used to develop two non-resistant and fault-tolerant QCA layout structures implemented in QCA technology.

2. Fault-tolerant QCA was implemented based on popular clocking 2DW. In addition, the proposed reversible ANG was validated through the Miller algorithm.

Conclusions

3. The simulations of circuits and their power consumption analysis were performed using QCADesigner 2.0.03 and QCAPro tools, respectively, and the power consumption of the suggested reversible ANG showed 4.19%, 6.74%, and 8.52% improvement over the NFT design corresponding to three levels of 0.5Ek, 1.0Ek, and 1.5Ek, respectively.

4. All three input Boolean functions to 13 standard functions of the proposed block showed that the suggested reversible block was superior to recent designs.

Seyed Sajad AHMADPOUR was born in Iran in 1990. He is a post-doctor and research assistant in the Department of Computer Engineering, Kadir Has University, Istanbul, Türkiye. He is the editor of various journals. His interests are quantum-dot cellular automata, reversible logic, atomic silicon, and fault-tolerance.

Nima Jafari NAVIMIPOUR (Associate Professor) received his BSc, MSc, and PhD degrees in computer engineering from Islamic Azad University, Iran, in 2008, 2009, and 2014, respectively. He is a technical committee member, guest editor, and associate editor of some high-ranked journals such as *IET Quantum Communication*, *Optik*, *Journal of Management & Organization*, *Computer Communications*, *Cluster Computing*, and *Kybernetes*. Furthermore, he is a chair member of many prestigious conferences and a reviewer of several high-ranked journals. He has been giving invited tutorials/talks in IEEE conferences and has been invited to give lectures in different universities. He also won the Publons Top Peer Review Awards in 2018 and 2019. He has been featured among the World's Top 2% Scientists List, according to a conducted study by US-based Stanford University in 2020. He is also a senior member of IEEE, IEEE Communications Society and IEEE Young Professionals. His research interests include green computing, cloud and distributed computing, Internet of Things (IoT), Software-Defined Networking (SDN), information systems, computational intelligence, evolutionary computing, and quantum computing. He has published many papers in various journals and conference proceedings as well as supervising/co-supervising several PhD and Master students in these research areas.

Mohammad MOSLEH is an associate professor at Islamic Azad University, Dezful, Iran. His research interests are audio security (watermarking and steganography) and nano-computing including quantum-dot cellular automata and reversible circuits.

Senay YALCIN is a professor at Nisantasi University. YALCIN received his undergraduate degree from the Department of Physics and Mathematics at Ege University. He completed his master's degree in Nuclear Sciences and his doctorate in Nuclear Sciences at Ege University. He was a post-doctoral research fellow in the field of hydrogen energy at the University of Miami Clean Energy Center. He worked as a researcher on photoelectron spectrography at Montana State University. He served as the Head of the Department of Mathematics and Computer Sciences at Bahçeşehir University. His research focuses on nuclear energy, geometric augmented product codes, separable codes, soft calculations, Monte Carlo Computation in nuclear reactors and neuro-fuzzy interference system. He is the editor of various journals.