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Traffic-oriented reconfigurable NoC with augmented inter-port buffer sharing

Key words: Network-on-chip; Reconfigurable; Traffic-oriented; Buffer sharing

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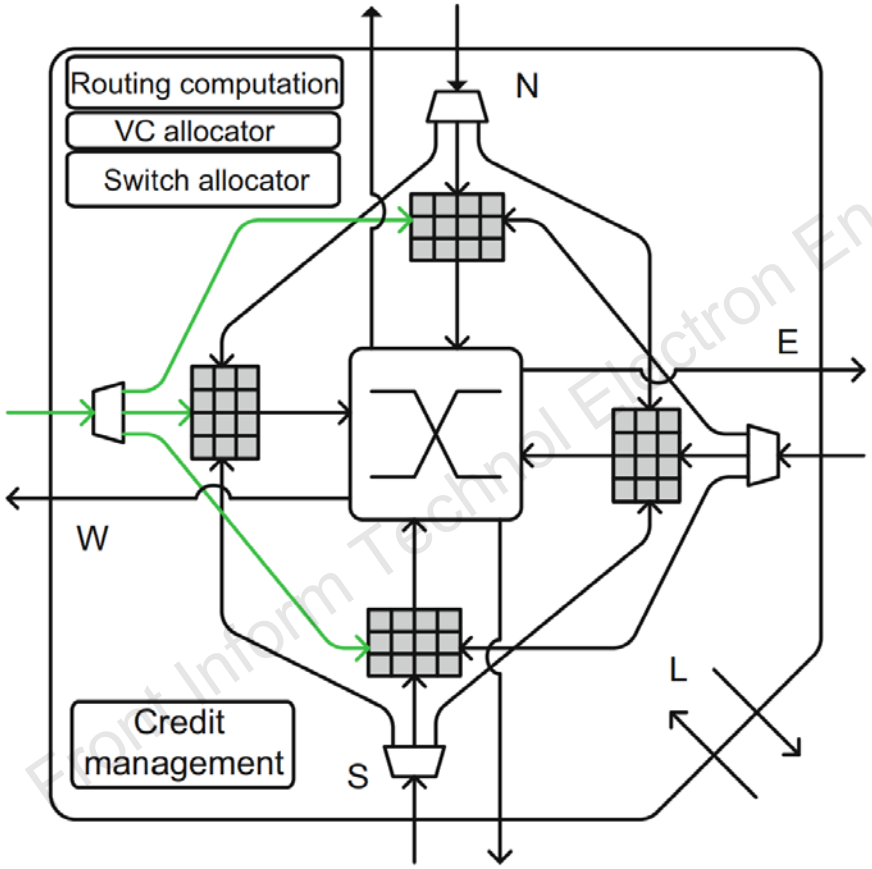
Motivation

- The performance of the conventional network-on-chip (NoC) architecture cannot meet the requirements of growing communication complexity and intensive communication. The traffic within NoC varies across time as well as spatial regions, making the traffic exhibit spatial–temporal variation. Therefore, the design of future NoC is expected to be dynamically reconfigured to satisfy time-varying traffic loads.
- The congestion status of each port within the router varies greatly with the variation of traffic load, resulting in part of the buffer resources remaining underutilized.

Main idea

- We propose a traffic-oriented reconfigurable NoC (TOR-NoC) that modifies the input port to support buffer sharing between adjacent ports. Specifically, the modified input port can be reconfigured dynamically to handle on-demand traffic.
- We present the centralized output-oriented buffer management that works well with the reconfigurable input ports.
- Together with the modified input port and enhanced buffer management, we present a method of reconfigurable routing under which packets shared in an adjacent port compete for the output of that adjacent port, thus reconfiguring the transmission path of data.

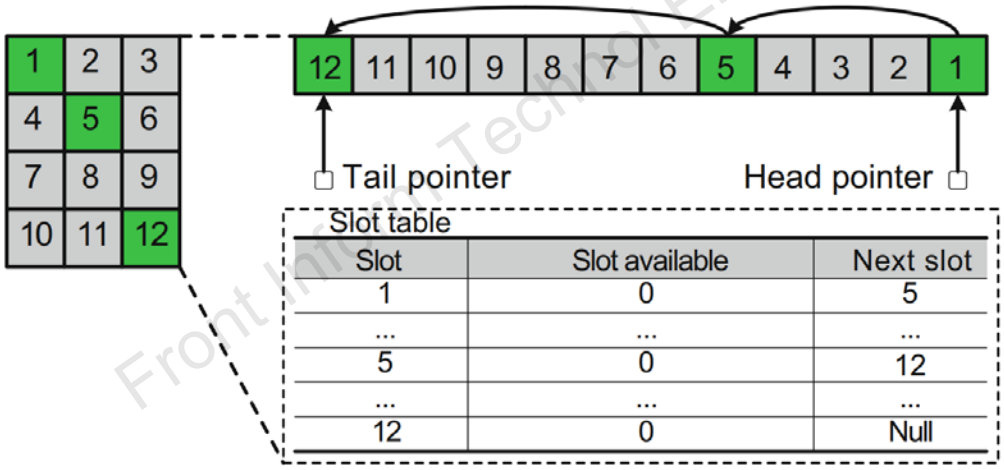
Microarchitecture



The microarchitecture of the traffic-oriented reconfigurable router. The proposed router can perform reconfiguration using DEMUX according to current communication on-demand traffic. As depicted by the solid green lines, the three green lines are candidates for reconfigurable paths.

Method

To avoid the conflicts between the current port and the adjacent port, we present the centralized output oriented buffer management that works well with the reconfigurable input ports.



When an arriving flit enters the current port, it goes to the VC pointed by the pointer according to its VC_ID; the tail pointer is shifted to point to the newly arriving flit, and slot available is set to 0.

Results

Table 2 The experimental parameters

Parameter	Value/Description
Topology	4×4 and 8×8 2D mesh
Channel width	64
Number of VCs	4 or dynamic
Input buffer	4-flit depth or dynamic
Routing	XY routing algorithm
Traffic pattern	Uniform, transpose, bit-reversal, and shuffle

Table 3 Area of the three router architectures

Module	Area (μm^2)		
	Baseline	Said et al. (2021)'s	TOR-NoC
Input port	10 147.8	10 832.6	10 755.4
Crossbar	301.3	306.5	309.1
Logic unit	1237.3	1273.8	1298.0
Total	11 686.4	12 412.9	12 362.5
Normalized	1.000	1.062	1.058

Results

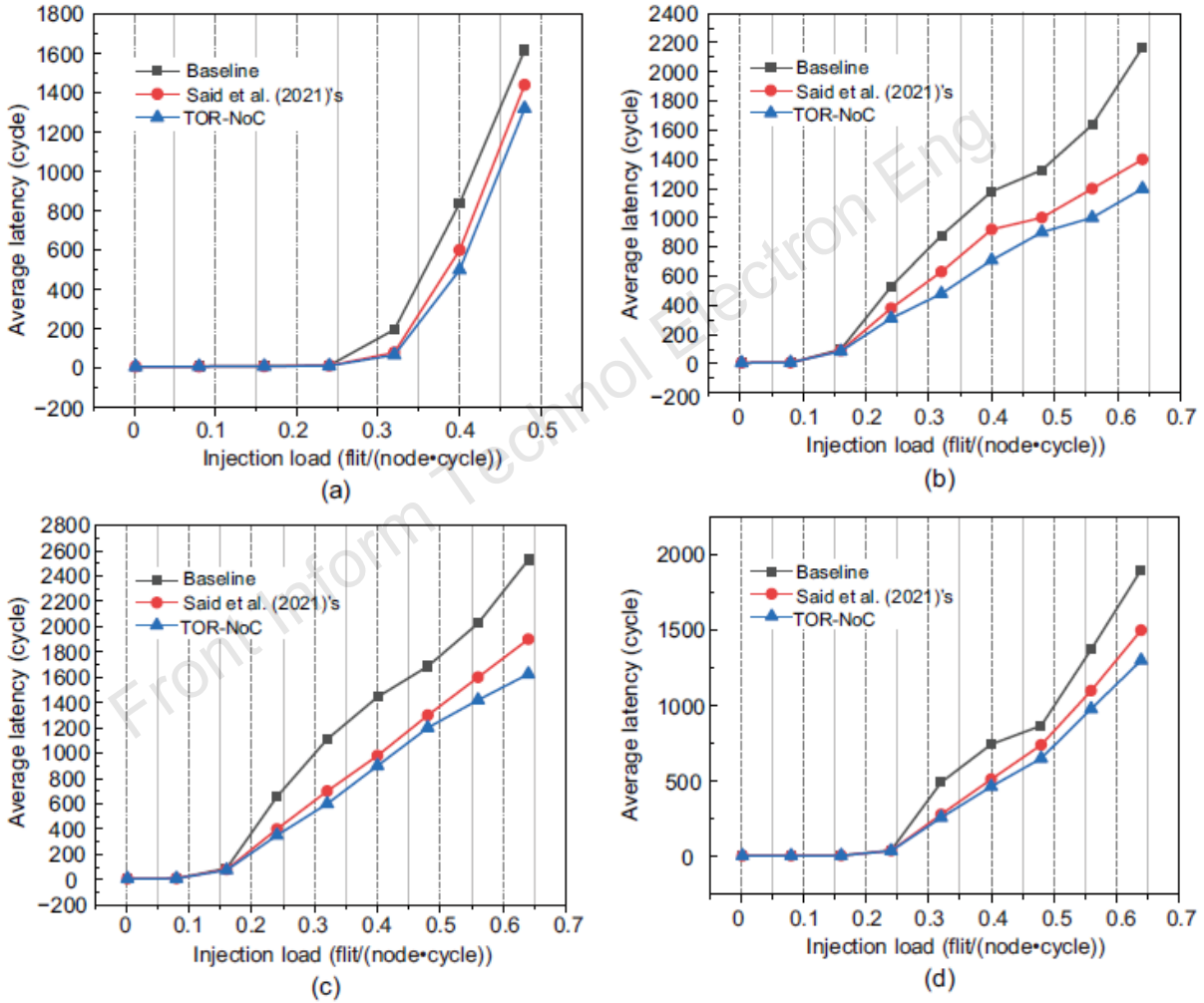


Fig. 7 Network average latency with different injection loads under different traffic workloads in a 4×4 2D mesh: (a) uniform; (b) transpose; (c) bit-reversal; (d) shuffle

Conclusions

In this work, traffic-oriented reconfigurable routers have been presented as an alternative for baseline routers. A reconfiguration mechanism is proposed that dynamically stores newly arriving packets on current or adjacent ports. At the same time, the use of centralized output-oriented buffer management facilitates a further enhancement in the performance of the reconfigurable NoC proposed in the present research. Therefore, our reconfigurable NoC provides the needed flexibility along with balancing hardware cost and communication.

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