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Data-driven intermittent connection fault diagnosis for complex topology DeviceNet based on Bayesian inference

Key words: DeviceNet; Fieldbus; Complex topology; Fault diagnosis; Intermittent connection; Bayesian inference

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Motivation

- As the topology of DeviceNet in industrial automation systems grows more complex and the reliability requirement for industrial equipment and processes becomes more stringent, the importance of network troubleshooting is increasingly evident.
- Intermittent connection (IC) faults frequently occur in DeviceNet systems, impairing production performance and even operational safety. However, existing IC troubleshooting methods for DeviceNet, especially those with complex topologies, cannot directly handle multi-fault scenarios, which require human intervention for a full diagnosis.
- In this paper, a novel data-driven IC fault diagnosis method based on Bayesian inference is proposed for DeviceNet with complex topologies, which can accurately and efficiently localize all IC faults.

Main idea

- An accurate and efficient data-driven diagnostic framework is designed by formalizing the IC fault location problem as a Bayesian problem for dealing with the fault occurrence probability from symptom data, which can determine the full locations of IC faults in a single diagnosis.
- A rapid fault localization algorithm based on Bayesian inference of fault likelihoods, generalized to various network topologies, is developed, which has lower computational complexity than existing algorithms and can thus be extended to large industrial systems.
- This method provides a practical-to-implement data acquisition (DAQ) scheme that needs to attach sensors only to the open ports at the network ends to diagnose the entire network, without the need to deploy them at the unreachable network interior as existing methods.

Method

- Overall framework

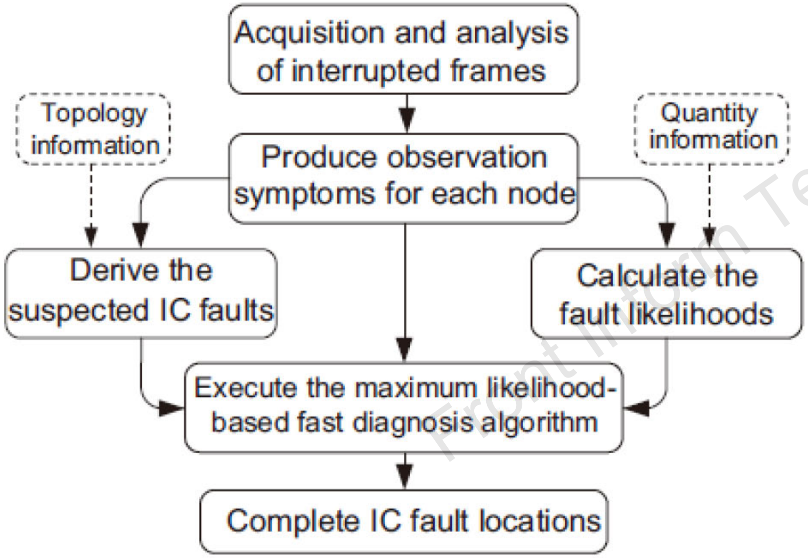


Fig. 2 Framework of the proposed methodology

- Definition of observation symptoms

$$\begin{cases} \mathfrak{a}_{N_i}^{<1>} = (e_{s_1}^{<1>}, e_{s_2}^{<1>}, \cdots, e_{s_z}^{<1>}), \\ \mathfrak{a}_{N_i}^{<2>} = (e_{s_1}^{<2>}, e_{s_2}^{<2>}, \cdots, e_{s_z}^{<2>}), \\ \vdots \\ \mathfrak{a}_{N_i}^{<m_i>} = (e_{s_1}^{<m_i>}, e_{s_2}^{<m_i>}, \cdots, e_{s_z}^{<m_i>}), \end{cases}$$

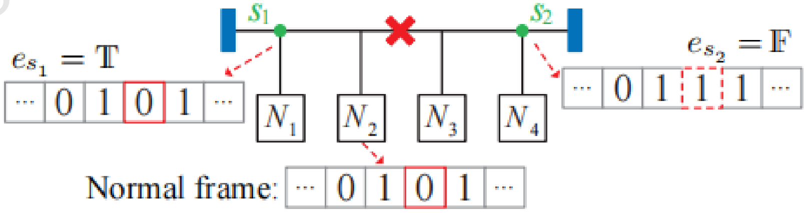


Fig. 3 Illustration of the error events

- Derivation of the suspected IC faults

$$\mathcal{F}_{N_i}^{<t>} = \left\{ f_j \,\middle|\, j \in \left(\mathcal{L} - \bigcup_{e_{s_k}^{<t>} = \mathbb{T}} \mathcal{L}_{N_i - s_k} \right) \bigcap \left(\bigcap_{e_{s_k}^{<t>} = \mathbb{F}} \mathcal{L}_{N_i - s_k} \right) \right\}$$

Method

- Likelihood of the suspected IC faults

$$\mathfrak{C}_{f_j} = \frac{1}{d}\sum_{v=1}^{d} \Pr(f_j|\mathfrak{a}_{\mathrm{o}}^{(v)}),$$

where

$$\Pr(f_j|\mathfrak{a}_{\mathrm{o}}^{(v)}) = \frac{\Pr(\mathfrak{a}_{\mathrm{o}}^{(v)}|f_j)\Pr(f_j)}{\sum_{i=1}^{u}\Pr(\mathfrak{a}_{\mathrm{o}}^{(v)}|f_i)\Pr(f_i)}.$$

$$\Pr(\mathfrak{a}_{\mathrm{o}}^{(v)}|f_j) = \frac{\mathcal{Q}(\mathfrak{a}_{\mathrm{o}}^{(v)})}{\sum\limits_{\mathfrak{a}_{\mathrm{o}}^{(c)}:f_j\in\mathcal{F}_{\mathrm{o}}^{(c)}} \mathcal{Q}(\mathfrak{a}_{\mathrm{o}}^{(c)})}, \forall f_j \in \bigcup_{v=1}^{d}\mathcal{F}_{\mathrm{o}}^{(v)},$$

$$\begin{cases} \min\limits_{\Pr(f_j):f_j\in\bigcup\limits_{v=1}^{d}\mathcal{F}_{\mathrm{o}}^{(v)}} \sum_{v=1}^{d}\left|\hat{\Pr}(\mathfrak{a}_{\mathrm{o}}^{(v)})-\Pr(\mathfrak{a}_{\mathrm{o}}^{(v)})\right|^2 \text{ s.t.} \\ \hat{\Pr}(\mathfrak{a}_{\mathrm{o}}^{(v)}) = \sum_{i=1}^{u}\Pr(\mathfrak{a}_{\mathrm{o}}^{(v)}|f_i)\Pr(f_i), \\ \Pr(\mathfrak{a}_{\mathrm{o}}^{(v)}) = \dfrac{\mathcal{Q}(\mathfrak{a}_{\mathrm{o}}^{(v)})}{\sum_{x=1}^{d}\mathcal{Q}(\mathfrak{a}_{\mathrm{o}}^{(x)})}, \quad 0\le\Pr(f_j)\le 1. \end{cases}$$

- Maximum likelihood-based fast diagnosis algorithm

Algorithm 1 Maximum likelihood-based fast diagnosis (MLBFD)

```
Initialization: $F_{\mathrm{R}} = \bigcup_{\mathfrak{a}_{\mathrm{o}}^{(v)}\in\mathcal{S}_{\mathrm{o}}} \mathcal{F}_{\mathrm{o}}^{(v)}, \mathcal{S}_{\mathrm{R}} = \mathcal{S}_{\mathrm{o}}, \mathcal{H} = \varnothing$
MLBFD($F_{\mathrm{R}}, \mathcal{S}_{\mathrm{R}}$):
for all $f_j \in F_{\mathrm{R}}$ do
    $F_{\max} \leftarrow \varnothing$
    if $\mathfrak{C}_{f_j}$ is maximum then
        $F_{\max} \leftarrow F_{\max} \bigcup \{f_j\}$
    end if
end for
for all $f_j \in F_{\max}$ do
    $\mathcal{H} \leftarrow \mathcal{H} \bigcup \{f_j\}$
    $\mathcal{S}_{\mathrm{R}} \leftarrow \mathcal{S}_{\mathrm{R}} - \bigcup_{f_j\in\mathcal{H}} \mathcal{S}_{f_j}$
    if $\mathcal{S}_{\mathrm{R}} = \varnothing$ then
        return $\mathcal{H}$
    else
        $F_{\mathrm{R}} \leftarrow \bigcup_{\mathfrak{a}_{\mathrm{o}}^{(v)}\in\mathcal{S}_{\mathrm{R}}} \mathcal{F}_{\mathrm{o}}^{(v)}$
        return MLBFD($F_{\mathrm{R}}, \mathcal{S}_{\mathrm{R}}$)
    end if
end for
```

Results

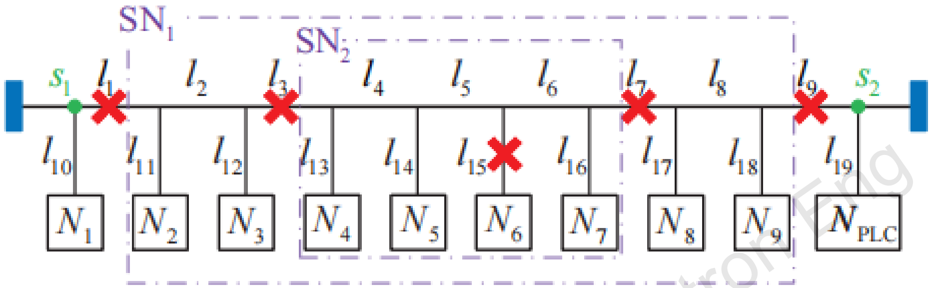
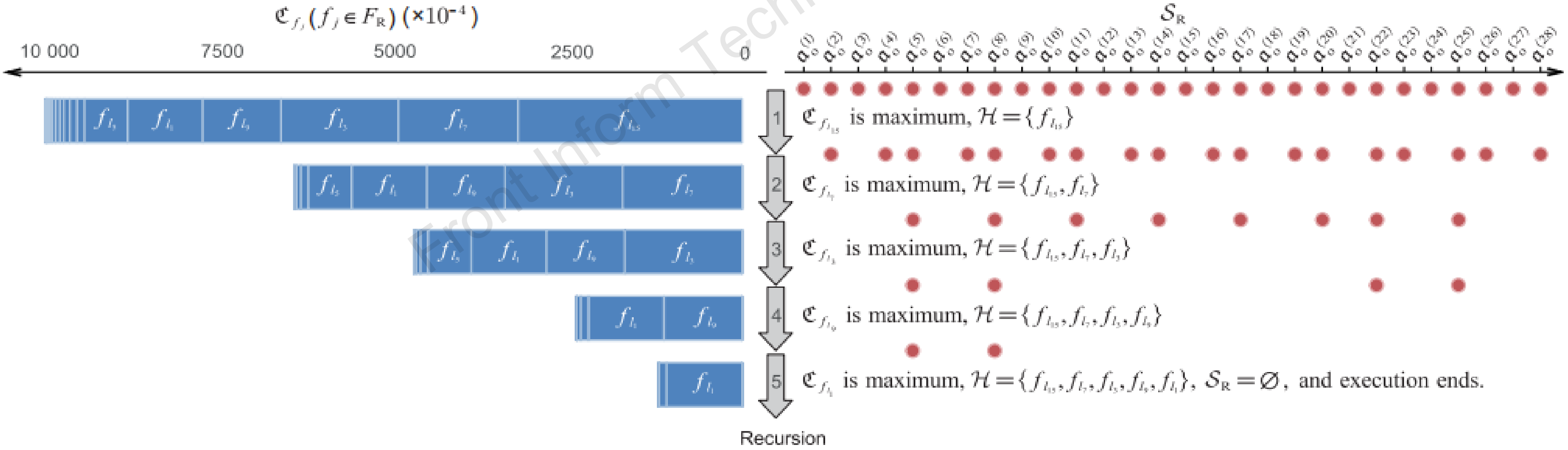


Fig. 5 Experimental setup in case study 1



$\mathfrak{C}_{f_{l_{15}}}$ is maximum, $\mathcal{H}=\{f_{l_{15}}\}$

$\mathfrak{C}_{f_{l_7}}$ is maximum, $\mathcal{H}=\{f_{l_{15}}, f_{l_7}\}$

$\mathfrak{C}_{f_{l_3}}$ is maximum, $\mathcal{H}=\{f_{l_{15}}, f_{l_7}, f_{l_3}\}$

$\mathfrak{C}_{f_{l_9}}$ is maximum, $\mathcal{H}=\{f_{l_{15}}, f_{l_7}, f_{l_3}, f_{l_9}\}$

$\mathfrak{C}_{f_{l_1}}$ is maximum, $\mathcal{H}=\{f_{l_{15}}, f_{l_7}, f_{l_3}, f_{l_9}, f_{l_1}\}$, $\mathcal{S}_{\mathrm{R}}=\varnothing$, and execution ends.

Fig. 6 Illustration of the algorithm execution process in case study 1

Results

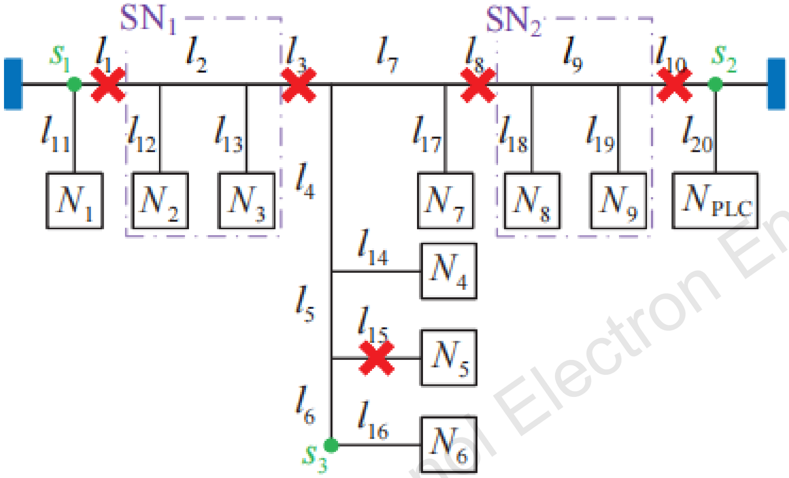


Fig. 7 Experimental setup in case study 2

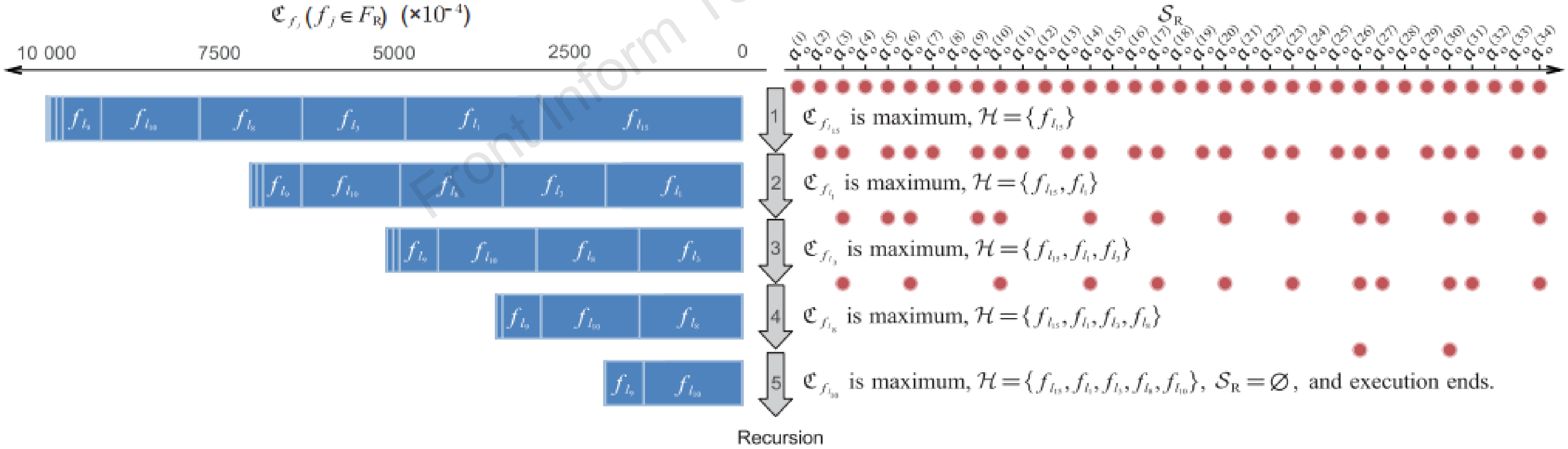


Fig. 8 Illustration of the algorithm execution process in case study 2

Results

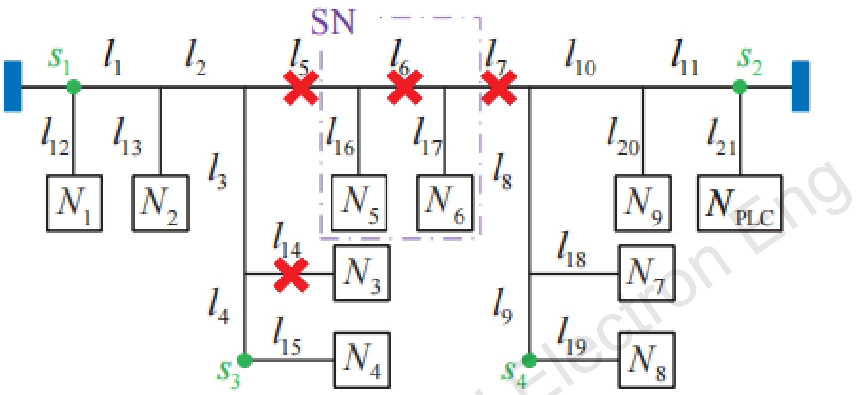


Fig. 9 Experimental setup in case study 3

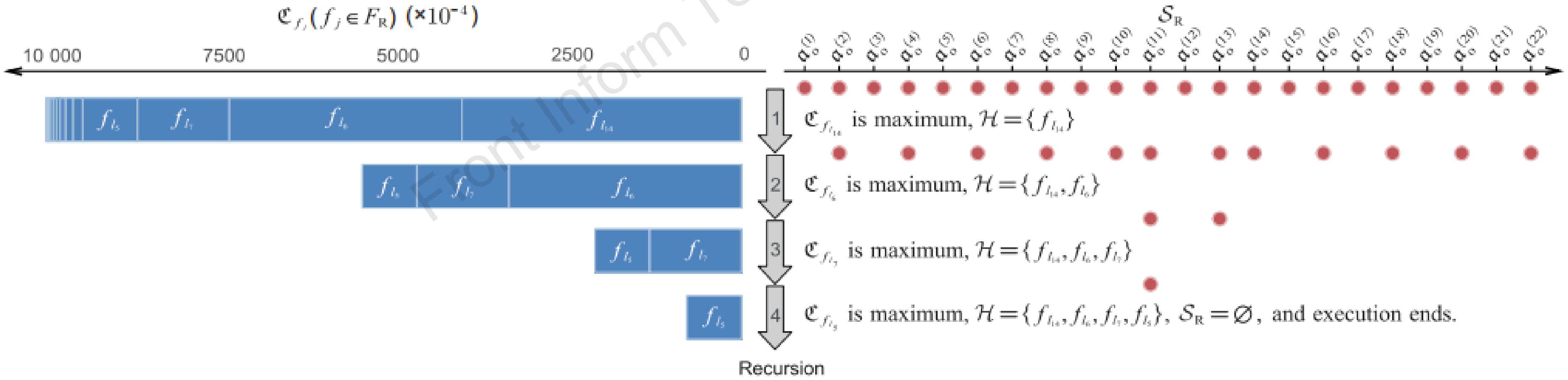


Fig. 10 Illustration of the algorithm execution process in case study 3

Results

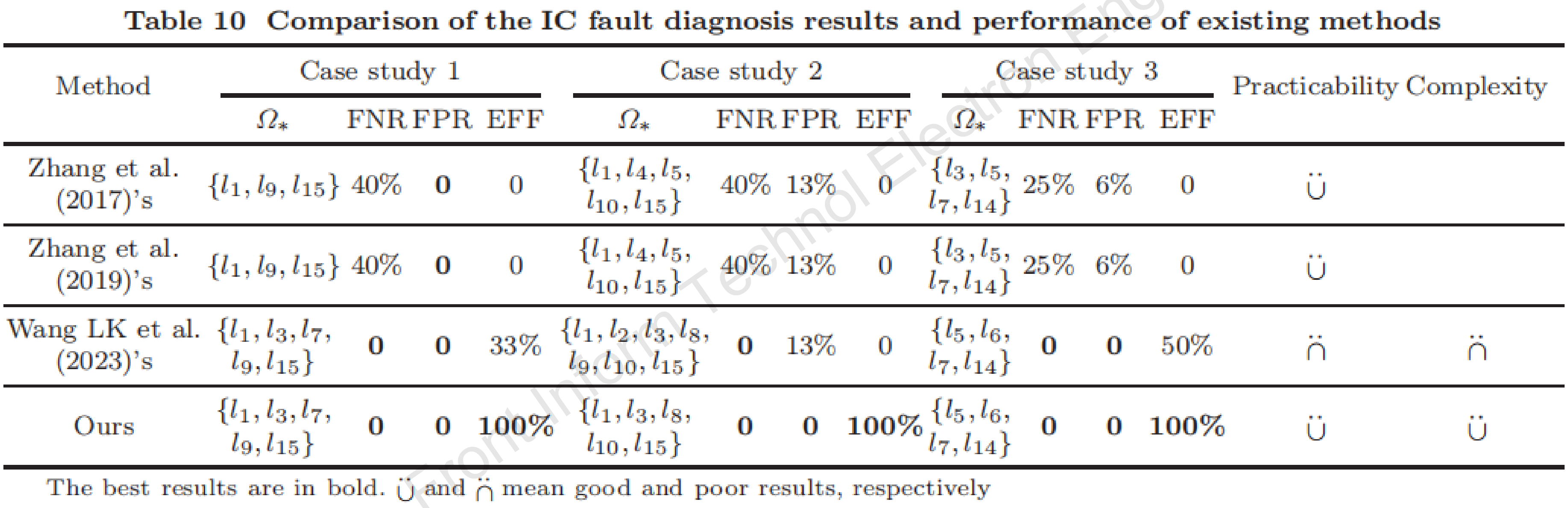


Table 10 Comparison of the IC fault diagnosis results and performance of existing methods

Method	Case study 1				Case study 2				Case study 3				Practicability	Complexity
	Ω_*	FNR	FPR	EFF	Ω_*	FNR	FPR	EFF	Ω_*	FNR	FPR	EFF		
Zhang et al. (2017)'s	$\{l_1, l_9, l_{15}\}$	40%	**0**	0	$\{l_1, l_4, l_5, l_{10}, l_{15}\}$	40%	13%	0	$\{l_3, l_5, l_7, l_{14}\}$	25%	6%	0	∪̈	
Zhang et al. (2019)'s	$\{l_1, l_9, l_{15}\}$	40%	**0**	0	$\{l_1, l_4, l_5, l_{10}, l_{15}\}$	40%	13%	0	$\{l_3, l_5, l_7, l_{14}\}$	25%	6%	0	∪̈	
Wang LK et al. (2023)'s	$\{l_1, l_3, l_7, l_9, l_{15}\}$	**0**	**0**	33%	$\{l_1, l_2, l_3, l_8, l_9, l_{10}, l_{15}\}$	**0**	13%	0	$\{l_5, l_6, l_7, l_{14}\}$	**0**	**0**	50%	∩̈	∩̈
Ours	$\{l_1, l_3, l_7, l_9, l_{15}\}$	**0**	**0**	**100%**	$\{l_1, l_3, l_8, l_{10}, l_{15}\}$	**0**	**0**	**100%**	$\{l_5, l_6, l_7, l_{14}\}$	**0**	**0**	**100%**	∪̈	∪̈

The best results are in bold. ∪̈ and ∩̈ mean good and poor results, respectively

Conclusions

In this paper, we propose a novel data-driven IC fault diagnosis method based on Bayesian inference for DeviceNet with complex topological layouts. The experimental results show that the IC fault locations diagnosed by the proposed method agree well with the experimental setup in various complex topologies and fault scenarios. Further discussion shows that the proposed method is an improvement over existing methods in terms of localization accuracy, diagnostic efficiency, practicality, and algorithm complexity.

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