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One-dimensional reconfigurable three-stage Doherty power amplifier with load mismatch resilience

Key words: Doherty power amplifier; Load mismatch; One-dimensional (1D) control; Reconfigurable; Three-stage

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Motivation

Targeting the inadequacy of current analysis on the resilience of three-stage Doherty power amplifiers (DPAs) under load mismatch conditions and the complexity of traditional resilience enhancement solutions, a novel reconfigurable three-stage DPA architecture based on exceptionally simple circuits and a one-dimensional (1D) control method is proposed, which can significantly enhance the resilience to load mismatch.

Main idea

- A novel three-stage DPA architecture is proposed which provides a large high-efficiency range against load mismatch, through the utilization of a 1D control method.
- A simple 1D control circuit is introduced to enhance mismatch resilience by changing reactance conditions at a single control port in the proposed load modulation network (LMN).

Method

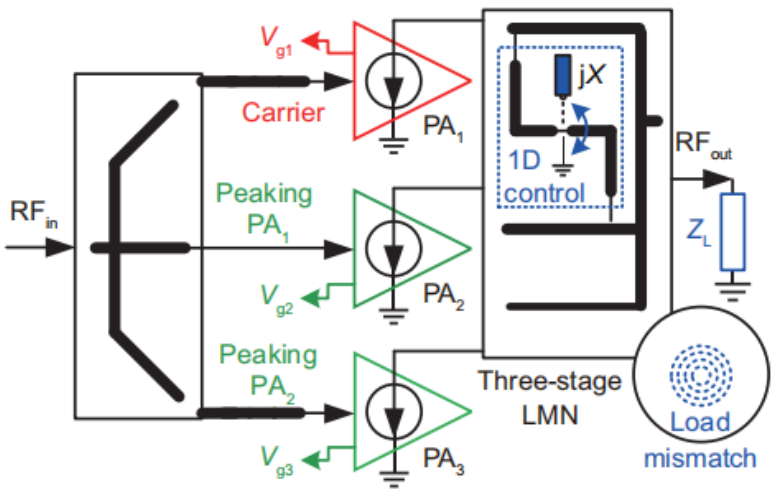

Fig. 1 The proposed three-stage DPA architecture (RF: radio frequency)

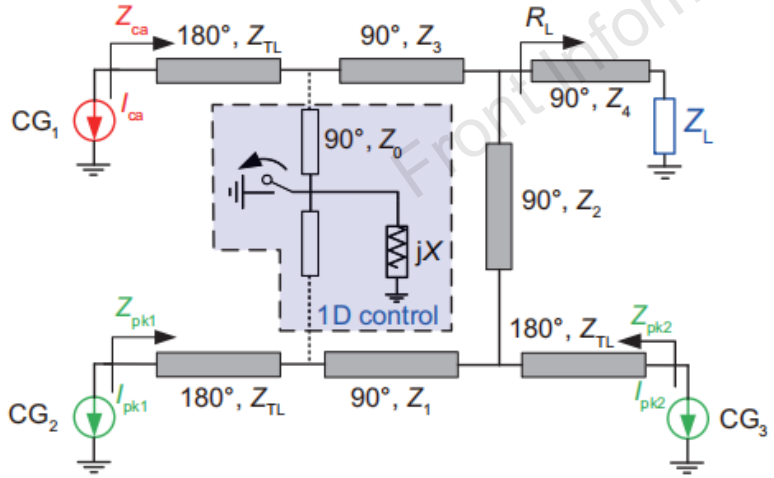

Fig. 2 Theoretical block diagram of the proposed sub-network (TL: transmission line)

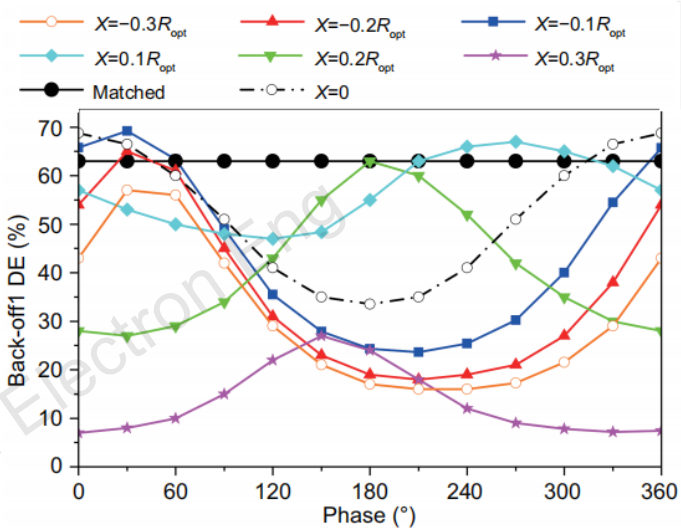

Fig. 6 Theoretical DE at OBO1 versus phase with different X values of 1D control

$$\hat{\boldsymbol{Z}}_2 = R_{\text{opt}} \begin{bmatrix} 0 & \frac{-\mathrm{j}2}{1+\beta} & 0 & 0 \\ \frac{-\mathrm{j}2}{1+\beta} & 0 & \frac{+\mathrm{j}}{1+\beta} & \frac{-\mathrm{j}\frac{5}{2\sqrt{3}}}{1-\beta} \\ 0 & \frac{+\mathrm{j}}{1+\beta} & 0 & \frac{-\mathrm{j}\frac{5}{4\sqrt{3}}}{\beta} \\ 0 & \frac{-\mathrm{j}\frac{5}{2\sqrt{3}}}{1-\beta} & \frac{-\mathrm{j}\frac{5}{4\sqrt{3}}}{\beta} & 0 \end{bmatrix}, \tag{11}$$

where $\beta = \frac{2x}{z_0^2}$, and z_0 and x are the normalized values of Z_0 and X for R_{opt}, respectively.

Method

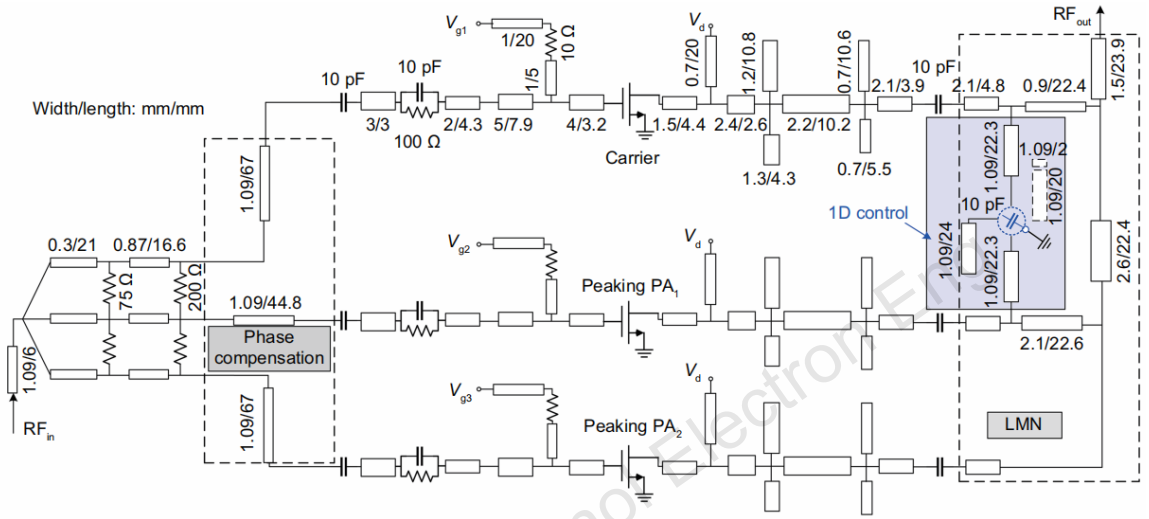

Fig. 10 Circuit details of the proposed three-stage DPA

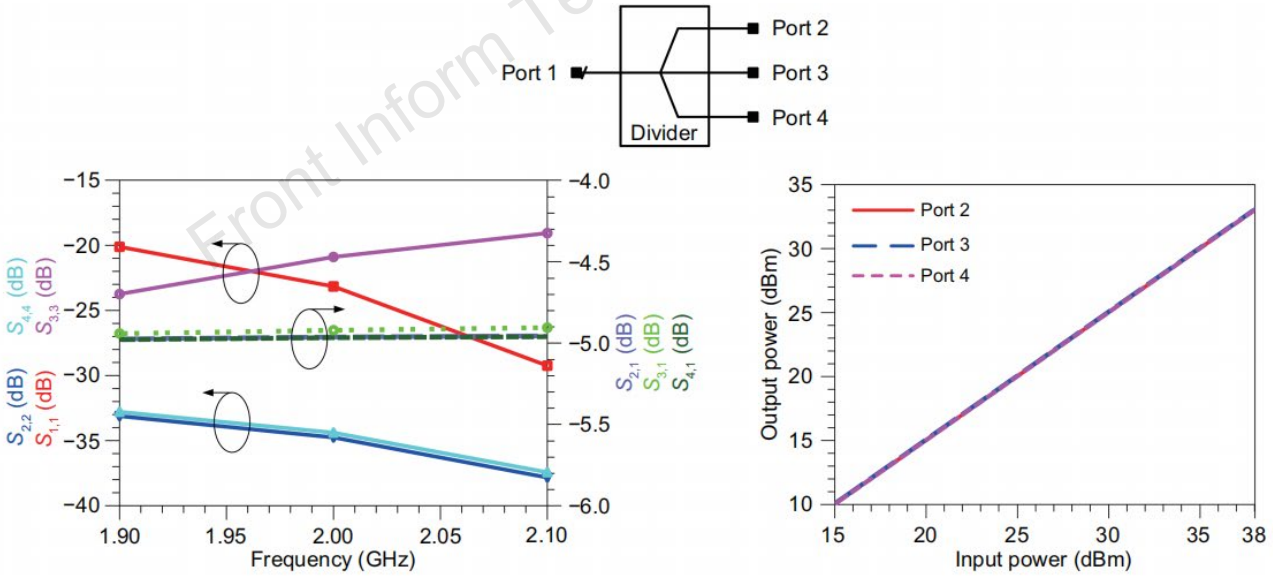

Fig. 11 Simulated *S*-parameters and output power versus input power of the three-way divider (References to color refer to the online version of this figure)

Results

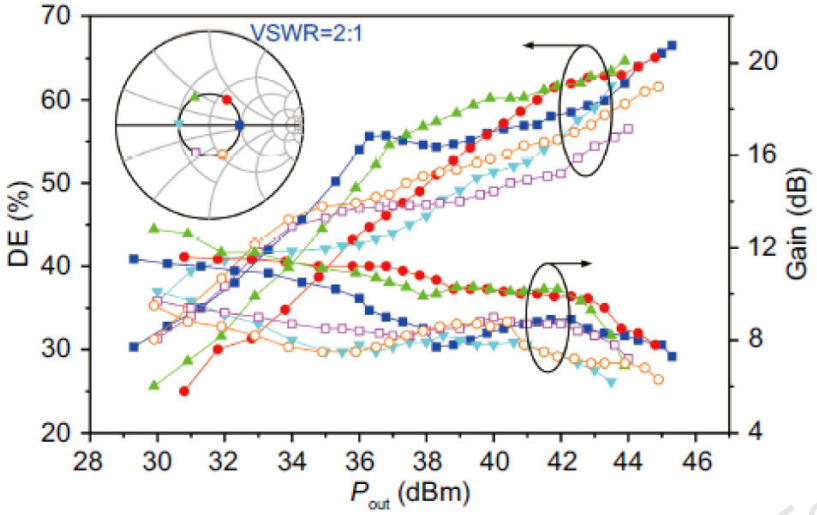

Fig. 20 Measured DE and gain versus output power under different load mismatch conditions

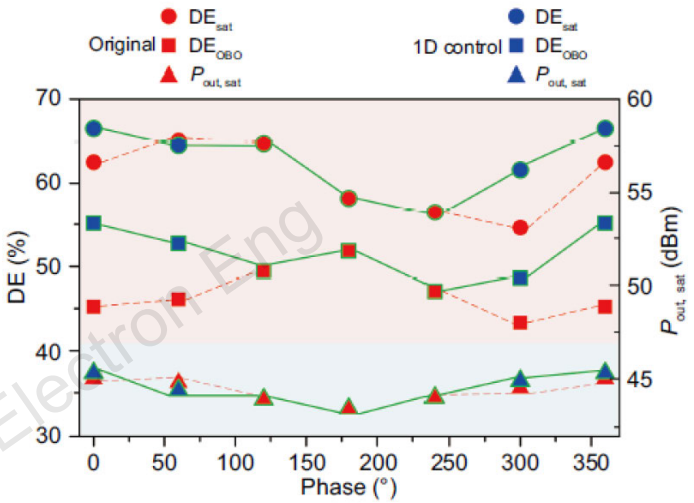

Fig. 21 Measured DE and saturated output power versus phase under different load mismatch conditions when VSWR=2:1 (References to color refer to the online version of this figure)

Table 1 Performance comparison of recently published PAs with load mismatch adaptability

Reference	Frequency (GHz)	Control variable	Load Z_0=50 (Ω) P_{sat} (dBm)	DE_{sat} (%)	OBO (dB)	DE* (%)	VSWR=2:1 P_{sat} (dBm)	DE_{sat} (%)	OBO (dB)	DE* (%)
This work	2	1D	45.2	73.1	9.5	51.0	43.4–45.3	56.5–66.5	8	47.0–55.1
Gonçalves et al. (2022)	3.6	2D	43.5	64	5	53	42.6–43.4	49–64	5	35–46
Shi et al. (2023)	2.4	3D	43.4/43.7	69.1/70.8	6	>60	41.5–43.3	52.8–60.7	6	50.1–62.5
Guo et al. (2023)	2.1	1D	42**	72**	10	64**	39.1–40.9	60.1–66.4	10	43.0–62.8
Pang et al. (2024)	2.0	3D	46.4/46.7	70.3/72.2	9	62.8/60.7	44.8–46.3	50.2–65.8	9	47.8–56.7

* At 8 dB OBO; ** graphically estimated. P_{sat}: saturation output power; DE_{sat}: saturation drain efficiency

Conclusions

In this paper, the load mismatch resilience of three-stage DPA is analyzed based on nonlinear current models. To further improve the mismatch resilience, a novel three-stage DPA with a very simple 1D circuit control method is then proposed. A DPA operating at 2 GHz is designed to verify the proposed method and architecture. The designed DPA has a 9.5 dB OBO DE of 51% for matched load and maintains DE of 47%–55.1% at 8 dB OBO against load mismatch when VSWR=2:1. The proposed three-stage DPA architecture with 1D control offers a brand-new solution to provide load mismatch insensitivity with a very simple circuit configuration.

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