

Emitter-couple logic circuit design based on the threshold-arithmetic algebraic system

基于阈算术代数系统的ECL逻辑电路设计

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1. Emitter-couple logic (ECL) circuits can operate at high switching speeds and allow the power dissipation to remain constant as the frequency increases. Traditional ECL circuit design methods use gates as the basic component based on Boolean algebra; in the theory of differential current switches, switches (transistors) are used as the basic component. In both cases, ECL circuits are treated as voltage-mode circuits, and the internal current signals of ECL circuits are not used, failing to achieve a direct, effective, and simple ECL circuit design.

2. As current signals are easy to add or subtract by simply tying wires with each other, we have proposed the threshold-arithmetic algebraic system (TAAS) for current-mode circuit design. In TAAS the threshold-arithmetic operations, arithmetic operations, and nonnegative operations are defined as basic operations, and the HE map is used to express a threshold-arithmetic function as a Karnaugh map for a logic function.

3. Based on TAAS and the HE map, in this paper we propose the ECL circuit design procedure at the switch level:

- (1) Draw the Karnaugh map of the logical function to be designed, which is the target HE map.
- (2) According to the target HE map and logical function, construct a relatively simple threshold-arithmetic function, for which the HE map is similar to the target HE map.
- (3) Operating on the constructed HE map using threshold-arithmetic, arithmetic, and non-negative operations, we can obtain the final HE map, which is the same as the target HE map.
- (4) According to the operating process of HE map operations, the corresponding threshold-arithmetic functions can be obtained, and the ECL circuits can be designed.

4. Example: Design of an ECL binary three-variable XOR circuit

$x \backslash yz$	00	01	11	10
0	0	1	0	1
1	1	0	1	0

(a)

$x \backslash yz$	00	01	11	10
0	0	1	2	1
1	1	2	3	2

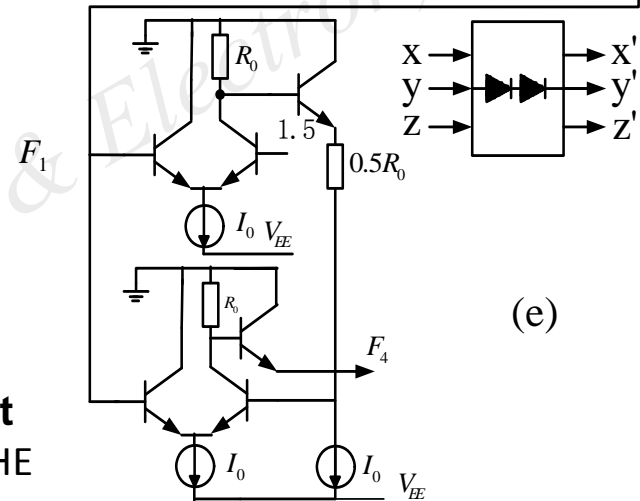
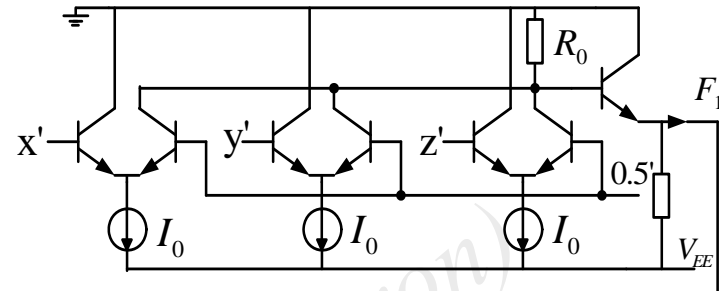
(b)

$x \backslash yz$	00	01	11	10
0	0	1	0	1
1	1	0	0	0

(c)

$x \backslash yz$	00	01	11	10
0	0	0	0	0
1	0	0	1	0

(d)



(e)

Fig. 3 ECL binary three-variable XOR circuit

(a) Karnaugh map of the XOR; (b) HE map of F_1 ; (c) HE map of F_2 ; (d) HE map of F_3 ; (e) XOR ECL circuit

The proposed design method is direct, simple, and effective, and also simplifies the structure of the designed ECL circuits.