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Folded down-conversion mixer for a 60 GHz receiver architecture in 65-nm CMOS technology

Key words: Folded mixer, Current reuse, Low power, Inductorless design, Direct conversion

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Introduction

- The conventional Gilbert mixer is unsuitable for low supply voltages due to its stacked architecture.

- To resolve the problem of voltage headroom and achieve an optimum performance from the mixer in terms of high conversion gain and low noise figure, folded mixer topology must be employed.

- A folded mixer design for a 60 GHz receiver in a 65 nm LP-CMOS process has been presented in this work.

The 60 GHz receiver with emphasis on this work

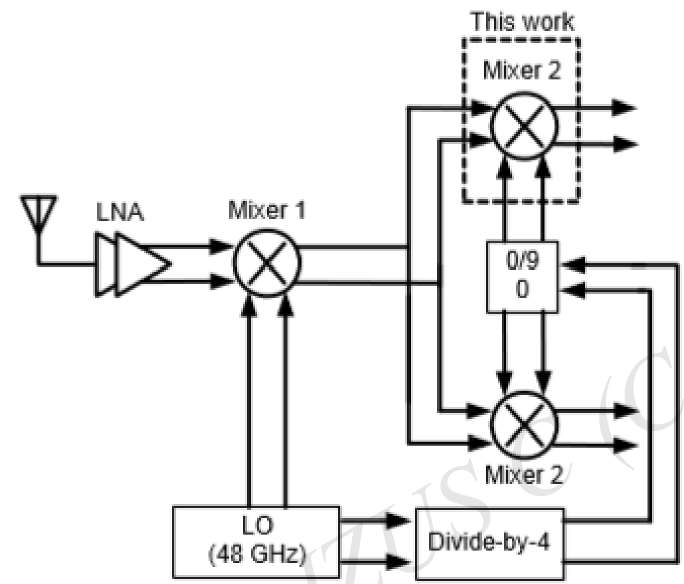

Fig. 1 The 60 GHz receiver architecture with emphasis on this work

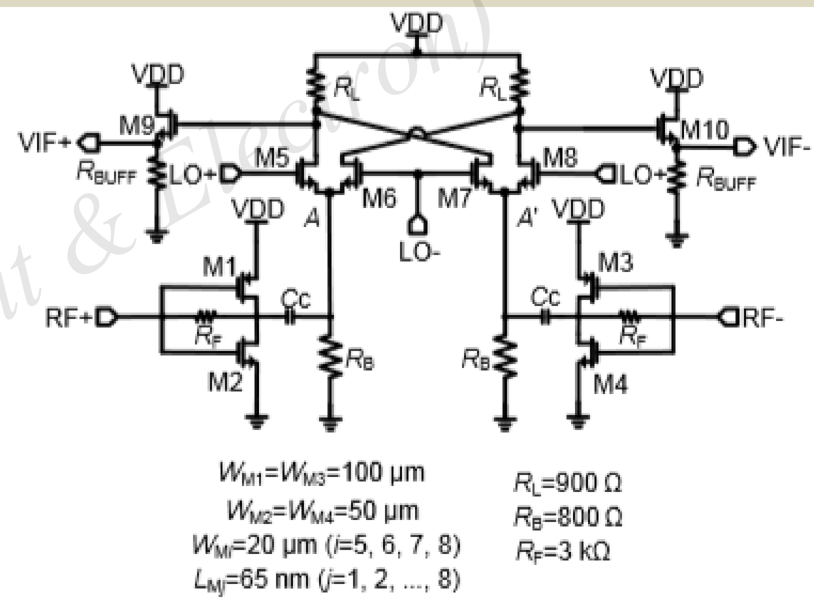

Fig. 2 Schematic of the proposed folded mixer design along with component values

Chip micrograph

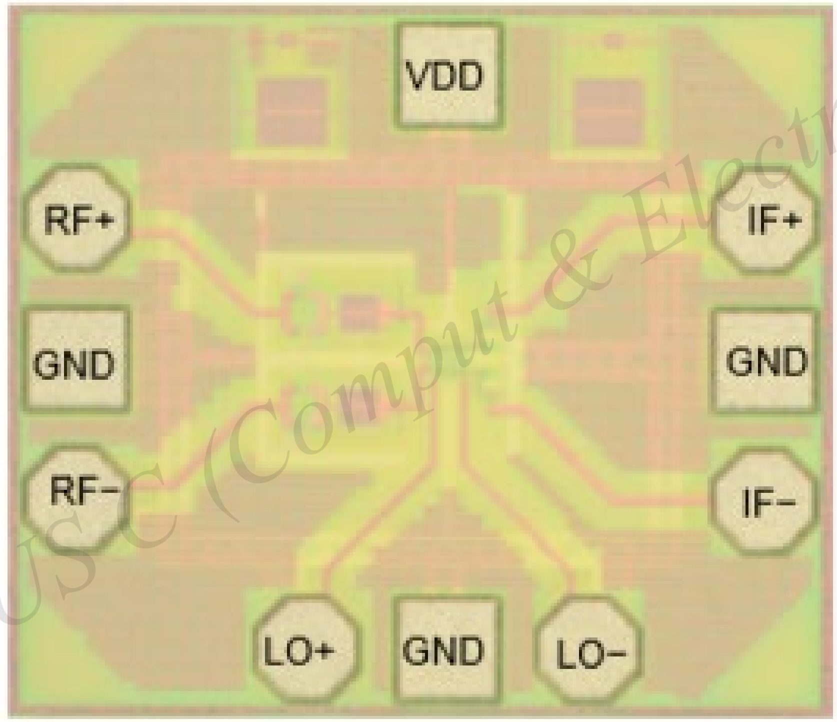

Fig. 7 Chip micrograph of the proposed folded mixer

Measurement results (1)

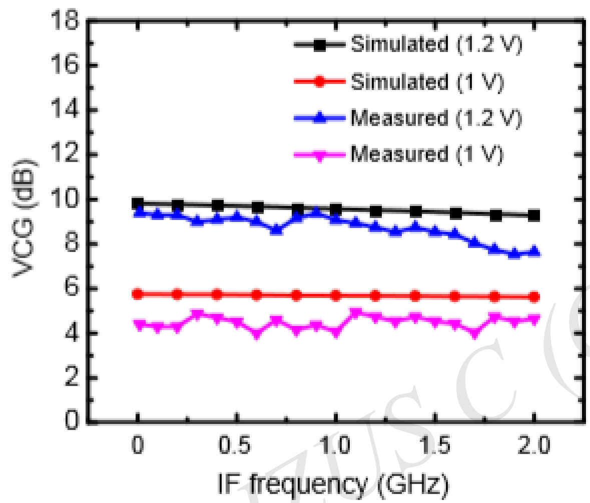

Fig. 8 Measured and simulated voltage conversion gains for VDD=1.2 V and 1 V

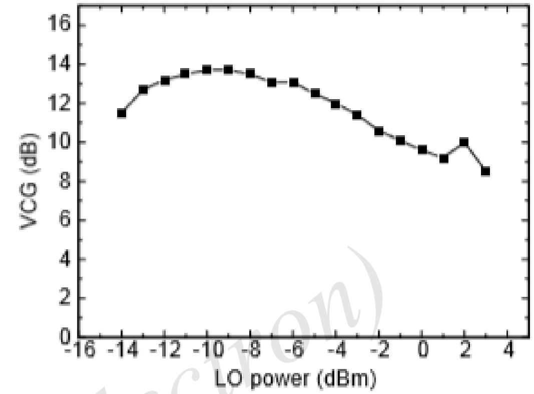

Fig. 9 Conversion gain variation with respect to LO power at an IF=10 MHz

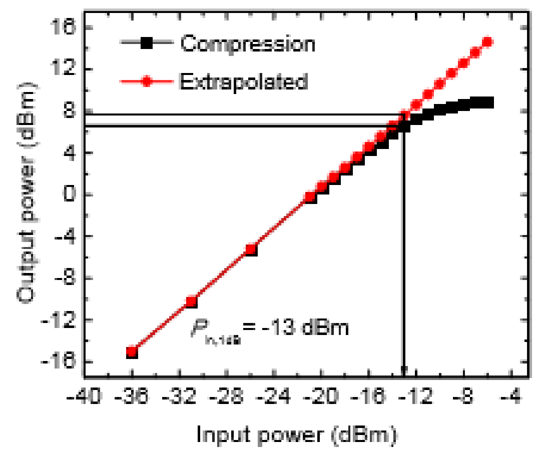

Fig. 10 $P_{in,1dB}$ at an IF of 10 MHz (f_{RF}=12.01 GHz, f_{LO}=12 GHz)

Measurement results (2)

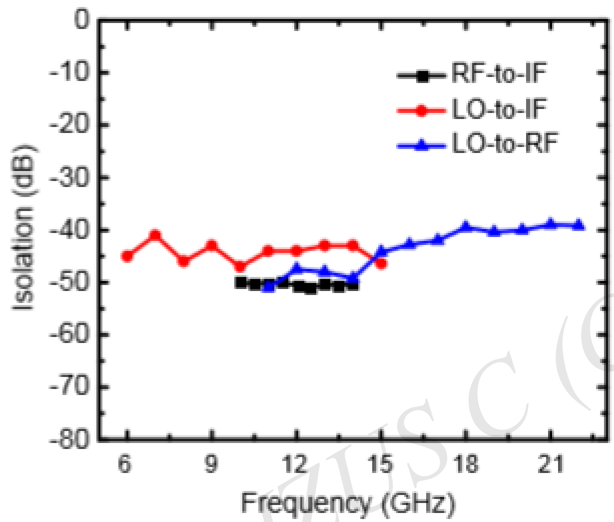

Fig. 11 Isolation characteristics of the proposed mixer (baluns with different frequency ranges were employed to measure isolation)

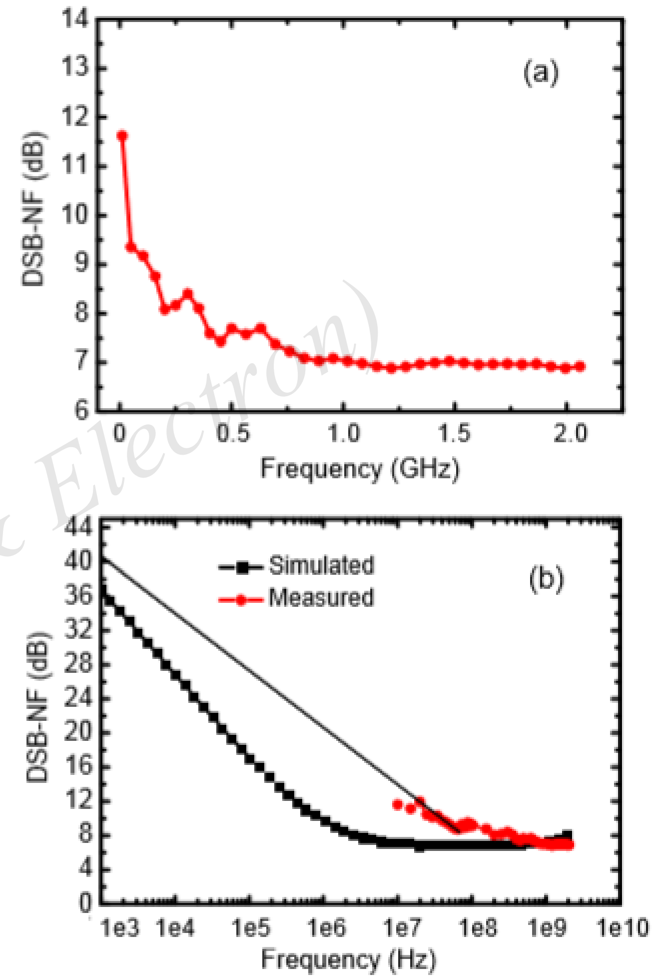

Fig. 13 Double sideband noise figure (DSB-NF): (a) linear IF axis; (b) simulated NF along with measured and extrapolated NF curves in a log-frequency axis

Performance comparison

Table B1 Performance summary with comparison to other works

Parameter	Value/Description						
	Hermann *et al.* (2005)	Klumperink *et al.* (2004)	Furuta *et al.* (2007)	Poobuapheun *et al.* (2007)*	Safarian *et al.* (2005)	Hampel *et al.* (2010)	This work
Process	0.13 μm CMOS	0.18 μm CMOS	0.13 μm CMOS	0.13 μm CMOS	0.18-μm CMOS	65 nm CMOS	65 nm CMOS
RF frequency (GHz)	2.1–3	0.3–4	0.85–2.1	0.7–2.5	3–8.72	1–10.5	10.25–13.75
CG_{max} (dB)	5.4	11	13.2	38	5	14.5	≈10
$P_{in,1dB}$ (dBm)	−9.2	NA	−6	−25.8	NA	−13.8	−13
IIP3 (dBm)	3.5	4.1	4.5	11	5	−4.2	−3.4**
NF_{min} (dB)	14.8 (SSB)	14 (SSB)	12.3 (DSB)	10 (DSB)	6.8	6.5 (DSB)	7 (DSB)
P_{DC} (mW)	1.6	6.6	8.25	24	10.4	14.4	6
VDD (V)	0.6	1	1.5	1.5	1.8	1.2	1.2
FOM*** (dB)	9.45	10.3	9.37	22.6	10	9.037	10.5
Area (mm^2)	NA	0.0048	NA	NA	1.624	0.011	0.017

* Including narrowband opamp; ** IIP3=$P_{-1\,dB}$+9.6 (Razavi, 1988); *** $\mathrm{FOM}=10\lg\left(\frac{10^{G/20}\cdot 10^{(\mathrm{IIP3}-10)/20}}{10^{NF/10}\,P(\mathrm{mW})}\right)$

Conclusions

- The folded mixer employing an ac-coupled self-biased current reuse topology for its transconductance stage shows good performance in terms of conversion gain, noise figure, and linearity.
- The proposed mixer achieves a competitive (slightly better) FOM compared to those proposed in the recent literature.