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A 37 GHz wide-band programmable divide-by-*N* frequency divider for millimeter-wave silicon-based phase-locked loop frequency synthesizers

Key words: Wide-band, Divide-by-*N*, Frequency divider, Dynamic current-mode logic (DCML), Pulse and swallow counter, CMOS

Corresponding author: Zhi-qun Li
E-mail: zhiqunli@seu.edu.cn

Motivation

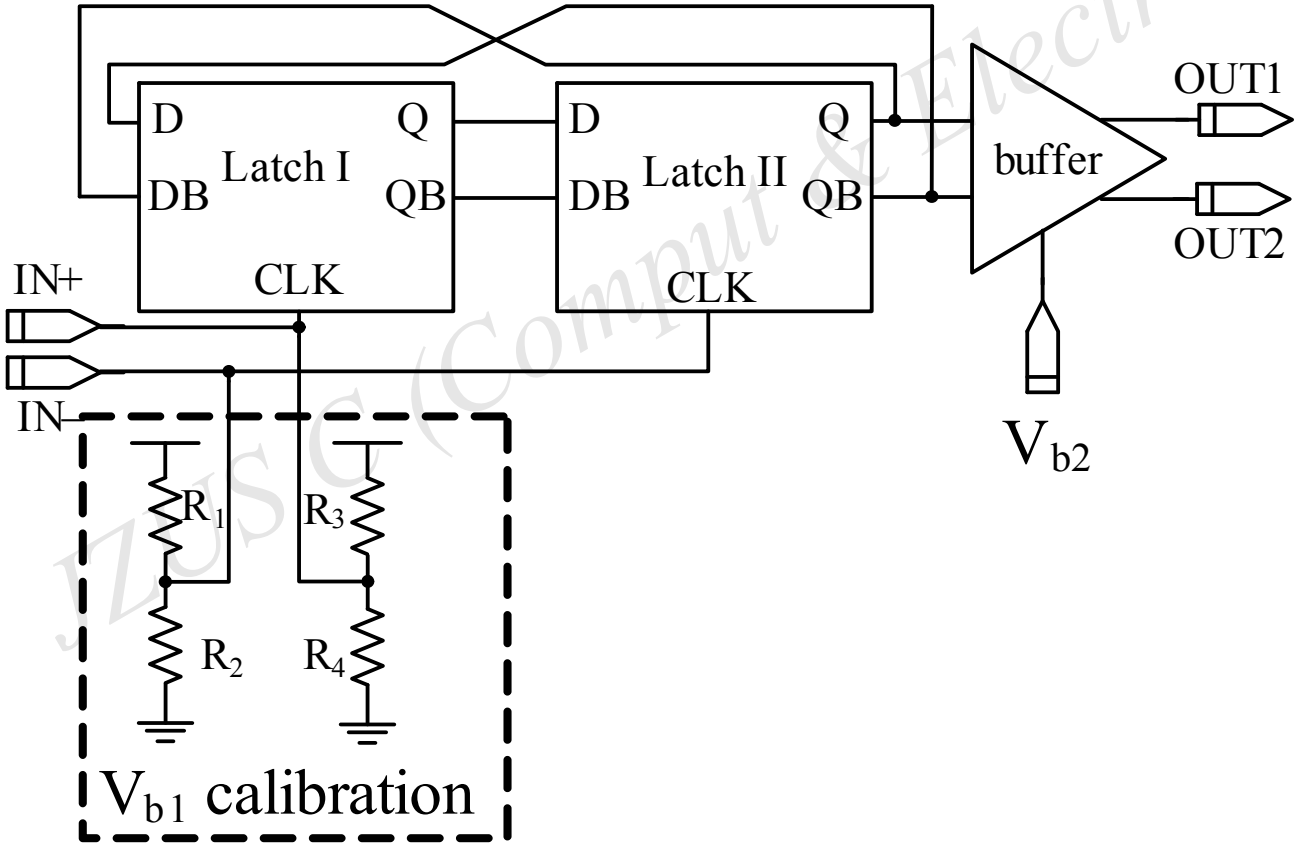
- Use a wide-band divide-by-2 divider and a pulse and swallow counter based programmable divider in millimeter-wave wide-band programmable divide-by-*N* FD , so as to achieve a consecutive programmable division ratio frequency modulation
- Disadvantages of existing methods:
  - Lower working frequency of normal DCML divide-by-2 and sensitivity
  - Fixed division ratios in mm-wave PLL

Features of our method

- Use an external bias voltage calibration block to modulate the first stage divide-by-2 divider to increase working frequency
- Optimization of divide-8/9 divider, using a signal locking DFF to reduce the gate delay
- Use a modified DCML integrated NOR gate to reduce gate delay

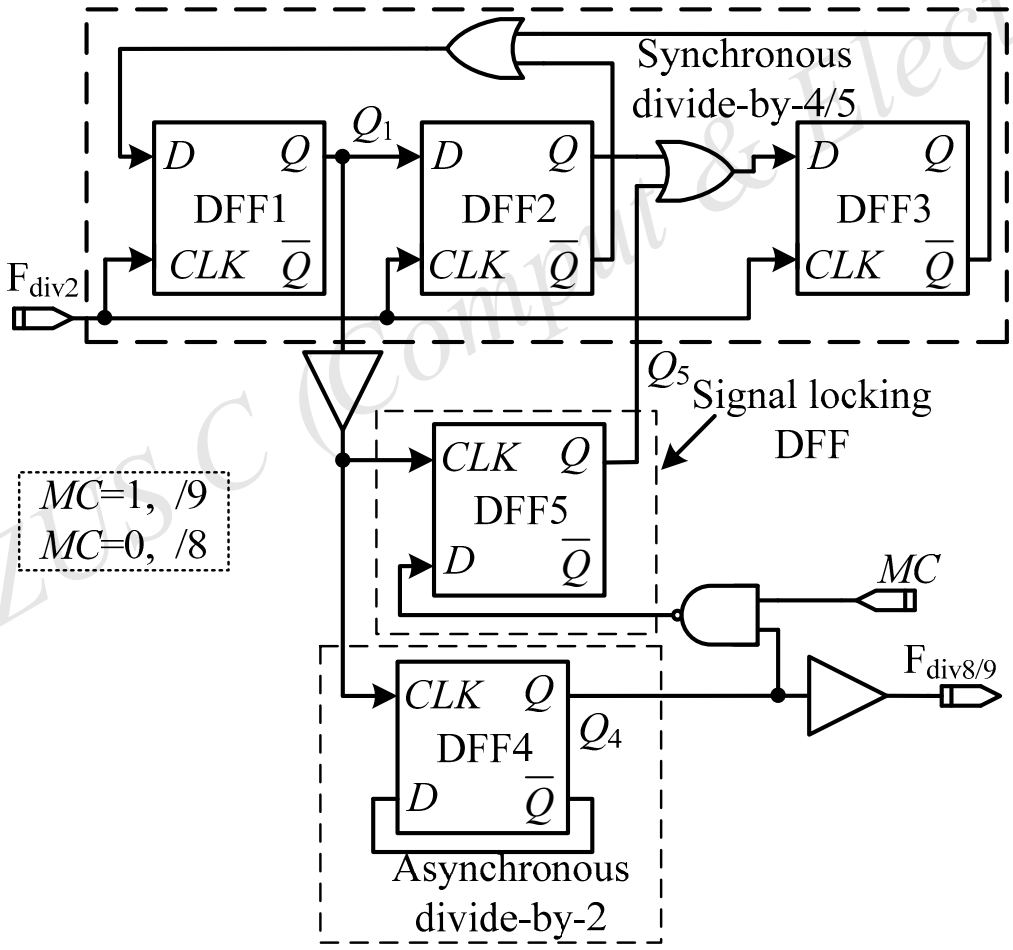
Framework of our method (I)

The calibration block which can modulate the dynamic load so that to increase working frequency:



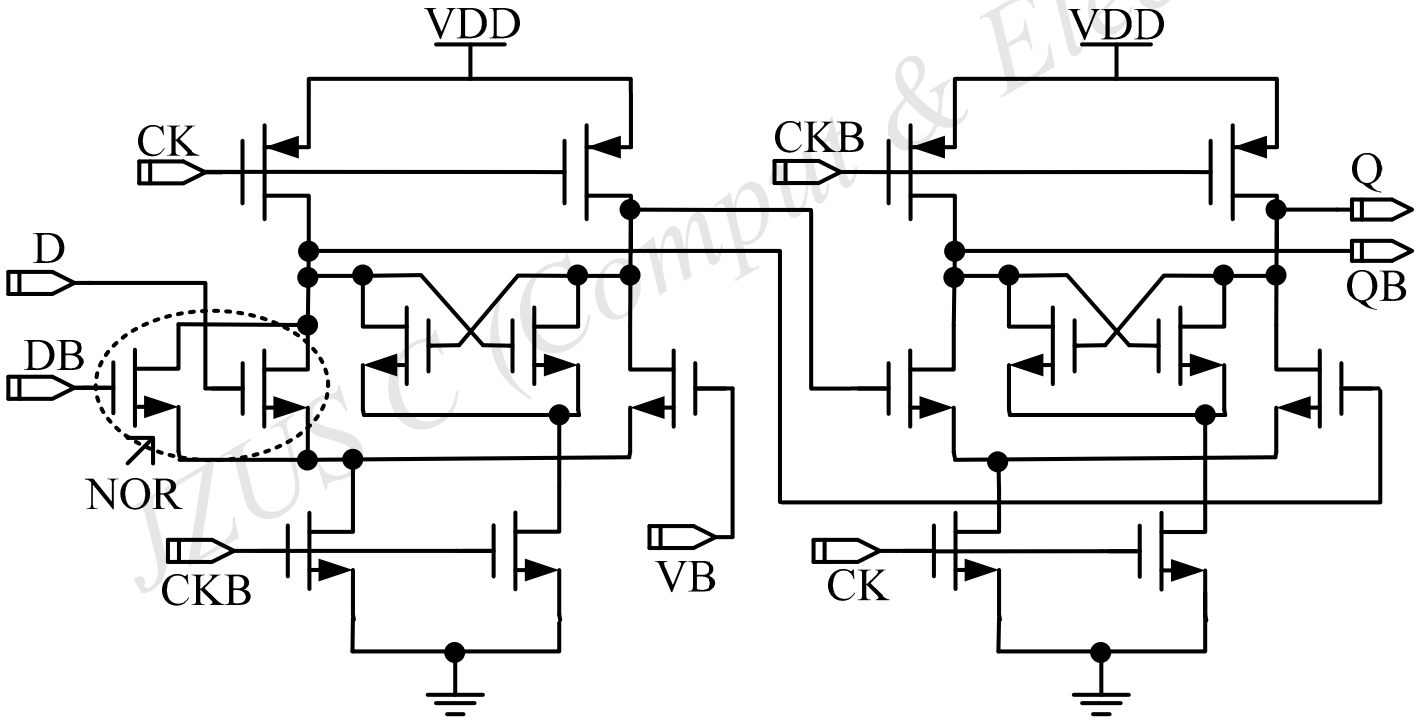
Framework of our method (II)

1. Optimization of divide-8/9 divider, using a signal locking DFF to reduce the gate delay



Framework of our method (II)

2. Modified DCML integrated NOR gate to reduce gate delay



Major results (I)

Comparison of the performance of similar structures of the first stage divider

Ref.	Wong *et al*., 2005	Wong *et al*., 2005	Usama *et al*., 2006*	Ting *et al*., 2012	**This work**
Supply (V)	1.2	1-1.35	1-1.2	1.2	**1.2**
Structure	Static CML	Dynamic CML	Static CML	Dynamic CML	**Dynamic CML**
PD (mW)	5.28	2.97	0.9	1.22	**0.96**
Maximum Freq. (GHz)	44	37	41	27	**40**
Division ratio	/2	/2	/2	/2	**/2**
Locking range (GHz)	20	20	37	20	**38**
Process (nm)	90	90	90	90	**90**

* Simulation results

Major results (II)

Comparison of the performance of similar structures of the whole 37 GHz wide-band programmable divide-by-N FD

Ref.	Ding and O, 2007	Pellerano *et al*., 2008	Chen *et al*., 2011	**This work**
Supply (V)	1.5	1.2	1.5	**1.2**
PD (mW)	9.075	-	-	**17.88**
Maximum Freq. (GHz)	21	41.6	41.2	**37**
Input power (dBm)	0	-	-	**0**
Division ratio	8	512-2032	512	**546-660**
Locking range (GHz)	14.78	2.5	1.5	**11**
Process (nm)	130	90	90	**90**