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A 31–45.5 GHz injection-locked frequency divider in 90-nm CMOS technology

Key words: CMOS, Injection-locked frequency divider (ILFD), Millimeter wave, Wide locking range, Monolithic microwave integrated circuit (MMIC)

Contact: Fa-en LIU
E-mail: liufaenseu@gmail.com
ORCID: http://orcid.org/0000-0003-1656-7936

Motivation

- An NMOS transistor with a tunable gate bias voltage, acting as an adjustable resistor, is connected to the differential output terminals for locking range extension.

- Disadvantages of existing methods:
  - A conventional ILFD usually suffers from a narrow locking range.
  - The utilization of varactors is not conductive to the operating frequency.
  - The match circuit used in the input port is not propitious to the wide locking range.

Design method (I)

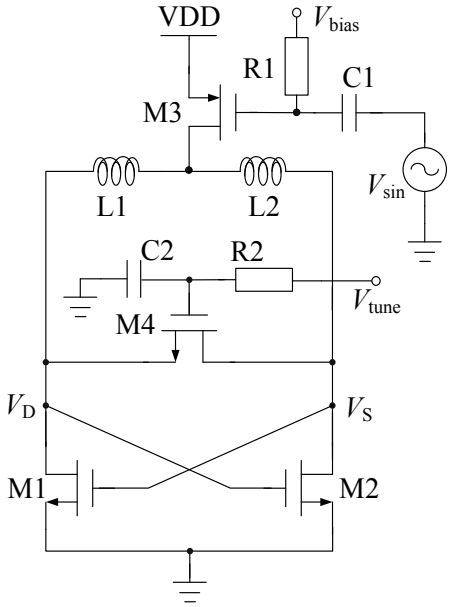


Fig. 1 Circuit schematic of the proposed ILFD

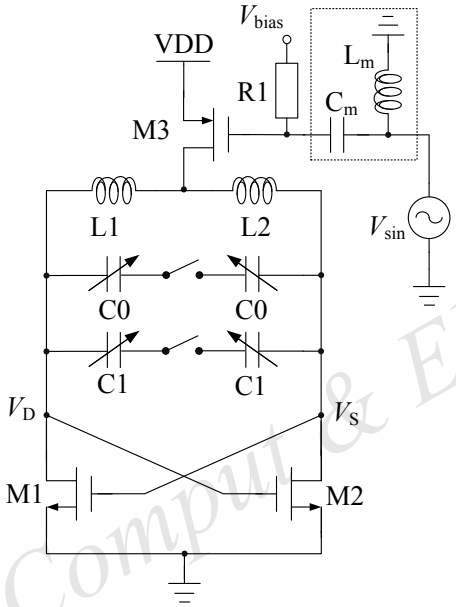


Fig. 2 Circuit schematic of the ILFD proposed in Katz *et al*.

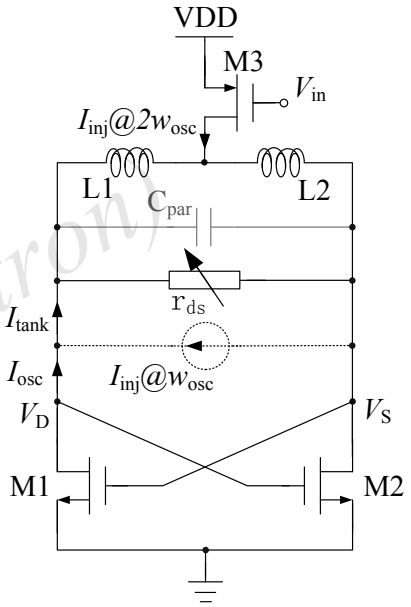


Fig. 3 Equivalent current model of the proposed ILFD

To extend the locking range, a modified ILFD is developed in this design (Fig. 1). Compared with the structure in Fig. 2:

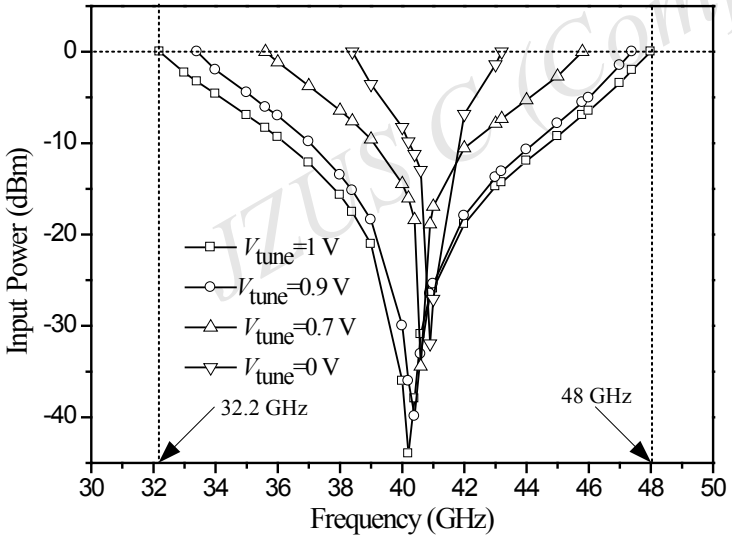
- Instead of the varactors, an NMOS transistor M4 with a tunable gate bias voltage V_{tune} is introduced to produce an adjustable resistance r_{ds} (Fig. 3) and extend the locking range.
- The matching network is not used in the proposed design for large injection power in a wide locking range.

Design method (II)

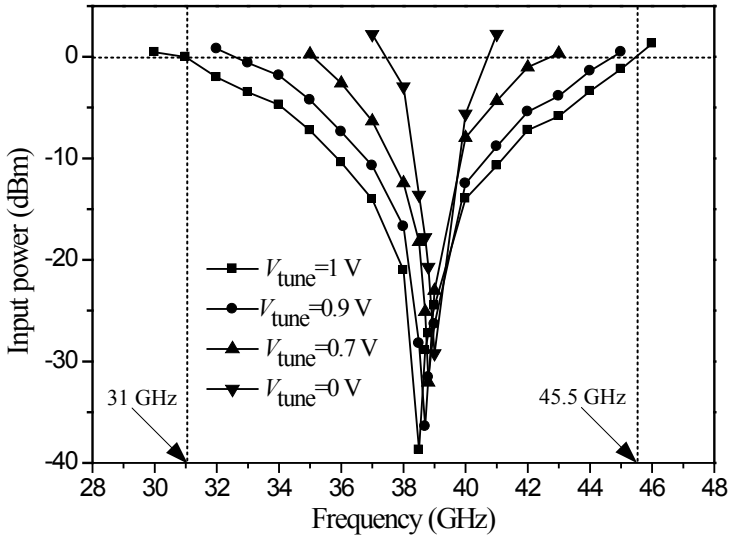
Due to the utilization of M4 with a tunable voltage V_{tune}, the locking range can be expressed as

$$\Delta\omega_{\max} = 2\omega_{\text{o}} \cdot \left(1 - \sqrt{1 - \frac{\eta \mu_{\text{n}} C_{\text{ox}} \left(\frac{W}{L} \right) (V_{\text{tune}} - V_{\text{S}} - V_{\text{TH}} - V_{\text{DS}}) \sqrt{L_{\text{ind}}}}{\sqrt{C_{\text{par}}} \sqrt{1 - \eta^2}}} \right).$$

Under different gate bias voltage V_{tune}, the simulated and measured injection sensitivity curves are shown as follows:



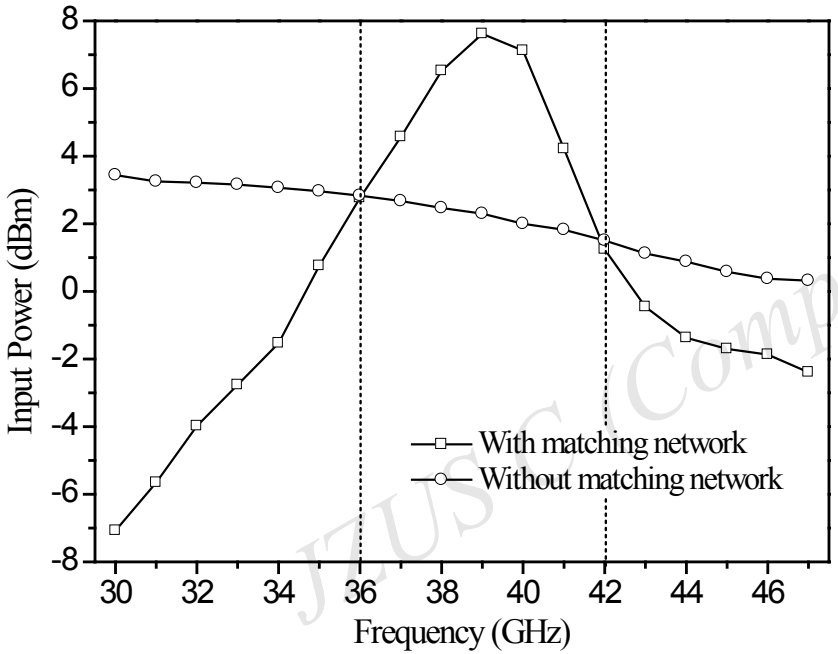
Simulated sensitivity curves



Measured sensitivity curves

Design method (III)

The simulated input power with or without the matching network is shown as follows:



Simulated input signals for the situations with or without matching network circuit

◆ Due to the matching network, a large input power is achieved within the matching frequency range. However, for a first-order LC matching network, a smaller matching bandwidth is achieved.

◆ When the frequency is out of the matching frequency range, the input power decreases rapidly and becomes lower than that without the matching network, which goes against the wide locking range.

As a result, the matching network is not used in the proposed design.

Conclusions

- A modified ILFD with a tunable locking range and tunable output power is proposed in this design.
- An NMOS transistor with a tunable voltage V_{tune} is used to produce adjustable resistance r_{ds}. By increasing the bias voltage V_{tune}, the frequency locking range of the ILFD is extended while the output power is reduced.
- For special applications, V_{tune} can be set to be an apt value for the divider to produce large enough output power and achieve a relatively wide locking range.