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Suppression of initial value changes in the dual transponder carrier ranging system for absolute distance measurement

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Abstract: The dual transponder carrier ranging system, an enhancement over the dual one-way ranging system, provides high-precision relative distance measurements without imposing stringent time synchronization requirements. However, a critical limitation to its use in absolute distance measurement is the initial value change phenomenon, which manifests as abrupt phase changes after every system restart. Through theoretical analysis, the root causes of this phenomenon are identified as a fractional output-to-input frequency ratio in the frequency synthesizer and a non-integer coherent turnaround ratio. To validate the theoretical analysis, simulations are conducted using Simulink, and experimental verification is performed on an S-band and C-band hardware platform. Both simulation and experimental results demonstrate that configuring both ratios as integers effectively suppresses these abrupt phase changes. These findings establish an integer-ratio design rule that is independent of specific frequency plans, providing a general design guideline for coherent transponder ranging systems intended for absolute distance measurement, as well as a reference for frequency planning in other absolute distance measurement systems of the same kind.

Key words: Dual transponder; Carrier phase ranging; Absolute distance measurement; Initial value change

1 Introduction

The fundamental principle of radio ranging involves measuring the time delay of a radio signal propagating from the transmitter to the receiver and then multiplying this delay by the propagation speed of the radio wave to obtain the distance. Common radio ranging techniques include side-tone ranging, pseudorandom code ranging, and carrier phase ranging. Among these, side-tone ranging employs multiple modulation tones for distance estimation (Miesen et al., 2012; Liu et al., 2017), typically achieving accuracy at the meter or decimeter level (Liu et al., 2017). Pseudorandom code ranging generally attains accuracy at the decimeter to centimeter level (Jin et al., 2017, 2020), which generally falls short of the requirements for high-precision ranging applications. In contrast, microwave carrier phase ranging uses phase information of the carrier signal for distance measurement, achieving significantly higher precision compared to both side-tone and pseudorandom code methods (Xiang et al., 2019; Wang et al., 2021; Müller et al., 2022). This technique has been widely adopted in various fields, such as deep space ranging (Berner and Bryant, 2002), telemetry (Kreng et al., 2007), and geodesy (Pollinger et al., 2012).

A representative microwave carrier phase ranging technique is the dual one-way ranging (DOWR) system, which suppresses oscillator noise effects by combining one-way range measurements from two microwave units (Kim and Tapley, 2003). A notable implementation is the K-band and Ka-band ranging system used in the gravity recovery and climate experiment (GRACE) mission, commonly referred to as the KBR system (Bertiger et al., 2002, 2003). This system uses K-band and Ka-band carrier signals for relative distance measurement and achieves ranging accuracy on the order of 10 μm (Kim and Tapley, 2005).

Despite its high measurement accuracy, the performance of the DOWR system critically depends on precise time

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synchronization between the master and slave units. Significant clock offsets can severely degrade ranging accuracy (Zhao MC et al., 2013). To alleviate the stringent time synchronization requirements in the DOWR system, Kim and Tapley (2005) proposed an optimized frequency configuration scheme at the expense of increased hardware complexity and cost. Furthermore, the DOWR system is incapable of delivering real-time distance measurements. Data collected at both units must be transferred to a central processing unit for joint and computationally intensive post-processing before the final range information can be obtained.

Building upon the foundational framework of the DOWR system and the unified S-band (USB) system (Hood, 1965), Zhao XY et al. (2009) proposed a dual transponder carrier ranging system to overcome inherent limitations such as stringent time synchronization requirements and the lack of real-time data processing capabilities. In contrast to the DOWR system, the proposed system maintains the advantage of suppressing oscillator noise effects, while eliminating the requirements for time synchronization and computationally intensive post-processing to derive distance measurements. The key distinction between the two systems lies in their operational principles: whereas the DOWR system requires the master and slave units to simultaneously and independently transmit and receive signals (Kim and Tapley, 2003), the dual transponder system operates by having the slave unit coherently retransmit a regenerated version of the signal received from the master unit (Zhao XY et al., 2009).

The dual transponder carrier ranging system was originally designed for relative distance measurement (i.e., Doppler velocity measurement or range variation measurement), and has been proven to offer exceptionally high precision (Zhao MC et al., 2013). However, when its application scope is extended from relative distance measurement to absolute distance measurement, an initial value change phenomenon emerges. This issue severely constrains the broader application of the dual transponder carrier ranging system. This paper aims to analyze the underlying causes of the initial value change phenomenon and propose corresponding solutions, thereby enabling stable application of the dual transponder carrier ranging system to absolute distance measurement.

2 Measurement principle and initial value change phenomenon in the dual transponder carrier ranging system

The dual transponder carrier ranging system measures the distance by extracting the carrier phase difference. Fig. 1 illustrates the phase transfer mechanism within the system, under the assumption of equal signal propagation time for both forward (master to slave) and return (slave to master) paths.

In this system, the phase difference of a single-frequency carrier at the nominal time t can be expressed as

$$\Theta(t) = \varphi_{\mathrm{ref}}(t) - \varphi_{\mathrm{m}}^{\mathrm{r}}(t) + E, \tag{1}$$

where $\varphi_{\mathrm{ref}}(t)$ denotes the reference carrier phase at the master unit, $\varphi_{\mathrm{m}}^{\mathrm{r}}(t)$ represents the received carrier phase at the master

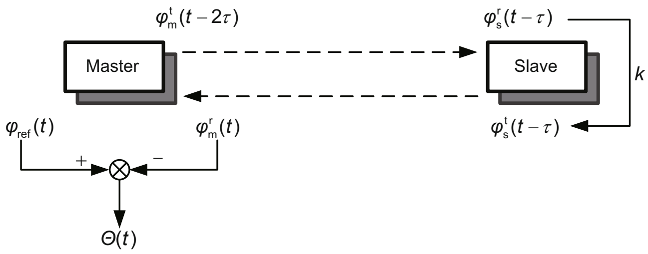

Fig. 1 Phase transfer in the dual transponder carrier ranging system

unit, and E encompasses integer ambiguity and measurement noise.

The received carrier phase can be expressed in terms of the transmitted carrier phase. Therefore, the received carrier phases at the master and slave units can be respectively given by

$$\begin{cases} \varphi_{\mathrm{m}}^{\mathrm{r}}(t) = \varphi_{\mathrm{s}}^{\mathrm{t}}(t-\tau), \\ \varphi_{\mathrm{s}}^{\mathrm{r}}(t-\tau) = \varphi_{\mathrm{m}}^{\mathrm{t}}(t-2\tau), \end{cases} \tag{2}$$

where τ denotes the time of flight of the carrier signal from the master to the slave unit, $\varphi_{\mathrm{s}}^{\mathrm{t}}$ and $\varphi_{\mathrm{m}}^{\mathrm{t}}$ denote the transmitted carrier phase at the slave and master units respectively, and $\varphi_{\mathrm{s}}^{\mathrm{r}}$ denotes the received carrier phase at the slave unit.

Furthermore, the signal transmitted by the slave unit is a coherent turnaround version of its received signal, maintaining phase synchronization during retransmission. Let k be the coherent turnaround ratio, defined as the ratio between the phase of the slave's transmitted signal and the phase of its received signal. Similarly, the reference phase at the master unit is synchronized with its transmitted signal phase, sharing the same proportionality constant k (Zhao XY et al., 2009):

$$\begin{cases} \varphi_{\mathrm{s}}^{\mathrm{t}}(t-\tau) = k\varphi_{\mathrm{s}}^{\mathrm{r}}(t-\tau), \\ \varphi_{\mathrm{ref}}(t) = k\varphi_{\mathrm{m}}^{\mathrm{t}}(t). \end{cases} \tag{3}$$

Substituting Eqs. (2) and (3) into Eq. (1) yields the expression:

$$\begin{aligned} \Theta(t) &= k\varphi_{\mathrm{m}}^{\mathrm{t}}(t) - k\varphi_{\mathrm{m}}^{\mathrm{t}}(t-2\tau) + E \\ &= 4k\pi f_{\mathrm{m}}\tau + E \\ &= 4\pi f_{\mathrm{s}}\tau + E, \end{aligned} \tag{4}$$

where f_{m} represents the carrier frequency of the signal transmitted by the master unit, f_{s} denotes the carrier frequency of the signal transmitted by the slave unit, and $f_{\mathrm{s}} = kf_{\mathrm{m}}$.

Multiplying the phase difference measurement $\Theta(t)$ by the equivalent wavelength λ gives the distance $R(t)$ between the master and slave units:

$$R(t) \equiv \lambda\Theta(t), \tag{5}$$

where $\lambda = c/(4k\pi f_{\mathrm{m}})$ with c denoting the light speed.

When the dual transponder carrier ranging system is applied to absolute distance measurement, the measured value should remain constant provided that the distance between the master and slave units is kept unchanged and that both the system and its operating environment remain unchanged. Based on this principle, we conduct an experiment in which the system is used for absolute distance measurement.

It is important to note that in practical implementations of a radio frequency (RF) system, the selection of forward and return link frequencies is often dictated by external constraints such as spectrum allocation policies of the International Telecommunication Union (ITU), mission-specific frequency plans, and established engineering conventions. A prominent example is the 240/221 turnaround ratio adopted by the USB system since the Apollo program, which is formally specified as a recommended turnaround ratio in the Consultative Committee for Space Data Systems (CCSDS) radio frequency and modulation systems standards (e.g., CCSDS 401.0-B-32). In accordance with this convention, the dual transponder carrier ranging system adopts the S-band turnaround ratio of 240/221 recommended by the CCSDS. In addition, the frequency reference of the system is an oven-controlled crystal oscillator (OCXO). The detailed system parameters are listed in Table 1.

Table 1 S-band parameter configuration

Parameter	Value
Frequency of the OCXO (MHz)	40.0
System forward frequency (MHz)	2165.8
System return frequency (MHz)	2352.0
Coherent turnaround ratio	240/221

With the system and its operating environment kept unchanged, the system is reset or restarted multiple times. The measured distance values are presented in Fig. 2, where it is clearly observable that they undergo multiple discrete changes. After repeated experiments, the phenomenon can be summarized as follows: even without any modifications to the software or hardware platform, the measured value may exhibit a discrete change following a software reset or a hardware power cycle. The initial value change phenomenon makes it difficult to apply the dual transponder carrier ranging system to absolute distance measurement, limiting its application to relative distance measurement only and significantly hindering its broader adoption. Therefore, it is necessary to analyze the underlying mechanism of this phenomenon and to develop an effective mitigation strategy.

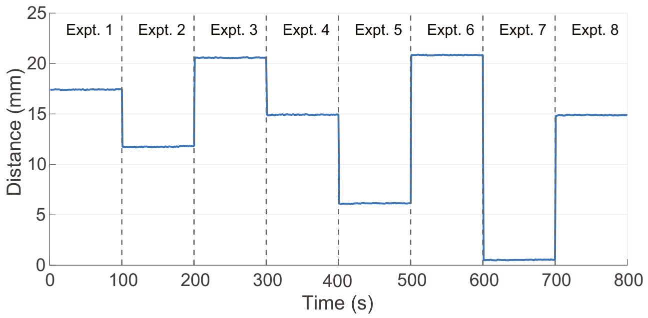

Fig. 2 Initial value changes (Expt.: experiment)

3 Theoretical analysis of the source and resolution of the initial value changes

According to Eq. (5), the distance measurement in the dual transponder carrier ranging system is derived from the phase difference between the master and slave units. An abrupt change in the measured distance after system restart implies a corresponding discontinuity in this phase difference. Therefore, analysis of the initial value change phenomenon requires a detailed examination of the phase measurement transmission process between the master and slave units to pinpoint the specific stage at which such an abrupt phase change occurs.

As shown in Fig. 3, the carrier signal processing in both master and slave units of the dual transponder carrier ranging system can be divided into analog and digital sections. The analog processing stage includes frequency synthesis, mixing, filtering, and amplification. The digital processing stage comprises analog-to-digital (A/D) conversion, digital mixing, digital filtering, digital phase locking, and digital-to-analog (D/A) conversion. Additionally, the slave unit incorporates a coherent turnaround module, which receives the signal from the master unit and retransmits it in a phase-coherent manner. It is therefore necessary to examine the above stages to analyze the root causes of the initial value change phenomenon and to propose effective solutions.

3.1 Mixing

3.1.1 Analog mixer

In the analog processing section, the mixing function is implemented using mixers. Based on power supply requirements, mixers can be classified into two categories: passive mixers and active mixers. Passive mixers typically employ Schottky diodes (Araki and Hirayama, 1971) or field-effect transistors operating in the linear region as the mixing elements, whereas active mixers use bipolar junction transistors and field-effect transistors operating in the saturation region as their core components, the most representative of which is the Gilbert cell mixer structure (Gilbert, 1968; Sandalci and Kiaei, 1998). The fundamental principle of a mixer is the use of nonlinear devices (such as the exponential current–voltage characteristic of a diode or the square-law characteristic of a transistor) or time-varying switches to shift signals in the frequency domain. Mathematically, this operation corresponds to the multiplication of two signals in the time domain. The transmission delay introduced by the mixer is an intrinsic phase delay determined jointly by the physical delay of the internal diodes or transistors and the impedance matching network. Under ideal conditions, this delay is constant. In practical applications, the delay may vary with factors such as changes in the local oscillator (LO) signal power or ambient temperature; however, such variations are continuous and do not cause abrupt changes in the phase measurement after a system restart. Therefore, the phase delay introduced by the mixer does not contribute to the initial value change phenomenon.

3.1.2 Digital mixer

The digital mixer is implemented within the field-programmable gate array (FPGA). The local oscillator signal is generated by the Coordinate Rotation Digital Computer (CORDIC) algorithm, and the mixing process is performed by a digital multiplier. The entire process operates in a pipelined manner, and the input-to-output delay introduced by this process corresponds to a fixed number of pipeline clock cycles;

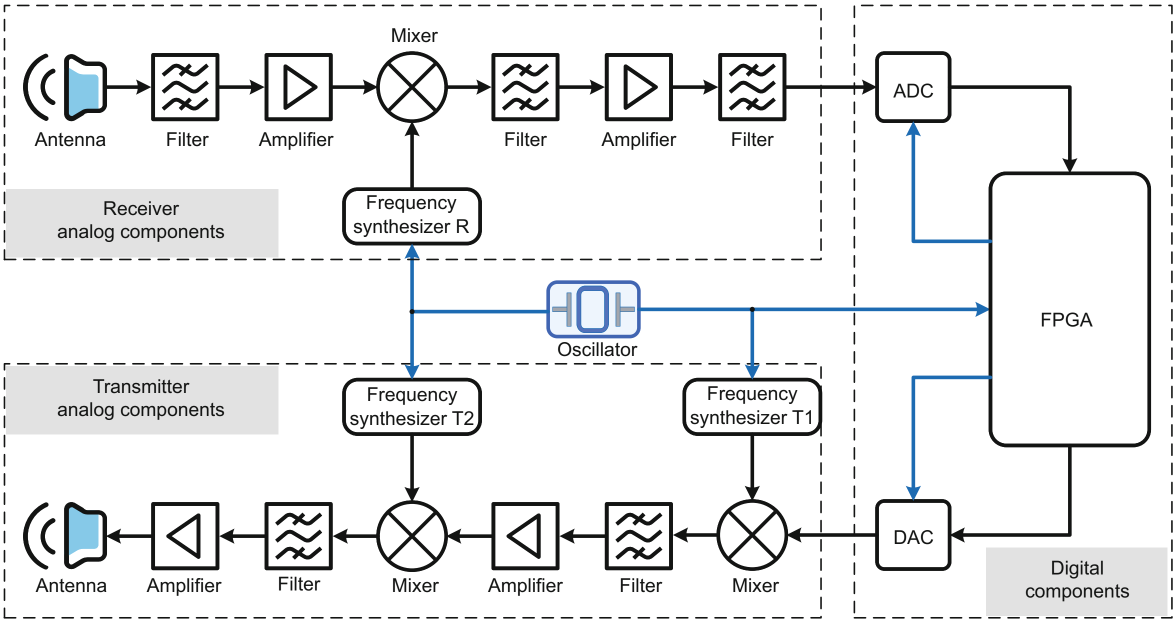

Fig. 3 Hardware architecture of the dual transponder carrier ranging system

therefore, the resulting phase difference is determined solely by the frequency of the driving clock. Since the module driving clock of the FPGA is traceable back to an external crystal oscillator, the phase difference introduced by the digital mixer may also be affected by the frequency drift of the crystal oscillator. However, this influence is slight and continuous, and does not cause abrupt phase changes after a system restart. Consequently, the phase difference introduced by the digital mixer does not contribute to the initial value change phenomenon.

3.2 Filtering

3.2.1 Analog filter

Analog filtering is performed by RF filters. Commonly used filters include surface acoustic wave (SAW) filters and cavity filters. The core function of these filters is to selectively transmit or suppress signals within a specific frequency range by means of specific structural designs. Typically, the frequency response of a filter can be expressed as the product of its magnitude–frequency response $|H(\mathrm{j}\omega)|$ and its phase–frequency response $\varPhi(\omega)$:

$$H(\mathrm{j}\omega)=|H(\mathrm{j}\omega)|\mathrm{e}^{\mathrm{j}\varPhi(\omega)}, \tag{6}$$

where $|H(\mathrm{j}\omega)|$ determines the filter's ability to attenuate or amplify signal energy at different frequencies, which serves as the basis for achieving frequency selectivity (e.g., low-pass, high-pass, band-pass, and band-stop), $\varPhi(\omega)$ determines the phase delay accumulated by the signal as it traverses the filter network, and ω is the analog angular frequency.

For a single-frequency carrier input signal with an angular frequency of ω_0, the phase–frequency response introduced by the filter is $\varPhi(\omega_0)$. In practice, factors such as crystal oscillator phase noise and aging can cause a frequency offset $\delta\omega_0$ in the input signal, which in turn changes the phase–frequency response introduced by the filter from $\varPhi(\omega_0)$ to $\varPhi(\omega_0+\delta\omega_0)$. Moreover, variations in operating temperature can lead to changes in the material properties and structure of the filter, resulting in a temperature drift of its frequency response (Keats et al., 2003; Djerafi et al., 2012; Ruby et al., 2021); this also causes a drift in the phase difference introduced by the filter. However, both the frequency offset and temperature drift are continuous in nature and do not cause abrupt changes in the phase difference after a system restart. Therefore, the transmission delay introduced by the filter does not contribute to the initial value change phenomenon.

3.2.2 Digital filter

A digital filter is a mathematical algorithm system that operates in the discrete-time domain. In essence, it performs high-speed multiply–accumulate operations on sampled and quantized digital sequences using a microprocessor, a digital signal processor (DSP), or an FPGA. The transfer function $H(z)$ of such a system can be expressed as

$$H(z)=\frac{Y(z)}{X(z)}=\frac{\sum_{k=0}^{L_{\mathrm{num}}}b_k z^{-k}}{1+\sum_{k=1}^{L_{\mathrm{den}}}a_k z^{-k}}, \tag{7}$$

where $X(z)$ and $Y(z)$ denote the Z-transforms of the input and output digital signals, respectively, z is the complex variable in the Z-transform, b_k and a_k are the feedforward and feedback coefficients of the digital filter, and L_{num} and L_{den} are the feedforward and feedback orders of the filter, respectively. The frequency response of this discrete-time system can be written as

$$H(\mathrm{e}^{\mathrm{j}\varOmega})=|H(\mathrm{e}^{\mathrm{j}\varOmega})|\mathrm{e}^{\mathrm{j}\phi(\varOmega)}, \tag{8}$$

where $|H(\mathrm{e}^{\mathrm{j}\varOmega})|$ denotes the magnitude–frequency response of the digital filter, $\phi(\varOmega)$ denotes its phase–frequency response, and $\varOmega$ is the normalized digital angular frequency, defined as the product of the analog angular frequency ω and the sampling period T_{s}, i.e.,

$$\varOmega=\omega T_{\mathrm{s}}=2\pi\frac{f}{f_{\mathrm{sam}}}, \tag{9}$$

with f being the analog signal frequency and $f_{\rm sam}$ the sampling frequency.

For a digital filter that has been completely designed and fixed (i.e., its order, coefficients, and internal topology are no longer subject to change), its phase–frequency response $\phi(\varOmega)$ is a fully determined mathematical function. Suppose that the single-frequency carrier signal passing through the digital filter is expressed as

$$x(n_{\rm s}) = A\cos(\varOmega_{\rm c} n_{\rm s} + \phi_0), \tag{10}$$

where A is the amplitude of the input signal, $n_{\rm s}$ is an integer denoting the index of a sample point in the discrete sequence $x(n_{\rm s})$, $\varOmega_{\rm c}$ is the normalized digital angular frequency of the input signal, given by $\varOmega_{\rm c} = 2\pi f_{\rm c}/f_{\rm sam}$, and ϕ_0 is the initial phase of the input signal. In this case, the phase–frequency response of the digital filter corresponding to this carrier frequency is $\phi(\varOmega_{\rm c})$. Since the structure of the digital filter is fixed, the only factor that can cause a change in the phase–frequency response is a variation in the normalized digital angular frequency $\varOmega_{\rm c}$ of the carrier signal. When the actual carrier frequency $f_{\rm c}$ deviates from its nominal value due to temperature effects or the aging of the crystal oscillator, or when the clock signal driving the analog-to-digital converter (ADC) exhibits phase noise or jitter, the actual sampling interval $T_{\rm s}$ may undergo slight fluctuations. This results in a small offset $\Delta\varOmega_{\rm c}$ in $\varOmega_{\rm c}$, thus causing the phase–frequency response of the digital filter to change from $\phi(\varOmega_{\rm c})$ to $\phi(\varOmega_{\rm c}+\Delta\varOmega_{\rm c})$. However, the frequency drift of the crystal oscillator is slow, and the carrier frequency normally lies within the flat passband of the digital filter; therefore, the variation of $\phi(\varOmega_{\rm c})$ is continuous and minute, and does not cause abrupt phase changes after a system restart. Consequently, the phase difference introduced by the digital filter does not contribute to the initial value change phenomenon.

3.3 Amplification

In RF circuits, signal amplification is performed by power amplifiers (PAs) and low-noise amplifiers (LNAs). PA is typically located at the final stage of the transmitter chain and is responsible for boosting the transmit power. LNA, on the other hand, is placed at the front end of the receiver chain, where it amplifies weak signals while minimizing the introduction of additional noise. The core function of an amplifier is to increase the amplitude of the input signal by exploiting the gain characteristics of active devices, such as transistors.

3.3.1 Power amplifier

PA is one of the most significant nonlinear devices in wireless communication systems. In practical applications, PAs are typically operated near their saturation point to maximize efficiency. Since the active devices that constitute a PA inherently exhibit nonlinear characteristics, PAs inevitably display various types of nonlinear behavior to varying degrees. Such nonlinear behavior commonly manifests as amplitude and phase distortions caused by the gain nonlinearity of the amplifier, i.e., AM–AM distortion and AM–PM distortion (Quindroit et al., 2024). AM is short for amplitude modulation and PM is short for phase modulation. A classic behavioral model for describing the nonlinear characteristics of PAs is the Saleh model proposed by Saleh (1981). The Saleh model is a simple static nonlinear model, and its description of the AM–PM characteristics of a PA is given by

$$\phi[r(t)] = \frac{\alpha_\phi r^2(t)}{1+\beta_\phi r^2(t)}, \tag{11}$$

where $\phi[r(t)]$ denotes the phase shift introduced by the PA, $r(t)$ denotes the amplitude of the input signal to the PA, and α_ϕ and β_ϕ are empirically fitted parameters. From Eq. (11), it can be seen that the phase shift $\phi[r(t)]$ introduced by the PA is a continuous function of the input signal amplitude $r(t)$. When the input signal amplitude varies, the phase shift introduced by the PA also changes accordingly. In the experiment described in Section 2, the amplitude of the input signal to the PA remains stable and therefore does not introduce significant phase shift variations, let alone cause abrupt phase changes after a system restart.

3.3.2 Low-noise amplifier

Like PA, LNA is also an active device with nonlinear characteristics. However, since LNAs typically process weak signals, they normally operate in the linear or quasi-linear region and therefore exhibit relatively weak nonlinear behaviors. Furthermore, when the dual transponder carrier ranging system performs stationary measurements, the amplitude of the input signal to the LNA remains stable. Under such conditions, the phase shift introduced by the LNA is also relatively stable and does not cause abrupt phase changes after a system restart.

3.4 A/D conversion and D/A conversion

3.4.1 A/D conversion

The A/D conversion function is typically implemented by an ADC, which is an electronic device that converts a continuous-time and continuous-amplitude analog signal into a discrete-time and discrete-amplitude digital signal. The total latency of an ADC, denoted as $t_{\rm LAT}$, refers to the time interval between the instant at which the analog input is sampled and the instant at which the corresponding digital signal appears at the output. In general, the total latency of an ADC can be expressed as follows:

$$t_{\rm LAT} = t_{\rm CT} + t_{\rm OD} - t_{\rm AD}, \tag{12}$$

where $t_{\rm CT}$ is the conversion latency, which reflects the time required from the analog signal input to the completion of conversion and encoding; $t_{\rm OD}$ is the output latency, which represents the overall analog delay of the ADC from the sampling clock edge to the appearance of the digital signal at the output, and $t_{\rm AD}$ is the aperture latency.

The conversion latency $t_{\rm CT}$ of an ADC is typically measured in number of sampling clock cycles. This value is clearly specified in the device datasheet and is a fixed constant. Therefore, the conversion latency depends solely on the sampling clock frequency. Since the sampling clock ultimately originates from an external crystal oscillator, frequency drift of the crystal oscillator may cause a drift in the sampling clock frequency, which in turn leads to a variation in the conversion latency t_{CT} and ultimately results in a drift of the phase difference experienced by the signal passing through the ADC. However, this drift is continuous and does not cause abrupt phase changes after a system restart. The output latency t_{OD} is influenced by factors such as process conditions, the supply voltage of the digital pins, and the load capacitance. This parameter is normally fixed and does not cause jumps in the total ADC latency. The aperture latency t_{AD} is also typically a fixed value and is explicitly specified in the datasheet. Due to internal noise within the ADC, the aperture latency t_{AD} may exhibit minute random jitter; this jitter is referred to as aperture jitter. However, this jitter primarily affects the signal-to-noise ratio of the sampled signal and does not exert a significant influence on the signal propagation delay introduced by the ADC. Therefore, the propagation delay introduced by the ADC does not cause abrupt phase changes after a system restart.

3.4.2 D/A conversion

A digital-to-analog converter (DAC) is the electronic component that converts a discrete-time and discrete-amplitude digital signal into a continuous-time and continuous-amplitude analog signal. The core function of a DAC is to realize the conversion from digital signals to analog signals through processes such as interpolation and filtering. The phase difference introduced by the DAC also stems from the processing delays within its internal circuitry, including the inherent delay characteristics of the digital input interface, interpolation filter, and output buffer circuit. These delays are typically either fixed or slowly varying and do not cause abrupt phase changes after a system restart.

3.5 Frequency synthesizer

In the dual transponder carrier ranging system, an integer-N frequency synthesizer chip is employed to generate the carrier signals. The core component of a frequency synthesizer is a phase-locked loop (PLL) module containing a frequency divider, and its functional block diagram is shown in Fig. 4.

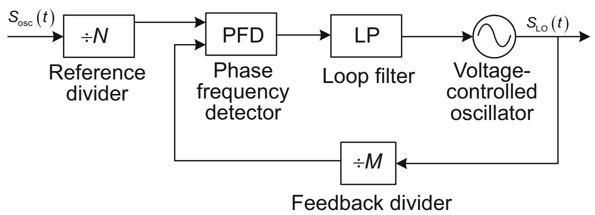

Fig. 4 Functional block diagram of the integer-N frequency synthesizer

The input to the frequency synthesizer is a signal provided by a crystal oscillator, expressed as

$$S_{\mathrm{osc}}(t) = \sin(2\pi f_{\mathrm{osc}} t + \theta_{\mathrm{osc}}), \tag{13}$$

where f_{osc} denotes the frequency of the crystal oscillator's output signal, and θ_{osc} represents its initial phase. The output of the frequency synthesizer is given by

$$S_{\mathrm{LO}}(t) = \sin(2\pi f_{\mathrm{LO}} t + \theta_{\mathrm{LO}}), \tag{14}$$

where f_{LO} denotes the frequency of the frequency synthesizer's output signal, and θ_{LO} represents its initial phase. Theoretically, the input–output relationship of the frequency synthesizer can be described as

$$\begin{aligned} S_{\mathrm{LO}}(t) &= \sin\left[\frac{f_{\mathrm{LO}}}{f_{\mathrm{osc}}}(2\pi f_{\mathrm{osc}} t + \theta_{\mathrm{osc}})\right] \\ &= \sin\left[\frac{M}{N}(2\pi f_{\mathrm{osc}} t + \theta_{\mathrm{osc}})\right], \end{aligned} \tag{15}$$

where

$$\frac{M}{N} = \frac{f_{\mathrm{LO}}}{f_{\mathrm{osc}}}, \tag{16}$$

M and N are positive integers, and M/N is an irreducible fraction. Although both M and N are integers, the ratio M/N is not necessarily an integer.

However, in practice, due to the periodic nature of the input signal, as well as the uncertain initial conditions and lock time of the PLL, the signal actually tracked by the PLL is not the ideal waveform $\sin(2\pi f_{\mathrm{osc}} t + \theta_{\mathrm{osc}})$ but rather $\sin(2\pi f_{\mathrm{osc}} t + 2n\pi + \theta_{\mathrm{osc}})$, where n is an integer. Therefore, the actual output signal becomes

$$S_{\mathrm{LO}}(t) = \sin\left[\frac{M}{N}(2\pi f_{\mathrm{osc}} t + 2n\pi + \theta_{\mathrm{osc}})\right], \tag{17}$$

with the initial phase expressed as

$$\theta_{\mathrm{LO}} = \frac{M}{N}(2n\pi + \theta_{\mathrm{osc}}). \tag{18}$$

Owing to the uncertainty in the initial condition and lock time of the PLL, the value of n may change upon each reinitialization of the frequency synthesizer.

When $N = 1$, the term $2n\pi M/N$ becomes an integer multiple of 2π, which can be omitted regardless of the value of n. Therefore, the initial phase simplifies to

$$\theta_{\mathrm{LO}} \equiv \frac{M}{N}\theta_{\mathrm{osc}}. \tag{19}$$

Under this condition, the actual output signal described by Eq. (17) matches the ideal output signal specified in Eq. (15), and no abrupt initial phase change occurs.

However, when $N \neq 1$, Eq. (19) no longer holds. Different values of n produce distinct initial phases θ_{LO}, leading to abrupt phase changes when the frequency synthesizer is reinitialized. Under this condition, the initial phase θ_{LO} may assume N distinct values, which decrease sequentially by $2\pi/N$ from the largest to the smallest.

Therefore, in practical applications, to prevent abrupt initial phase changes induced by the frequency synthesizer, the output signal frequency should be configured as an integer multiple of the input signal frequency.

3.6 Digital phase-locked loop and coherent turnaround

The digital phase-locked loop (DPLL) is implemented within the FPGA. The master DPLL locks onto the carrier phase difference at zero frequency, while the slave DPLL tracks the carrier frequency offset resulting from the crystal oscillator frequency deviation between the master and slave units. Both the master and slave DPLLs achieve 1 : 1 phase locking in the digital domain.

The phase difference obtained by the master DPLL is directly used for distance computation and does not introduce phase changes. In contrast, the carrier frequency offset acquired by the slave DPLL is multiplied by the coherent turnaround ratio k and then applied to the slave transmitted carrier to maintain coherence between the transmitted and received signals. Consequently, the slave DPLL combined with the coherent turnaround module is functionally equivalent to a DPLL that contains a frequency divider. Under this condition, the input signal to this module can be expressed as

$$S_{\mathrm{i}}(t)=\sin(2\pi f_{\mathrm{i}}t+\theta_{\mathrm{i}}), \tag{20}$$

where f_{i} represents the frequency of the input signal, and θ_{i} denotes its initial phase. The output signal of this module is given by

$$S_{\mathrm{o}}(t)=\sin(2\pi f_{\mathrm{o}}t+\theta_{\mathrm{o}}), \tag{21}$$

where f_{o} and θ_{o} denote the frequency and initial phase of the output signal, respectively.

The ideal output signal of this module can be expressed as

$$S_{\mathrm{o}}(t)=\sin\left[k(2\pi f_{\mathrm{i}}t+\theta_{\mathrm{i}})\right]. \tag{22}$$

However, based on the analysis in Section 3.5, the actual output signal is

$$S_{\mathrm{o}}(t)=\sin\left[k(2\pi f_{\mathrm{i}}t+2n\pi+\theta_{\mathrm{i}})\right], \tag{23}$$

with the initial phase described as

$$\theta_{\mathrm{o}}=k(2n\pi+\theta_{\mathrm{i}}). \tag{24}$$

Based on the analysis in Section 3.5, when the coherent turnaround ratio k is a positive integer, the term $k\cdot 2n\pi$ constitutes an integer multiple of 2π and can be omitted regardless of the value of n. In this case, the actual output signal matches the ideal output signal, and no phase change occurs. However, when k is a non-integer, the term $k\cdot 2n\pi$ cannot be omitted. Variations in n will lead to corresponding changes in the phase of the actual output signal. Assuming that

$$k=\frac{P}{Q}, \tag{25}$$

where both P and Q are positive integers and P/Q is irreducible. Under these conditions, the initial phase θ_{o} may assume Q distinct values, and these Q values decrease sequentially by $2\pi/Q$ from the largest to the smallest.

Therefore, in practical applications, to prevent phase changes induced by coherent turnaround, the carrier frequency of the slave unit should be configured as an integer multiple of the master's transmitted carrier frequency.

4 Simulations of abrupt phase changes in the dual transponder carrier ranging system

To validate the analysis and solution for abrupt phase changes presented in Section 3, a parameter-configurable simulation model is built in Simulink, as illustrated in Fig. 5, and multiple simulation runs are conducted.

In the simulation architecture, M-CLKGEN represents the master clock generation module, while S-CLKGEN corresponds to the slave clock generation module. These modules generate the original sinusoidal clock signals and the square-wave clocks required by the digital processing units in the transceivers. M-TX denotes the master transmitter module, while S-TX refers to the slave transmitter module. Both modules generate digital intermediate frequency (IF) signals and analog LO signals, which are upconverted to RF. Additionally, S-TX incorporates a coherent turnaround module. M-RX indicates the master receiver module, and S-RX represents the slave receiver module. These modules downconvert the received analog signals to IF, digitize them, and then deliver the resulting digital signals to the DPLL for phase tracking.

4.1 Abrupt phase changes induced by frequency synthesizers

To validate the analysis in Section 3.5, the output-to-input frequency ratio of the frequency synthesizer is set to 10.8, while the coherent turnaround ratio is maintained at 2. A total of 100 simulations are conducted, and after each simulation,

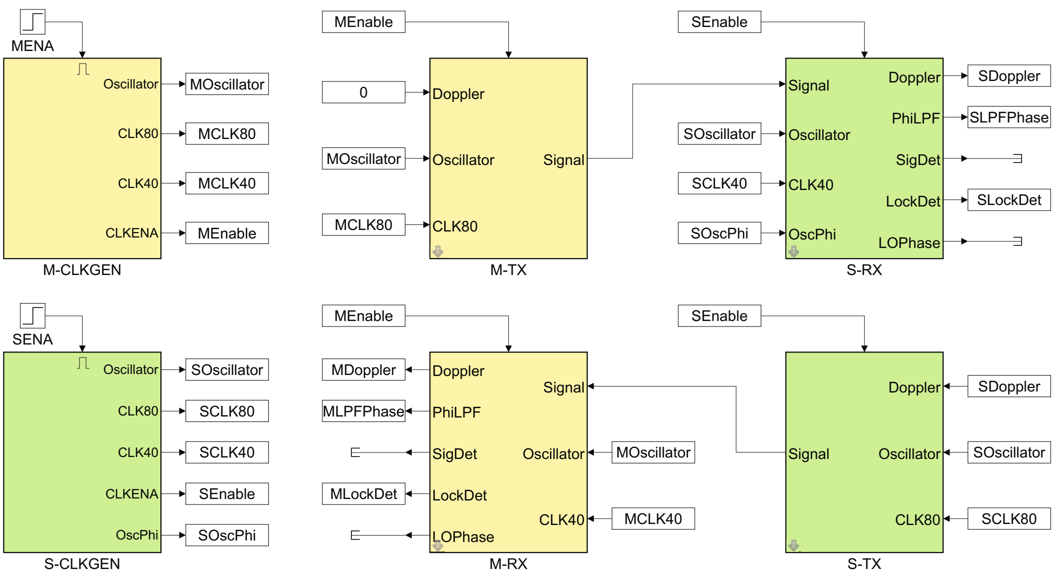

Fig. 5 Schematic diagram of the Simulink simulation model (MENA: master-enable; SENA: slave-enable)

the system is restarted for the next one. Fig. 6 displays the phase data collected during the first seven simulations. As shown, the stabilized initial phase values after each restart are inconsistent.

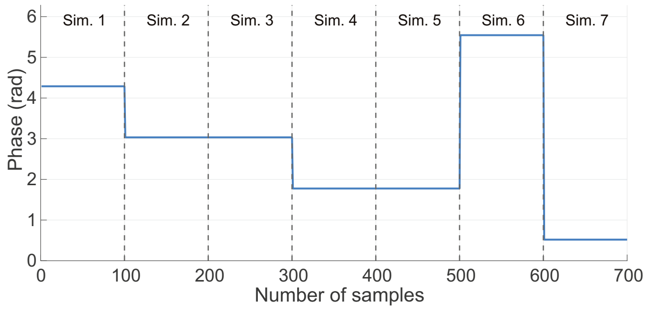

Fig. 6 Simulation results of the fractional output-to-input frequency ratio of the frequency synthesizer (Sim.: simulation)

The average phase value is computed for each simulation, and the results from all 100 simulation runs are summarized in Table 2. The simulation results converge to five distinct phase values, which increase sequentially by $2\pi/5$ from the smallest to the largest. This discrete distribution aligns precisely with the theoretical predictions presented in Section 3.5.

Table 2 Simulation results of the fractional output-to-input frequency ratio of the frequency synthesizer

Average phase (rad)	Number of occurrences
0.52±0.01	14
1.78±0.01	20
3.03±0.01	21
4.29±0.01	21
5.55±0.01	24

4.2 Abrupt phase changes induced by coherent turnaround

To validate the analysis in Section 3.6, the output-to-input frequency ratio of the frequency synthesizer is set to a positive integer, while the coherent turnaround ratio is configured as 1.6. A total of 100 simulations are conducted, and after each simulation, the system is restarted for the next one. Fig. 7 shows the phase data obtained from the first seven simulations. As shown, the stabilized initial phase values after each restart are inconsistent.

The average phase value is computed for each simulation, and the results from all 100 simulation runs are summarized in Table 3. The simulation results exhibit five distinct phase values, which increase sequentially by $2\pi/5$ from the smallest to the largest. This behavior is consistent with the theoretical analysis provided in Section 3.6.

5 Experiments on abrupt phase changes in the dual transponder carrier ranging system

To validate the theoretical analysis presented in Section 3 and the simulation results from Section 4, an experimental

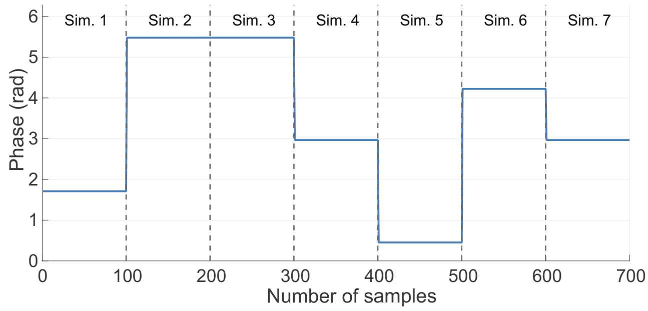

Fig. 7 Simulation results of the fractional coherent turnaround ratio

Table 3 Simulation results of the fractional coherent turnaround ratio

Average phase (rad)	Number of occurrences
0.45±0.01	21
1.71±0.01	13
2.97±0.01	26
4.22±0.01	22
5.48±0.01	18

platform for the dual transponder carrier ranging system is constructed, as illustrated in Fig. 8. The platform uses an OCXO to supply the reference clock signal. The transceiver modules on the ranging boards operate within the S-band; hence, the forward signal is transmitted in the S-band. By employing external frequency synthesizers and mixers, the return signal is upconverted to the C-band. Except for differences in transmission/reception frequencies and their associated peripheral circuits (e.g., filters), the hardware configurations of the master and slave units are identical.

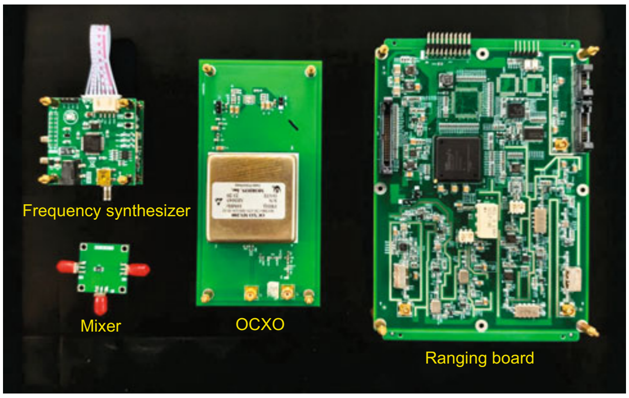

Fig. 8 Experimental platform

5.1 Abrupt phase changes induced by frequency synthesizers

To verify the abrupt phase changes induced by a fractional output-to-input frequency ratio in the frequency synthesizer, the output-to-input frequency ratio of the frequency synthesizer is set to a non-integer value, while the coherent turnaround ratio is configured as an integer. The specific parameter configuration of the experimental platform is summarized in Table 4.

After the hardware reaches full thermal stability, the external frequency synthesizers of both the master and slave units

Table 4 System parameter configuration for a fractional output-to-input frequency ratio of the frequency synthesizer

Parameter	Value
Frequency of the OCXO (MHz)	10
System forward frequency (MHz)	2166
System return frequency (MHz)	6498
Output frequency of the frequency synthesizer (MHz)	4146
Output-to-input frequency ratio of the frequency synthesizer	414.6
Coherent turnaround ratio	3

are reset multiple times, and the phase data are recorded. Since integer phase ambiguity is not resolved in the experiment, all phase results are constrained to the interval $[0, 2\pi)$. Fig. 9 displays the phase measurement results. The abrupt phase changes observed after each frequency synthesizer restart correspond to transitions among five distinct values, which decrease sequentially by $2\pi/5$ from the largest to the smallest. This behavior is consistent with the theoretical analysis in Section 3.5 and aligns with the simulation results in Section 4.1.

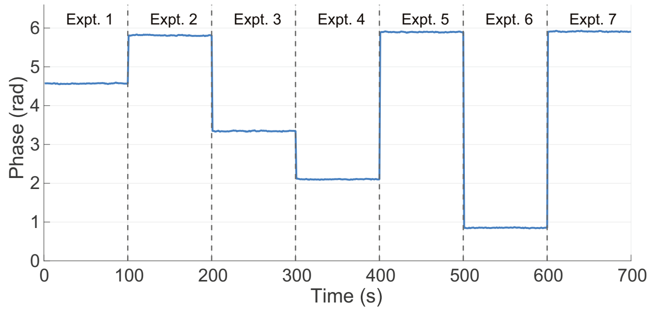

Fig. 9 Experimental results of the fractional output-to-input frequency ratio of the frequency synthesizer

5.2 Abrupt phase changes induced by coherent turnaround

To examine abrupt phase changes caused by a fractional coherent turnaround ratio, the coherent turnaround ratio is set to a non-integer value, while the output-to-input frequency ratio of the frequency synthesizer is configured as an integer in this experiment. The specific parameter configuration of the experimental platform is summarized in Table 5.

After the hardware is fully warmed up, the master and slave units are reset multiple times, and the phase data are recorded. Since integer phase ambiguity is not resolved in the experiment, all phase results are constrained to the interval $[0, 2\pi)$. Fig. 10 displays the phase measurement results. The abrupt phase changes observed upon system restart correspond to changes among four distinct values, which decrease sequentially by $2\pi/4$ from the largest to the smallest. This result aligns with the theoretical analysis provided in Section 3.6 and agrees with the simulation results in Section 4.2.

Table 5 System parameter configuration for a fractional coherent turnaround ratio

Parameter	Value
Frequency of the OCXO (MHz)	10
System forward frequency (MHz)	2160
System return frequency (MHz)	5940
Output frequency of the frequency synthesizer (MHz)	3590
Output-to-input frequency ratio of the frequency synthesizer	359
Coherent turnaround ratio	2.75

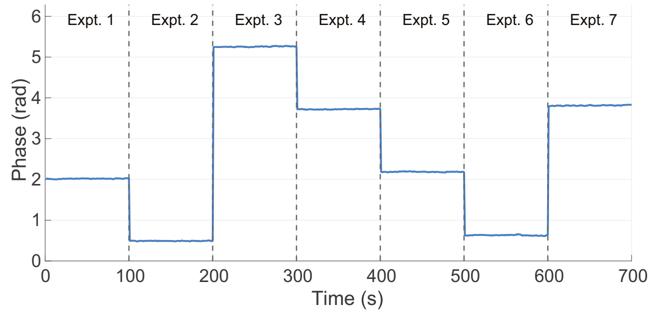

Fig. 10 Experimental results of the fractional coherent turnaround ratio

5.3 Suppression of abrupt phase changes

To validate the solution proposed in Section 3 for addressing the abrupt phase change issue, an experimental scheme for abrupt phase change suppression is designed, in which the coherent turnaround ratio and the output-to-input frequency ratio of the frequency synthesizer are configured as integers. The specific parameter configuration of the experimental platform is summarized in Table 6.

Table 6 System parameter configuration for suppression of initial value changes

Parameter	Value
Frequency of the OCXO (MHz)	10
System forward frequency (MHz)	2160
System return frequency (MHz)	6480
Output frequency of the frequency synthesizer (MHz)	4130
Output-to-input frequency ratio of the frequency synthesizer	413
Coherent turnaround ratio	3

Nine independent system restart tests are performed. For each test, the master unit, slave unit, or frequency synthesizer is reset, and the phase data are recorded after the hardware reaches thermal stability. Since integer phase ambiguity is not resolved in the experiment, all phase results are constrained to the interval $[0, 2\pi)$. Fig. 11 displays the phase and distance measurement results. After the steady-state data from each independent test are averaged, the statistical results are as follows: the standard deviation of the nine averaged phase values is 0.0101 rad, corresponding to a distance standard deviation of 0.0373 mm; the peak-to-peak variation of the nine averaged phase values is 0.0277 rad, corresponding to a peak-to-peak distance of 0.1019 mm. In stark contrast, the initial phase changes observed in Figs. 9 and 10 (where no suppression

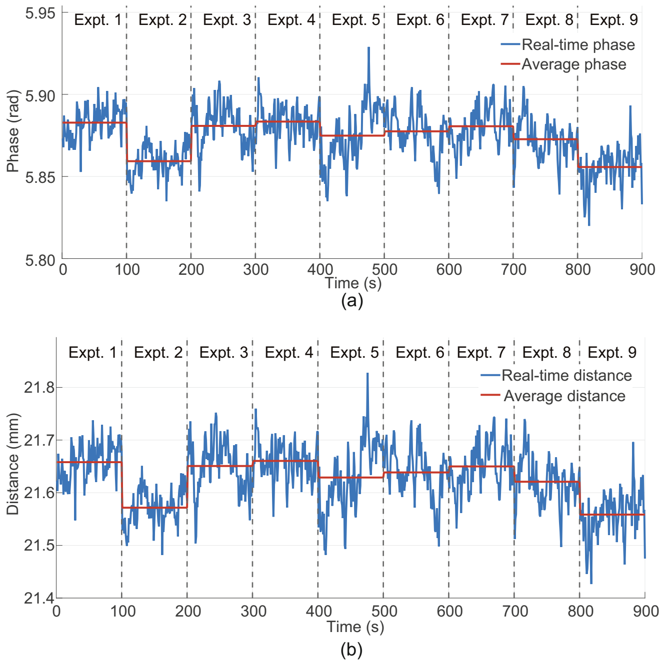

Fig. 11 Suppression of the initial value changes: (a) phase; (b) distance

is applied) exhibit variations of no less than $2\pi/5$ and $2\pi/4$, respectively, corresponding to distance changes of 4.6136 mm and 6.3087 mm.

The above results indicate that the deterministic and large-magnitude initial phase changes caused by system restarts have been effectively eliminated. The remaining phase fluctuations are attributed to stochastic noise, which is primarily induced by factors such as the phase noise of the crystal oscillator and the thermal noise of the receiver. Critically, these fluctuations no longer contain discrete change components caused by the frequency synthesizer or coherent turnaround, confirming the effectiveness of the proposed solution as analyzed in Section 3.

6 Conclusions

In this paper, a detailed theoretical analysis reveals that the fractional output-to-input frequency ratio and the non-integer coherent turnaround ratio are the primary causes of the initial value changes in the dual transponder carrier ranging system, and corresponding solutions are proposed. Furthermore, the theoretical analysis elucidates the quantitative relationship between the number of discrete initial values and these ratios. Simulation results confirm that the change of the initial value upon system restart is discrete, fluctuating strictly within a set of fixed values, which aligns perfectly with the theoretical analysis. The effectiveness of the proposed method for suppressing the initial value changes is experimentally validated; specifically, configuring both the output-to-input frequency ratio of the frequency synthesizer and the coherent turnaround ratio as integers effectively suppresses this change. This suppression enables stable and repeatable absolute distance measurements, significantly enhancing the system's practical viability in high-precision ranging applications. Moreover, the analysis presented in this study can serve as a valuable reference for frequency planning of similar absolute distance measurement systems in the future.

Author contributions

Tao ZHANG designed the research, processed the data, and drafted the paper. Ziru LI helped organize the paper. Zhaobin XU and Zhonghe JIN revised and finalized the paper.

Conflict of interest

Zhonghe JIN is an editorial board member of *ENGINEERING Information Technology & Electronic Engineering*, and he was not involved with the peer review process of this paper. All the authors declare that they have no conflict of interest.

Data availability

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Declaration on the use of generative AI tools

During the preparation of this work, the authors used DeepSeek and Gemini to improve language. After using these tools, the authors reviewed and edited the content as needed and take full responsibility for the content of the published article.

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