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Design and analysis of carbon nanotube FET based quaternary full adders

Mohammad Hossein MOAIYERI[†‡1,2], Shima SEDIGHIANI[2], Fazel SHARIFI[2], Keivan NAVI[2]

([1]*Faculty of Electrical Engineering, Shahid Beheshti University, Tehran 1983963113, Iran*)

([2]*Nanotechnology and Quantum Computing Lab, Shahid Beheshti University, Tehran 1983963113, Iran*)

[†]E-mail: h_moaiyeri@sbu.ac.ir

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Abstract: CMOS binary logic is limited by short channel effects, power density, and interconnection restrictions. The effective solution is non-silicon multiple-valued logic (MVL) computing. This study presents two high-performance quaternary full adder cells based on carbon nanotube field effect transistors (CNTFETs). The proposed designs use the unique properties of CNTFETs such as achieving a desired threshold voltage by adjusting the carbon nanotube diameters and having the same mobility as p-type and n-type devices. The proposed circuits were simulated under various test conditions using the Synopsys HSPICE simulator with the 32 nm Stanford comprehensive CNTFET model. The proposed designs have on average 32% lower delay, 68% average power, 83% energy consumption, and 77% static power compared to current state-of-the-art quaternary full adders. Simulation results indicated that the proposed designs are robust against process, voltage, and temperature variations, and are noise tolerant.

Key words: Nanoelectronics, Carbon nanotube FET, Multiple-valued logic, Quaternary logic
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1 Introduction

Technology dimension scaling, which increases the chip density and the number of economic circuits, is significant due to the widespread use of wireless communication and portable computing systems. Power density, design complexity, fabrication costs, and robustness are the important concerns for digital circuits and systems design. By the continuous scaling down of the feature size, interconnection has become the dominant component of delay, area, and power consumption in modern chips. Therefore, to overcome these problems and limitations, finding a new computing method seems to be a necessity.

The use of multiple-valued logic (MVL) can be an ultimate and suitable solution to solve the limitations of scaling. First, more data can be transferred by MVL in wired communication and consequently a dramatic reduction in chip area, complexity, and power consumption of wires can be achieved. In addition, serial-parallel arithmetic operation can be carried out faster (Hurst, 1984; Dubrova, 1999; Navi *et al.*, 2011). Thereby, lower chip complexity, increased computational ability, higher performance and reduced interconnect congestion motivate the use of MVL in a wide variety of applications.

Although ternary logic (radix-3) has been proved to be the most efficient MVL system (Hurst, 1984), quaternary logic has the advantage of easier communication with binary logic circuits and consequently less complex radix conversions.

The development of nanoelectronics has introduced new materials and devices with many key properties which can help researchers to overcome physical limitations and challenges caused by MOSFET scaling (Mansoori and Soelaiman, 2005). Considering the nanodevices introduced so far,

‡ Corresponding author
ORCID: Mohammad Hossein MOAIYERI, http://orcid.org/0000-0001-9711-7923

carbon nanotube field effect transistors (CNTFETs) are most likely to succeed in replacing MOSFET in future because of their electrical behavior and physical structure. Their very high carrier mobility, considerably higher carrier saturation velocity, near ballistic carrier transport, equal mobility for electrons and holes, very low OFF-current, and easy integration with high-k insulation materials give CNTFETs great potential for improving the performance of integrated circuits. More importantly, the desired CNTFET threshold voltage can be achieved by adjusting the diameter of the CNTs (Liang *et al.*, 2014). Many feasible and effective strategies have already been published for growing CNTs with a specified chirality and adopting the desired threshold voltage for multi-tube CNTFETs (Chen *et al.*, 2007; Lin *et al.*, 2009; Yang *et al.*, 2014).

Three types of CNTFETs have been introduced, SB-CNTFET, T-CNTFET, and MOSFET-like CNTFET. Of these, MOSFET-like CNTFET behaves like a normal MOSFET and demonstrates unipolar characteristics. Furthermore, it is suitable for ultra-high-performance CMOS-like designs because of its high I_{ON}/I_{OFF} ratio (Raychowdhury and Roy, 2007). In this study, MOSFET-like CNTFETs were used for the design and simulation of all circuits.

MVL circuit designs based on CNTFET have attracted attention in recent years and many CNTFET-based binary and ternary logic and arithmetic circuits have been proposed (Raychowdhury and Roy, 2005; Lin *et al.*, 2011; Moaiyeri *et al.*, 2011; Liang *et al.*, 2014). However, less effort has been put into developing quaternary full adders due to a lack of efficient circuit models and design challenges, especially for those based on MOSFET. Previous MOSFET-based quaternary full adders were designed using depletion-mode devices, which are not applicable to recent nanoscale FET technologies (Thoidis *et al.*, 1998; Datla *et al.*, 2009). The adder is undoubtedly the most important circuit among the various processing elements used in a microprocessor. Performance improvement of signal processors depends mainly on the development of adder circuits. Therefore, designing an efficient CNTFET-based quaternary full adder cell supporting all the possible logic values for near future non-silicon non-binary integrated circuits and systems is of considerable interest.

This paper presents two quaternary full adders using CNTFET as an emerging nanotechnology. Since the proposed quaternary cells functionality supports all the possible quaternary logics for all three inputs, they can also be referred to as quaternary 3-to-2 compressor circuits (Datla, 2009). There is no need for radix conversions to perform quaternary arithmetic operations in the proposed designs, which makes these designs more efficient than previous systems.

2 Review of quaternary logic design

MVL circuits can be designed by increasing the domain of binary algebra form {0, 1} to {0, 1, …, $M-1$}, $M>2$. For quaternary logic, M is 4 with domain $D\in\{0, 1, 2, 3\}$, and the high to low logic voltage level is divided into four levels, which can be considered around 0 V, $1/3V_{DD}$, $2/3V_{DD}$, and V_{DD}. The quaternary AND, OR, and NOT operations are the three most significant operations for implementing other quaternary logic functions. These basic functions can be defined as follows:

$$a\cdot b=\min(a, b), \tag{1}$$

$$a+b=\max(a, b), \tag{2}$$

$$\mathrm{NOT}(a)=3-a. \tag{3}$$

Since half adders (HAs) and full adders (FAs) are considered as the basic elements in almost all arithmetic circuits, optimized MVL half adders and full adders can significantly improve the performance of MVL processing units. A half adder was proposed by Moaiyeri (2012) (Fig. 1). High-performance operation in the presence of process variations has been reported for this design. This design method is based on a quaternary four-to-one multiplexer (MUX) which uses a quaternary decoder and CNTFET-based transmission switches (QTG) as building blocks, and is described in detail by Moaiyeri (2012). The design of the sub-circuits presented by Moaiyeri (2012) was based on transmission switches, pass transistors and threshold detectors.

Based on Eqs. (1) and (2) and a quaternary full adder with A, B, C_{in} inputs, Eqs. (4) and (5) for quaternary Sum and C_{out} outputs can be derived, where X_0, X_1, X_2, and X_3 binary signals are high, when X is equal to 0, 1, 2, and 3, respectively:

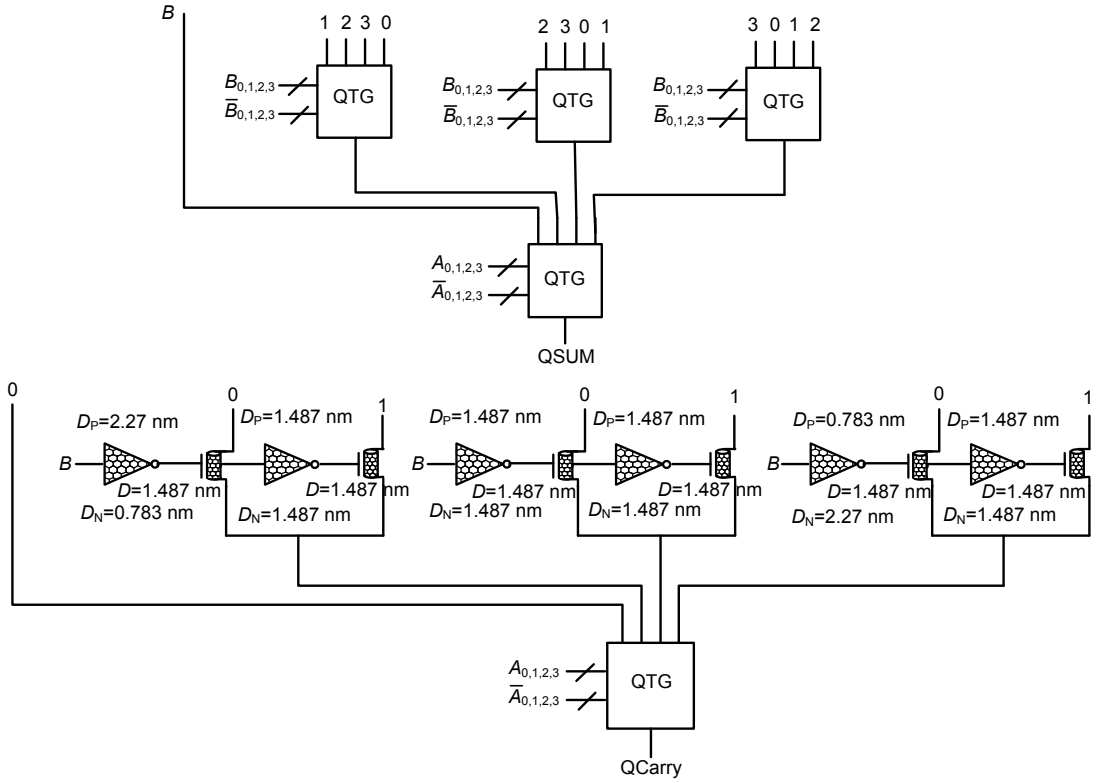

Fig. 1 The quaternary half adder presented by Moaiyeri *et al.* (2012)

$$\begin{aligned}\mathrm{SUM} = {} & 1.(C_{\mathrm{in}0}A_0B_1 + C_{\mathrm{in}0}A_0B_1 + C_{\mathrm{in}0}A_2B_3 + C_{\mathrm{in}1}A_0B_0 + C_{\mathrm{in}1}A_1B_3 + C_{\mathrm{in}1}A_3B_1 + C_{\mathrm{in}1}A_2B_2 \\ & + C_{\mathrm{in}2}A_0B_3 + C_{\mathrm{in}2}A_1B_2 + C_{\mathrm{in}2}A_2B_1 + C_{\mathrm{in}2}A_3B_0 + C_{\mathrm{in}3}A_0B_2 + C_{\mathrm{in}3}A_1B_1 + C_{\mathrm{in}3}A_2B_0 + C_{\mathrm{in}3}A_3B_3) \\ & + 2.(C_{\mathrm{in}0}A_0B_2 + C_{\mathrm{in}0}A_1B_1 + C_{\mathrm{in}0}A_2B_0 + C_{\mathrm{in}0}A_3B_3 + C_{\mathrm{in}1}A_0B_1 + C_{\mathrm{in}1}A_1B_0 + C_{\mathrm{in}1}A_2B_3 + C_{\mathrm{in}1}A_3B_2 \\ & + C_{\mathrm{in}2}A_0B_0 + C_{\mathrm{in}2}A_1B_3 + C_{\mathrm{in}2}A_2B_2 + C_{\mathrm{in}2}A_3B_1 + C_{\mathrm{in}3}A_0B_3 + C_{\mathrm{in}3}A_1B_2 + C_{\mathrm{in}3}A_2B_1 + C_{\mathrm{in}3}A_3B_0) \\ & + 3.(C_{\mathrm{in}0}A_0B_3 + C_{\mathrm{in}0}A_1B_2 + C_{\mathrm{in}0}A_2B_1 + C_{\mathrm{in}0}A_3B_0 + C_{\mathrm{in}1}A_0B_2 + C_{\mathrm{in}1}A_1B_1 + C_{\mathrm{in}1}A_2B_0 + C_{\mathrm{in}1}A_3B_3 \\ & + C_{\mathrm{in}2}A_0B_1 + C_{\mathrm{in}2}A_1B_0 + C_{\mathrm{in}2}A_2B_3 + C_{\mathrm{in}2}A_3B_2 + C_{\mathrm{in}3}A_0B_0 + C_{\mathrm{in}3}A_1B_3 + C_{\mathrm{in}3}A_3B_1),\end{aligned} \tag{4}$$

$$\begin{aligned}\mathrm{QC}_{\mathrm{out}} = {} & 1.(C_{\mathrm{in}0}A_1B_3 + C_{\mathrm{in}0}A_2B_2 + C_{\mathrm{in}0}A_2B_3 + C_{\mathrm{in}0}A_3B_1 + C_{\mathrm{in}0}A_3B_2 + C_{\mathrm{in}0}A_3B_3 + C_{\mathrm{in}1}A_0B_3 \\ & + C_{\mathrm{in}1}A_1B_2 + C_{\mathrm{in}1}A_1B_3 + C_{\mathrm{in}1}A_2B_1 + C_{\mathrm{in}1}A_2B_2 + C_{\mathrm{in}1}A_2B_3 + C_{\mathrm{in}1}A_3B_0 + C_{\mathrm{in}1}A_3B_1 + C_{\mathrm{in}1}A_3B_2 \\ & + C_{\mathrm{in}1}A_3B_3 + C_{\mathrm{in}2}A_0B_2 + C_{\mathrm{in}2}A_0B_3 + C_{\mathrm{in}2}A_1B_1 + C_{\mathrm{in}2}A_1B_2 + C_{\mathrm{in}2}A_1B_3 + C_{\mathrm{in}2}A_2B_0 + C_{\mathrm{in}2}A_2B_1 \\ & + C_{\mathrm{in}2}A_2B_2 + C_{\mathrm{in}2}A_2B_3 + C_{\mathrm{in}2}A_3B_0 + C_{\mathrm{in}2}A_3B_1 + C_{\mathrm{in}2}A_3B_2 + C_{\mathrm{in}3}A_0B_1 + C_{\mathrm{in}3}A_0B_2 + C_{\mathrm{in}3}A_0B_3 \\ & + C_{\mathrm{in}3}A_1B_0 + C_{\mathrm{in}3}A_1B_1 + C_{\mathrm{in}3}A_1B_2 + C_{\mathrm{in}3}A_1B_3 + C_{\mathrm{in}3}A_2B_0 + C_{\mathrm{in}3}A_2B_1 + C_{\mathrm{in}3}A_2B_2 + C_{\mathrm{in}3}A_3B_0 \\ & + C_{\mathrm{in}3}A_3B_1) + 2.(C_{\mathrm{in}2}A_3B_3 + C_{\mathrm{in}3}A_2B_3 + C_{\mathrm{in}3}A_3B_2 + C_{\mathrm{in}3}A_3B_3).\end{aligned} \tag{5}$$

A method for designing quaternary adders was presented by da Silva *et al.* (2006) based on down literal and successor circuits and transmission gate networks. This circuit was designed specifically for quaternary logic computations.

A quaternary adder was introduced by Sharifi *et al.* (2015) based on efficient quaternary-to-binary and binary-to-quaternary radix converters. The addition in this design is performed by means of a transmission gate based (3, 3, 4) compressor.

A radix-4 full adder was presented by Asif and Vesterbacka (2012). This design uses only two states for the input carry digit (0 and 1), which makes it unsuitable for being used as a building block of larger quaternary adders. In addition, to perform quaternary arithmetic operations with a radix-4 FA block, input

quaternary signals (quaternary input signals) should be converted to binary signal. Moreover, converting binary output signals of a radix-4 full adder to quaternary signals is needed. To achieve a complete quaternary full adder in which input and output signals are all quaternary, we modified the radix-4 FA using a binary-to-quaternary conversion before addition and a quaternary-to-binary conversion after addition (Patel and Gurumurthy, 2010).

The two designs last mentioned are inherently binary, which reduces the advantages of MVL and imposes high delay and power overheads.

3 Proposed quaternary full adders

Although a gate-level method like the one proposed by Lin *et al.* (2011) for ternary logic can be used for designing a quaternary adder circuit, it is not an efficient approach because of increasing critical path length and considerable circuit overhead. However, a quaternary full adder can be built by cascading two half adders to add three quaternary inputs *A*, *B*, and *C*, and generate a quaternary sum and a quaternary output carry (QC_{out}) as shown in Fig. 2.

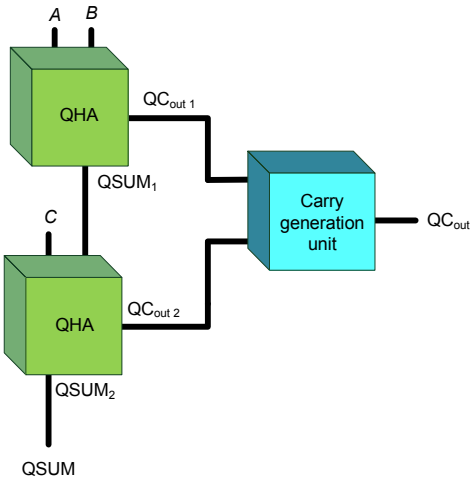

Fig. 2 The block diagram of the proposed quaternary full adder

This means that quaternary full addition can be fragmented into quaternary half addition and carry generation operations. By designing the quaternary half adder according to Moaiyeri *et al.* (2012) and the content of Table 1, two novel quaternary full adders are proposed.

Table 1 Deriving final carry based on the partial carries

$QC_{out\,1}$	$QC_{out\,2}$	QC_{out}
0	0	0
0	1	1
1	0	1
1	1	2

The context of Table 1 shows that QC_{out} at the output of the carry generation unit may have '0', '1', and '2' logic values equivalent to 0, 0.3, and 0.6 V voltage levels, respectively. It means a ternary module can be used instead of a quaternary one for the carry generation unit, which leads to a saving in the number of transistors. The next two subsections present two different designs for the carry generation unit.

3.1 The first proposed carry generation unit

Based on Table 1 and the complementary CNTFET-based design method, the first proposed idea has a structure based on two CNTFET binary inverters with a 0.6 V power supply, which are cascaded in two parallel paths (Fig. 3). The QC_{out} calculation is generated based on voltage division of *X* and *Y* signals, which are connected by means of p-type and n-type CNTFET switches. Only two different CNT diameters are needed for adjusting the transition point of inverters. In this scheme, for CNTFETs with diameters of 0.783 nm and 1.487 nm, the chirality numbers would be (10, 0) and (19, 0), respectively, and accordingly the threshold voltage values ($|V_t|$) would be 0.557 and 0.293 V, respectively. The relationships between chirality numbers, CNT diameter, and CNTFET threshold voltage have been given in detail by Kim *et al.* (2009) and Sharifi *et al.* (2015).

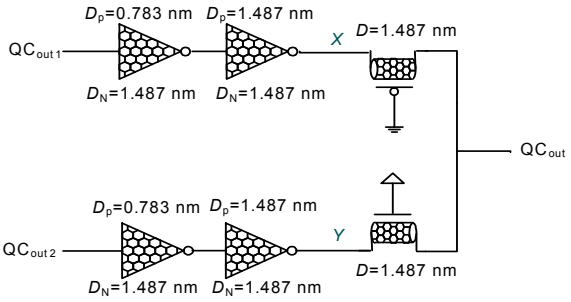

Fig. 3 The first proposed carry generation unit

The operation of the carry generation unit can be briefly described as follows:

If the inputs ($QC_{out\,1}$ and $QC_{out\,2}$) become '0', the output of the first inverter in each path will be equal to logic '2' because of being driven by a $2/3 \cdot V_{DD}$ supply. This voltage produces the required V_t to turn on the n-FET of the next inverters and this condition forces the X and Y nodes to be shorted to ground. Consequently, the output voltage of QC_{out} also equals logic '0'. If the inputs become '1', the output voltage of the first inverter in each path will be equal to 0 V due to being driven by ground. Then, it turns on the p-FET of the next inverters, which results in the output voltage of QC_{out} also being equal to logic '1'. Finally, if one of the inputs becomes '1' and the other becomes '0', the outputs of the inverters will be logic '2' and '0', respectively, and by a voltage division, logic '1' is produced at the output of QC_{out}. Note that when inputs are the same, there is no static power as no ON path exists from V_{DD} to ground.

3.2 The second proposed carry generation unit (based on a multiplexer)

Another efficient method to design the carry generation unit is based on an efficient design of a binary two-to-one MUX. This MUX consists of a CNTFET binary decoder, transmission switches and inverters (Fig. 4). The decoder produces signals S_0 and S_1 as the input signals for MUX, which act as selectors in the transmission gates. Other required selector signals are generated by the CNTFET-based inverters. According to the logic of QC_{out} (Table 1), when $QC_{out\,1}$ is '0', the QC_{out} signal is similar to $QC_{out\,2}$ and consequently $QC_{out\,1}$ can be transferred to the output. In addition, this proposed carry generator uses a simple module to generate the QC_{out} signal when $QC_{out\,1}$ is '1'.

This simple module is constructed based on the n-type CNTFET switches, which are controlled by the $QC_{out\,2}$ through the inverter, acting as threshold detectors.

The design of all the modules of the proposed quaternary full adders is based mainly on transmission switches, pass transistors and threshold detectors. Designing at switch level can considerably enhance the performance and efficiency of the circuits (Wu, 1992; Wu and Prosser, 1996; Pedram and Wu, 1997).

In addition, for designing the proposed quaternary full adders, only three distinct CNT diameters are required, which enhances the manufacturability and robustness of the designs.

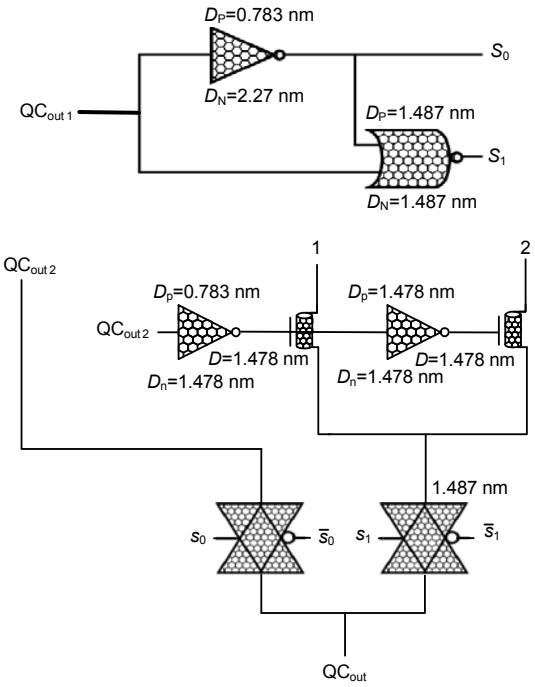

Fig. 4 The second proposed carry generation unit

4 Simulation results and comparison

In this section, the performance of the proposed quaternary full adders is examined under various conditions and is compared with those of previous designs. For this purpose, designs were simulated through a Synopsys HSPISE simulator using the 32 nm Stanford CNTFET comprehensive SPICE model including non-idealities (Deng, 2007; Deng and Wong, 2007a; 2007b). This standard model has been designed for MOSFET-like CNTFET devices, in which one or more CNTs are used in each channel of the transistor. This model also considers parasitic, inter-CNT charge screening, Schottky barrier effects at the contacts, and doped source-drain extension regions. Furthermore, the model includes a full transcapacitance network for more accurate transient and dynamic performance simulations. The important parameters of the CNTFET and their values, with brief descriptions, are shown in Table 2 (Deng and Wong, 2007a; 2007b).

This precise model is commonly used to simulate the CNTFET-based logic and arithmetic building blocks. However, to simulate larger circuits, this model will be quite time consuming and even may not

converge in a reasonable time. For larger circuits, other semiempirical SPICE models based on analytical approximations proposed by Marani and Perri (2011; 2012; 2014), Gelao *et al.* (2011), and Marani *et al.* (2013; 2014) are recommended, which considerably reduces the computational time.

Table 2 Some MOSFET-like CNTFET model parameters

Parameter	Value
Physical channel length	32 nm
Mean free path in the intrinsic CNT	100 nm
Length of doped CNT drain-side region	32 nm
Length of doped CNT source-side region	32 nm
Mean free path in p^+/n^+ doped CNT	15 nm
Distance between the centers of two adjacent CNTs within the same gate	≤30 nm
Sub-lithographic pitch	4 nm
Thickness of high-*k* top gate dielectric	4 nm
Dielectric constant of high-*k* top gate dielectric material (HfO_2)	16
Dielectric constant of substrate (SiO_2)	4
Coupling cap between the channel region and the substrate (SiO_2)	40 aF/μm
Fermi level of the doped S/D CNT	6 eV
Work function of S/D metal contacts	4.6 eV
CNT work function	4.5 eV

The proposed CNTFET-based quaternary adders were compared with the existing quaternary full adders reviewed in Section 3. To make the comparisons fairer, all the previous circuits were redesigned and optimized in terms of energy efficiency based on the CNTFET technology.

The quaternary adders were simulated at room temperature and with a 0.9 V supply voltage considering a 0.7 fF load capacitance and with quaternary input signals based on Thoidis *et al.* (1998). Fig. 5 indicates the transient responses of the proposed quaternary full adders, which confirms their correct functionality.

The simulation results, including propagation delay, average power consumption, average energy, and static power consumption of the quaternary full adders, are listed in Table 3.

The proposed designs have considerably fewer transistors than the quaternary full adder of da Silva *et al.* (2006) but have more than the designs of Asif and Vesterbacka (2012) and Sharifi *et al.* (2015).

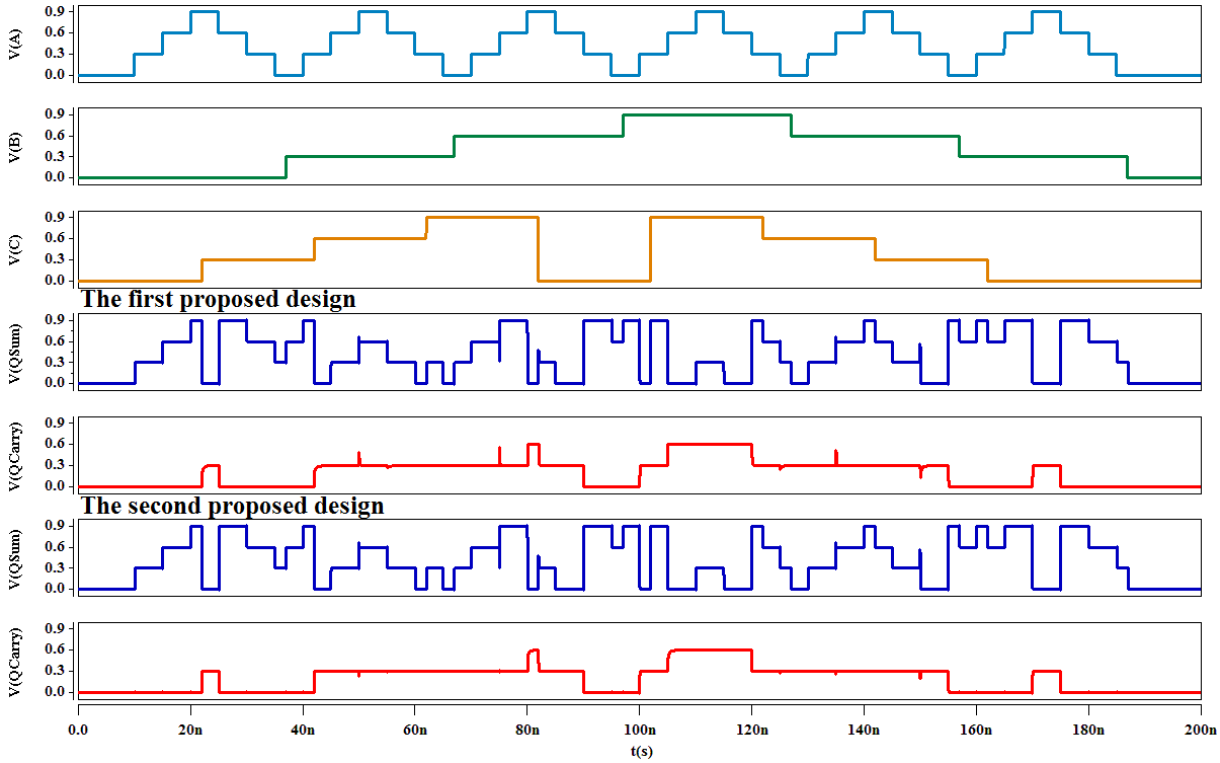

Fig. 5 The transient response of the proposed quaternary full adders

Table 3 Performance comparison of the quaternary adders (QFAs)

Design	Delay (ps)	Power (μW)	Energy (aJ)	Static power (μW)	Number of devices
The first proposed QFA	78.1	8.54	667	3.86	190
The second proposed QFA	85.9	7.67	658	3.51	200
The QFA of da Silva *et al.* (2006)	193.3	13.70	2646	8.51	320
The QFA based on Asif and Vesterbacka (2012)	173.1	37.87	6557	22.48	160
The QFA of Sharifi *et al.* (2015)	71.4	57.73	4125	41.57	154

However, the designs of Asif and Vesterbacka (2012) and Sharifi *et al.* (2015) are not inherently quaternary and the main part of these circuits is a binary circuit.

In addition, these circuits use radix converters which impose a considerable power consumption on the whole design, which is clearly indicated by the results. Moreover, the circuit of Sharifi *et al.* (2015) has four capacitors, which occupy a huge area compared to those of a typical CNTFET.

According to the simulation results, the proposed quaternary full adder designs have a delay comparable to that of the design of Sharifi *et al.* (2015) and significantly lower delay compared with the other designs. In addition, the proposed quaternary full adders have considerably lower average power, energy, and static power consumption than the other quaternary full adder. The higher performance of the proposed designs is due mainly to their shorter critical paths and considerably smaller number of transistors, which lead to smaller path resistance and smaller total switching capacitance.

Generally, comparing the proposed methods, the first one leads to 10 fewer transistors and lower delay. However, the second design has lower average power, energy consumption, and static power dissipation, which makes it more suitable for energy-efficient applications.

To evaluate the performance of the proposed quaternary full adders at different supply voltages, they were simulated at 0.8, 0.9, and 1 V supply voltages. Their propagation delay and average power consumption were measured (Fig. 6). Simulation results indicate the superiority of the novel proposed quaternary full adder circuits, especially in terms of power consumption, at all of these supply voltages.

In addition, the designs were simulated at various temperatures ranging from 0 to 90 °C, at 0.9 V supply voltage, to evaluate their sensitivity to ambient temperature variation. The results indicate little parametric variation in the proposed designs in the presence of temperature variation compared to the other quaternary full adders (Fig. 7).

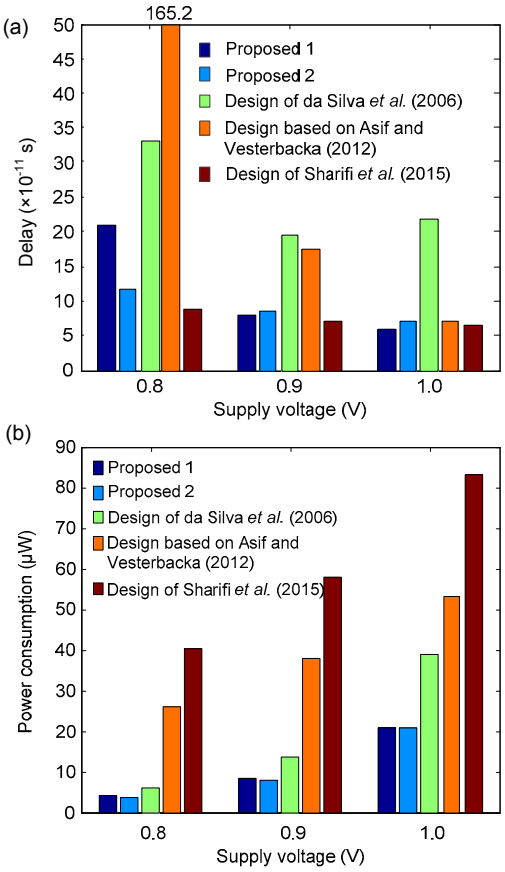

Fig. 6 Performance of the designs at different supply voltages: (a) delay; (b) power consumption

As the design of the proposed CNFEET-based quaternary full adders is based on the multiple V_{th} method, the impact of process variation on the threshold voltage of the CNTFETs should definitely be considered. The most important parameters which impact the operation of a CNTFET are the diameter and density of its nanotubes.

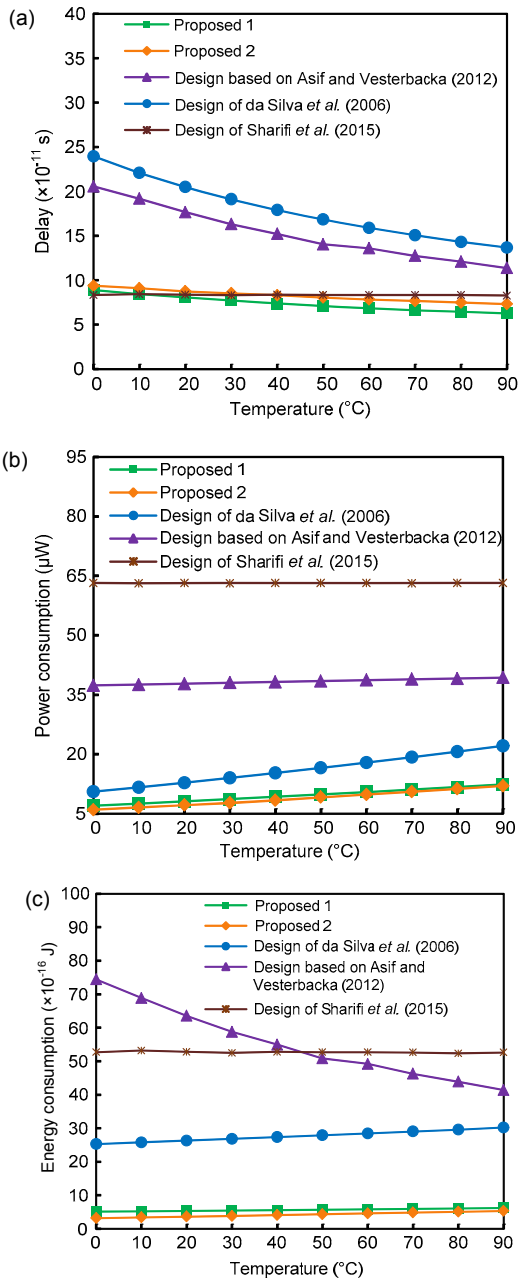

Fig. 7 Performance of the designs versus temperature variations: (a) delay; (b) power consumption; (c) energy consumption

Accordingly, a Monte Carlo simulation was conducted to assess these process variations with ±5 to ±15% Gaussian distributions and variation at the $\pm 3\sigma$ level. Figs. 8 and 9 show the variation in the performance parameters of the quaternary adders against the variation in CNT density and diameter. It can be inferred from the results that the proposed CNTFET-based quaternary full adders are considerably less sensitive to process variations compared to the other designs, due mainly to the considerably lower number of transistors and lower number of required distinct CNT diameters.

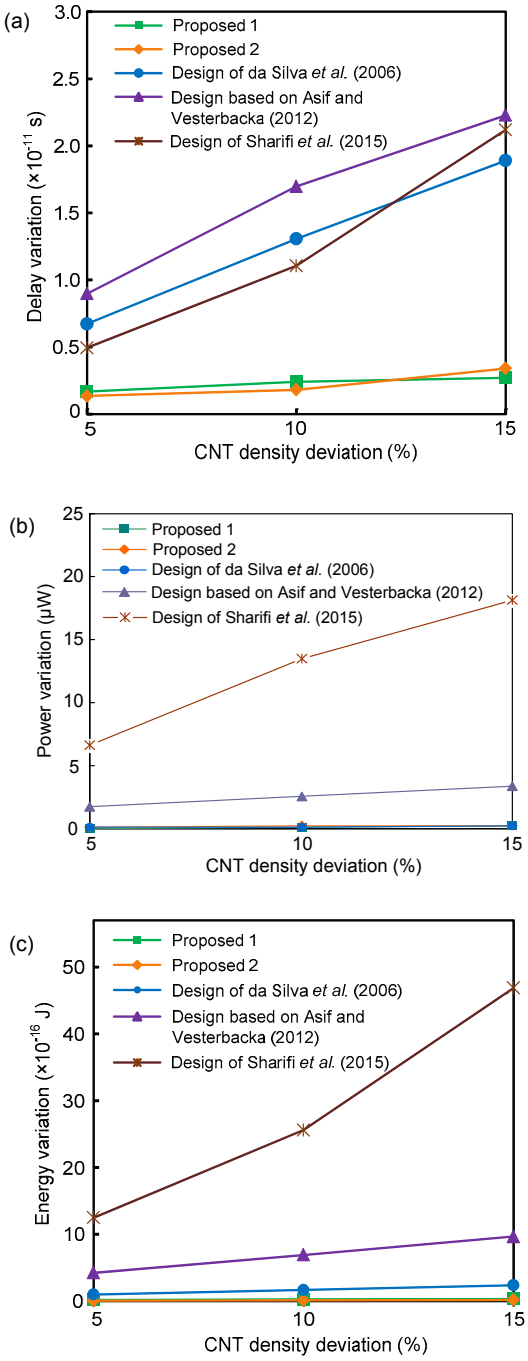

Fig. 8 Parameter variations of the designs with respect to carbon nanotube (CNT) density variation: (a) delay variation; (b) power variation; (c) energy variation

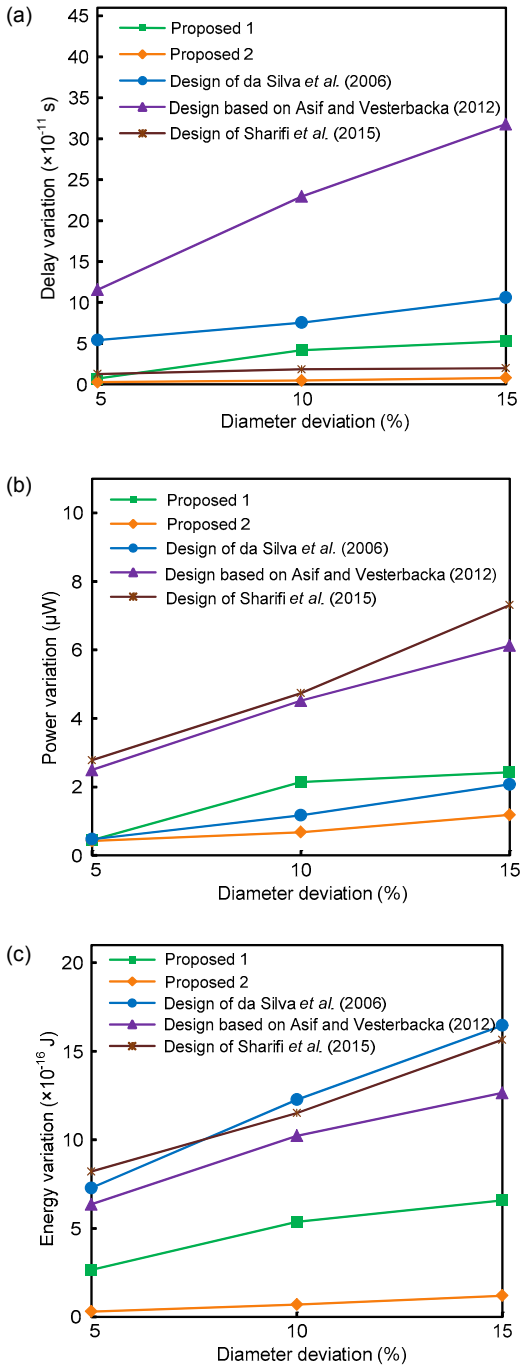

Fig. 9 Parameter variations of the designs with respect to diameter variation: (a) delay variation; (b) power variation; (c) energy variation

The sensitivity of the circuit to input noise becomes more critical in MVL circuits. This makes noise tolerance another important parameter for evaluating circuit performance. To measure the tolerance of the proposed circuits to input noise pulses, a noise immunity curve (NIC) was used. This curve is formed by the loci of input noise pulses with amplitude (V_{noise}) and width (T_{noise}) that appear at the inputs of circuits and cause the circuit to have a logic error. All points above the curve for a particular width represent noise pulses that cause output errors. Thus, a digital circuit with a higher NIC has more noise immunity. A tunable noise generation circuit described in detail by Balamurugan and Shanbhag (2001) was used to obtain the NIC. The NIC results for all the quaternary full adder cells are shown in Fig. 10. According to the results, the proposed designs have higher noise immunity than other quaternary designs, except the design of Sharifi *et al.* (2015) in which the output stage has a capacitive network which enhances the noise immunity but increases its power consumption and area wastage.

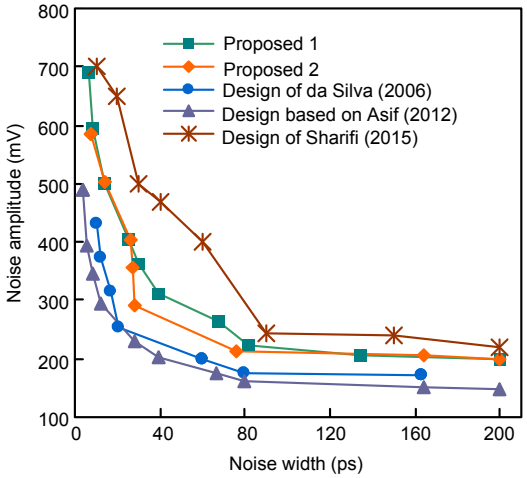

Fig. 10 Noise immunity curves for the proposed quaternary full adders

5 Conclusions

In this paper, two new CNTFET based quaternary full adder cells are proposed. Using the outstanding properties of CNTFETs makes the design of MVL circuits easier and efficient compared to using MOSFETs. The presented circuits were examined using a HSPICE simulator with a 32 nm CNTFET model. The results of the simulations conducted under various conditions indicate that the proposed circuits are faster, consume less power, and consequently have a lower energy consumption than the

state-of-the-art quaternary full adders. In addition, the circuits were precisely analyzed in terms of robustness against process, voltage, and temperature variation and noise, and the results confirm the higher robustness of the proposed designs.

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