Frontiers of Information Technology & Electronic Engineering
www.zju.edu.cn/jzus; engineering.cae.cn; www.springerlink.com
ISSN 2095-9184 (print); ISSN 2095-9230 (online)
E-mail: jzus@zju.edu.cn

A novel PV sub-module-level power-balancing topology for maximum power point tracking under partial shading and mismatch conditions*

Mustafa GOKDAG†[1], Mehmet AKBABA[2]

([1]*Department of Electrical-Electronics Engineering, Karabuk University, Karabuk 78050, Turkey*)

([2]*Department of Computer Engineering, Karabuk University, Karabuk 78050, Turkey*)

†E-mail: mgokdag@karabuk.edu.tr

Received Oct. 7, 2015; Revision accepted Feb. 25, 2016; Crosschecked Oct. 17, 2016

Abstract: Partial shading and mismatch conditions among the series-connected modules/sub-modules suffer from a nonconvex power curve with multiple local maxima and decreased peak power for the whole string. Energy transfer between the sub-modules brings them to the same operating voltage, and this collective operation produces a convex power curve, which results in increased peak power for the string. The proposed topology benefits from the switched-capacitor (SC) converter concept and is an application for sub-module-level power balancing with some novelties, including stopping the switching in absence of shading, string-level extension, and a reduced number of power electronics components as compared to those in the literature. Reduction in the number of power electronics components is realized by the fact that two sub-modules share one SC converter. This leads to reduced power electronics losses as well as less cost and volume of the converter circuit. Insertion loss analysis of the topology is presented. The proposed topology is simulated in the PSpice environment, and a prototype is built for experimental verification. Both simulation and experimental results confirm the loss analysis. This proves that with the proposed topology it is possible to extract almost all the power available on the partially shaded string and transfer it to the load side.

Key words: Sub-module-level maximum power point tracking (MPPT), Differential power processing (DPP), Distributed power converters, Switched-capacitor (SC) converters

http://dx.doi.org/10.1631/FITEE.1500322 **CLC number:** TM914; TM40

1 Introduction

Since high-voltage inverters have high efficiency, photovoltaic (PV) modules are connected in series to obtain high voltages (Kerekes, 2009). Recent research efforts and technological developments chronologically introduced us to central inverters, string inverters, string inverters with multiple inputs, multilevel inverters, micro-inverters for each PV module, DC-DC optimizers at the module and sub-module (SM) levels, and cell-level maximum power point tracking (MPPT) using diffusion charge redistribution (DCR). DCR, proposed by Chang and Leeb (2014) and Chang *et al*. (2014; 2015), can be used in 'future smart PV modules'. The idea of each approach has arisen as a solution to partial shading and the mismatch losses with increased granularity (Gokdag and Akbaba, 2014). Partial shading and mismatch conditions among the series-connected modules/sub-modules/cells suffer from a nonconvex output power characteristic curve with multiple local maxima and decreased peak power for the whole string/module, including bypass diodes. This limits the power extraction from the whole string/module (Giral *et al*., 2010).

* Project supported by the BAP Department of Karabuk University, Turkey (No. KBU-BAP-13/2-DR-010)

ORCID: Mustafa GOKDAG, http://orcid.org/0000-0001-5589-2278

Bypass diodes are connected in parallel with the SMs to bypass the SMs subjected to partial shading and prevent them from acting as a load to the unshaded modules. When the bypass diodes are activated because of shading, the power produced by the bypassed SMs is wasted. Consequently, recent studies have concentrated on regaining the bypassed power through the use of bypass diodes and bringing them to the same operating voltage (Giral *et al*., 2010). Pilawa-Podgurski and Perreault (2013), taking the advantage of the distributed power electronics concept, proposed a synchronous buck converter that is implemented in parallel with the SM, by employing both inductive and capacitive elements and processing the whole power produced from the SM. This topology does not use differential power processing (DPP), and the overall efficiency depends highly on the converter efficiency. Subsequent studies at the SM level generally rely on a similar idea, which is to transfer energy or redistribute charge between SMs using energy storage elements like a combination of inductor-capacitor or transformer-capacitor and switches. This energy transfer brings all SMs to the same operating voltage and produces a convex output power curve with increased peak power for series-connected SMs/cells. All these studies process only the power mismatch, which is small in comparison with the string power, and result in minimum loss. If the SMs are imbalanced, they do not lose power ideally. As a result, all of the DC-DC converters, which process only the mismatch power among the SMs, are categorized in the DPP concept. In Giral *et al*. (2010), a bidirectional buck-boost circuit with current control was proposed to guarantee equal section voltages in a module using active voltage sharing. The closed-loop control needs current measurement. In Qin and Pilawa-Podgurski (2013) and Qin *et al*. (2013), a DPP converter was implemented as a synchronous buck-boost circuit with voltage measurement feedback. The control strategy was designed to allow each and every DPP converter to track the local MPP of its corresponding SM. The control strategy searches for a convenient duty cycle on a two-dimensional surface to maximize the voltage of the string for a temporarily fixed string current. The string voltage information is required by each DPP converter to realize this strategy. Therefore, this concept requires a communication interface to acquire diagnostic data. The conventional perturb-observe MPPT algorithm working on the central inverter gradually moves the string current fixed previously toward the maximum power point value in a 'slow' loop, while the local DPP controllers adjust the duty cycles to maximize the string voltage in a 'fast' loop. This control approach may fail under rapidly changing environmental conditions. Hence, the SM voltage and the string current may never converge to their optimal values. The control complexity also increases. In Kim *et al*. (2012), the PV-to-bus and PV-to-PV DPP architectures for series string were examined for mismatch conditions using Monte Carlo simulation and compared with series strings with and without bypass diodes. The authors stated that the flyback topology can be employed in the PV-to-bus converter and that the buck-boost topology can be employed in the PV-to-PV converter. Their simulation results showed better performance for the PV-to-bus architecture. However, the switches used in PV-to-bus converters must be rated to the bus voltage, and this results in some disadvantages in application. In Shenoy *et al*. (2012a; 2013), a local control strategy requiring current and voltage measurements was developed for the bidirectional buck-boost converter, which was employed as a DPP in the PV-to-PV architecture proposed by Kim *et al*. (2012). A basic perturb-and-observe algorithm running on the local controller tries to maximize the power of each PV element to find the corresponding duty cycle. The converter efficiency was reported to be around 96%. In Shenoy *et al*. (2012b), several differential energy conversion architectures and associated local controls were analyzed. Their simulation results showed that the isolated flyback converter employed in a PV-to-bus architecture tends to process the least amount of power. In Levron *et al*. (2013; 2014), Olalla *et al*. (2013; 2014a; 2014b; 2015), and Choi *et al*. (2014), another bidirectional flyback converter that allows DPP and its control approach was analyzed. The secondary ports of the flyback transformers were connected in parallel and disconnected from the module/string output. This solves the disadvantage mentioned by Kim *et al*. (2012), brings the advantage of using low-voltage-rated switches, and results in a control without the need for additional sensing. This architecture increases the string cable usage since it uses dual-core cable at the secondary of the transformer. In

Kesarwani and Stauth (2012) and Stauth *et al*. (2012a; 2012b; 2013), resonant switched-capacitor (SC) converters were configured in a parallel-ladder architecture with strings of PV cells at the SM level to improve energy capture in the event of shading or mismatch. The balancing action extends from the SM level with one more added converter stage to the entire series string through a dual-core cable and connector. All the above studies generally use both inductive and capacitive elements and employ n or $n-1$ converters to prevent mismatch losses of n SMs, resulting in increased cost and power electronics losses.

The topology proposed in this work includes a power converter connected in parallel with PV SMs (Fig. 1), and benefits from the switched capacitor converter concept in a different manner from that of similar studies (Kesarwani and Stauth, 2012; Stauth *et al*., 2012a; 2012b; 2013). It is actually an application of the concept of Chang and Leeb (2014) and Chang *et al*. (2014; 2015) and with some novelties such as sub-module-level power balancing, stopping the switching in the absence of shading, string-level extension, and a reduced number of power electronics components compared to the concepts in related studies. Reduction in the number of power electronics components is realized by the fact that two SMs share one switched capacitor converter. This leads to reduced power electronics losses, less cost, and smaller volume of the converter circuit. Insertion loss analysis of the topology is presented in Section 2. The proposed topology is simulated in PSpice environment, and a prototype is built for experimental verification. Both simulation and experimental results confirm the loss analysis given in Section 2. With the proposed topology, it is possible to extract almost all the power available on the partially shaded string and transfer it to the load side.

2 Proposed topology

In the proposed topology, the SMs, each of which is supported by a charge storage capacitor, are configured in the parallel-ladder architecture to form a string (Fig. 1). These SMs are switched with each other to bring all SMs to the same operating voltage. The control of the converter is very simple and the SMs and associated capacitors are switched

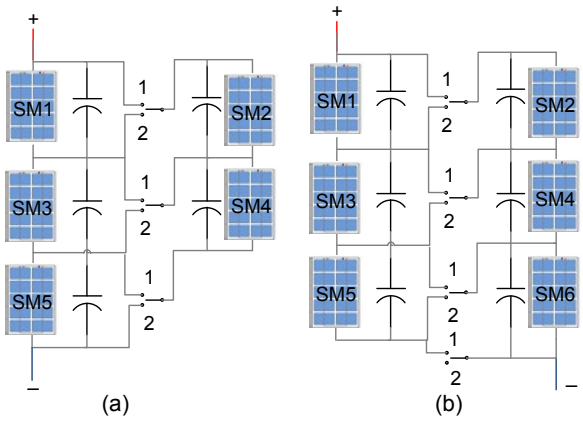


Fig. 1 Proposed ladder-connected sub-modules (SMs) topology that requires continuous switching (a) and allows stopping the switching process (b)

periodically between two states. The proposed topology requires n capacitors and $n+1$ switches for n SMs, while the resonant SC converter proposed by Kesarwani and Stauth (2012) and Stauth *et al*. (2012a; 2012b; 2013) requires $2n-1$ capacitors and $2n$ switches.

A single output version of this topology shown in Fig. 1a requires continuous switching. This causes an insertion loss even if there is no partial shading and mismatch among the SMs, because the power generated by the switched-ladder string shown in the right-hand side of Fig. 1a must be processed to be transferred to the load side. Hence, the whole power produced by the switched ladder string is lost when switching is stopped (Chang and Leeb, 2014; Gokdag and Akbaba, 2014). The topology shown in Fig. 1b allows stopping the switching process with the switches in position '1' when partial shading is not present, resulting in reduced insertion loss. In this case, the insertion loss is present only because of the on-state resistances of the uppermost and the lowermost switches of the string which carry the string current of the series SMs on the right-hand side of Fig. 1b. The approach can be extended to the string level by placing the SC converter into the junction box of the PV module (Fig. 2). Dual-core cables are used to connect PV modules in series.

The SC loss analysis presented in Chang *et al*. (2014) and Seeman and Sanders (2006) can be adopted for the topology shown in Fig. 1b. The SC conversion loss introduces two asymptotic limits on the output impedance, which are the slow and fast switching limits.

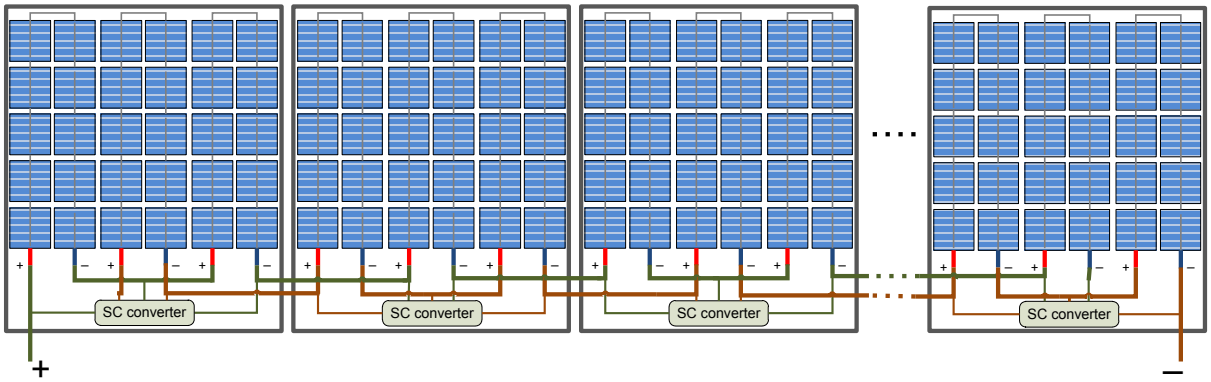


Fig. 2 String level extension of the proposed topology (references to color refer to the online version of this figure)

In calculation of the output impedance of the switching converter due to the slow switching limit (SSL), all the switches and all the other conductive interconnects are assumed to be ideal. It is also assumed that the capacitors experience impulsive currents. In the fast switching limit (FSL) condition, it is assumed that the capacitor voltages remain constant, and the resistive sources from switches and other interconnects dominate the losses. The loss analysis for the topology shown in Fig. 1b can be done by following the procedure given in Chang *et al*. (2014) and Seeman and Sanders (2006). Below, an insertion loss calculation is performed, assuming that all the SMs are matched perfectly.

The SSL output impedance (R_{SSL}) of the switched SM string is obtained as given in Eq. (1):

$$R_{\mathrm{SSL}}=\sum_{i=1}^{2N}\frac{\alpha_{\mathrm{c},i}^2}{Cf_{\mathrm{sw}}}=\frac{1}{32N^2Cf_{\mathrm{sw}}}\sum_{i=1}^{N}(2i-1)^2, \quad (1)$$

where $\alpha_{\mathrm{c},i}$ is the charge multiplier of the ith capacitor, which represents the normalized volume of charge flow into the capacitor with respect to the output charge flow, C is the capacitance connected in parallel to the SM, f_{sw} is the switching frequency, and N is the number of SMs connected in one arm of the proposed topology shown in Fig. 1b. The percentage insertion loss is calculated as the ratio between the SSL output impedance and the load resistance. The load resistance (R_{L}) is obtained as given in Eq. (2):

$$R_{\mathrm{L}}=\frac{V_{\mathrm{out}}}{I_{\mathrm{out}}}=\frac{V_{\mathrm{MP}}\left(\dfrac{2N+1}{2}\right)}{I_{\mathrm{MP}}\left(\dfrac{4N}{2N+1}\right)}=\frac{V_{\mathrm{MP}}}{I_{\mathrm{MP}}}\frac{(2N+1)^2}{8N}, \quad (2)$$

where I_{MP} and V_{MP} are the maximum power current and maximum power voltage of the SM, respectively. The percentage insertion loss for SSL ($\mathrm{IL}_{\mathrm{SSL}}$) is obtained as given in Eq. (3):

$$\mathrm{IL}_{\mathrm{SSL}}=\frac{R_{\mathrm{SSL}}}{R_{\mathrm{L}}}=\frac{I_{\mathrm{MP}}}{4NV_{\mathrm{MP}}Cf_{\mathrm{sw}}(2N+1)^2}\sum_{i=1}^{N}(2i-1)^2. \quad (3)$$

The expression for the FSL output impedance (R_{FSL}) of the switched SM string is obtained as given in Eq. (4):

$$R_{\mathrm{FSL}}=2\sum_{i=1}^{2N+1}R_{\mathrm{eff}}\alpha_{\mathrm{sw},i}^2=R_{\mathrm{eff}}\frac{(2N-3)(2N+1)}{4N^2}, \quad (4)$$

where $\alpha_{\mathrm{sw},i}$ is the charge multiplier of the ith switch, representing the normalized charge flow through the on-state switch with respect to the output charge flow, and R_{eff} is the effective resistance of the switch on-resistance in series with any interconnect resistance. The percentage insertion loss for FSL ($\mathrm{IL}_{\mathrm{FSL}}$) is obtained as given in Eq. (5):

$$\mathrm{IL}_{\mathrm{FSL}}=\frac{R_{\mathrm{FSL}}}{R_{\mathrm{L}}}=\frac{2R_{\mathrm{eff}}I_{\mathrm{MP}}(2N-3)}{V_{\mathrm{MP}}N\ (2N+1)}. \quad (5)$$

As an example, for a switched SM string, suppose N=3, V_{MP}=11.2 V and I_{MP}=4.66 A (under standard test conditions), C=20 μF, f_{sw}=250 kHz, and R_{eff}=10 mΩ. The SSL and FSL insertion losses are calculated as 0.50% and 0.12% of the total string power, respectively. The total insertion loss ($\mathrm{IL}_{\mathrm{TOT}}$) is calculated by using Eq. (6). For the aforementioned

parameters, it is calculated as 0.51% of the total power.

$$\mathrm{IL}_{\mathrm{TOT}} = \sqrt{\mathrm{IL}_{\mathrm{SSL}}^2 + \mathrm{IL}_{\mathrm{FSL}}^2}\,. \tag{6}$$

3 Simulation results

The subsequent simulations are performed by using PSpice. A 24-cell PV SM is simulated by using the single diode model with the parallel and series resistances. The SM with the following parameters is used in the simulation: V_{MP}=11.2 V, I_{MP}=4.66 A (under standard test conditions), parallel resistance of 75.36 Ω, series resistance of 0.326 Ω, C=20 μF, and f_{sw}=250 kHz, and R_{eff}=10 mΩ is used in the switched SM converter circuit. An example string with 6 SMs which are configured in a 3//3 ladder-type configuration is simulated to show that the proposed arbitrarily N//N configured topology can be used to obtain the convex power curve with increased peak power in the partial-shading conditions and the results obtained from this simulation have proved the loss analysis given in Section 2. The general scheme about the PSpice diagram used in the simulations is shown in Fig. 3.

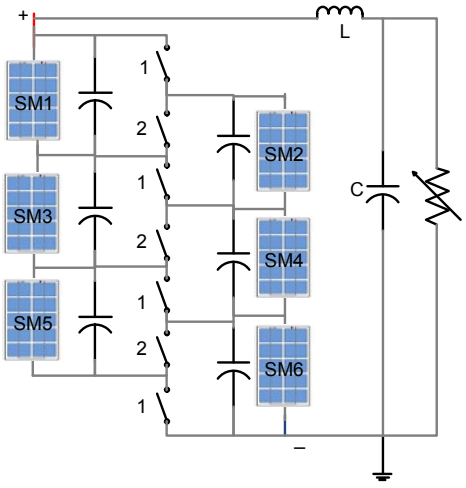


Fig. 3 General scheme about the PSpice diagram used in the simulations (SM: sub-module)

Fig. 4 shows the output power versus output voltage (P-V) curves under uniform irradiation for three different cases: (1) 6-series string, (2) 3//3 switched SM string during continuous switching, and (3) 3//3 string for switching stopped in position 1. Fig. 5 shows the P-V curves for the condition with 2 SMs 50% partially shaded (i.e., 16% overall shading). As shown in Fig. 5, the P-V curve for the series string with by-pass diode includes multiple local maximum points with decreased peak power. In this case, the MPPT algorithm working on the string inverter must be able to find the global maximum without hanging on the local maximum or minimum. The traditional hill-climbing based MPPT algorithm fail under the situation of multiple local maxima. The P-V curve for a 3//3 switched SM string is a convex curve with increased peak power as compared to the result of the series string with/without by-pass diodes. Further to this procedure, a traditional hill-climbing MPPT algorithm can easily find the maximum power point and extract more power, since the P-V curve for the switched SM string is always convex.

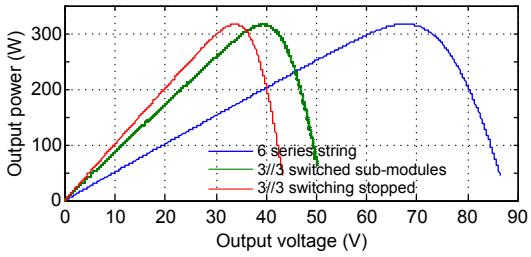


Fig. 4 Comparisons of power versus output voltage (P-V) curves for uniform irradiation conditions (references to color refer to the online version of this figure)

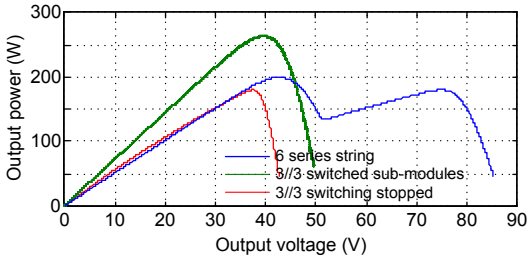


Fig. 5 Comparisons of power versus output voltage (P-V) curves for partially shaded condition (references to color refer to the online version of this figure)

The results listed in Table 1 show the maximum powers and efficiencies. In case of uniform irradiation, 99.48% conversion efficiency (CE) is obtained for the switched SM converter and this proves the loss analysis in Section 2 with a small loss of 0.51% of the total string power. An extracted power efficiency (EPE) of 83.49% in case of 16% overall shading proves that the proposed topology can extract nearly all the power available on the string. Under the

uniform irradiation condition, the switches are stopped in position 1 to prevent insertion loss. The CE in this case is obtained as 99.84%. A small loss of 0.16% is due to the on-state resistances of the uppermost and the lowermost switches of the string, which carry the string current of the series SMs on the right-hand side in Fig. 3. Thus, one may conclude that this loss will be almost constant and the ratio between this loss and the total string power will be negligible as the string size gets larger.

Table 1 Comparison for maximum powers and efficiencies in simulations

Configuration	Maximum power (W)		CE (%)	EPE (%)
	UR	16% OS		
6 series+by-pass	318.06	199.47	100	62.71
3//3 sw stopped	317.55	179.98	99.84	56.67
3//3 sw sub-module	316.41	264.18	99.48	83.49

UR: uniform radiation; OS: overall shading; CE: conversion efficiency; EPE: extracted power efficiency

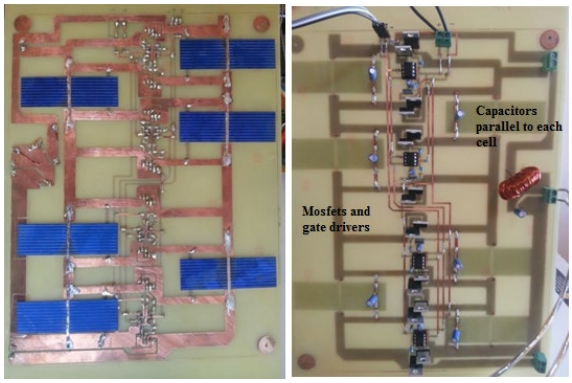
4 Experimental results

An experimental prototype to test the proposed topology is shown in Fig. 6. In this prototype, a 3//3 switched SM string, which has a nominal power of 1.35 W under standard test conditions, is established. Each SM is represented by a solar cell which has maximum power point voltage of 0.366 V and current of 0.454 A for the experiment conditions, and is supported by a 10 μF charge storage capacitor. MOSFETs with a 30 mΩ on-state resistance are used in the circuit as switches. The switching frequency f_{sw} is 200 kHz. For these parameters, the SSL and FSL insertion losses are calculated as 3.69% and 1.06% of the total string power, respectively. The total insertion loss of these two components is 3.84% of the total power.

A complementary PWM signal pair (Fig. 7) is generated by a PIC18F4431 microcontroller and is applied to the MOSFETs' gate driver inputs. A dead time of 130 ns is inserted between the PWM signal pair to prevent short circuits on the capacitances.

The prototype is tested under clear sky conditions to obtain repeatable experimental results for small time intervals. A multi-turn precision potentiometer of 50 Ω is used as a variable load to obtain the output current and output voltage (I-V) characteristics of the string from the short circuit point to the open circuit point. The current-voltage data pair is read and recorded from the oscilloscope while changing the resistance of the potentiometer from 0 Ω to 50 Ω. A picture of the experimental setup is shown in Fig. 8.

The experimental results are obtained for the 'normal string' and the proposed switching topology to compare power-voltage characteristics under uniform radiation and partially shaded conditions. The term 'normal string' means that the switching process



(a) (b)

Fig. 6 Experimental prototype: (a) front surface; (b) rear surface

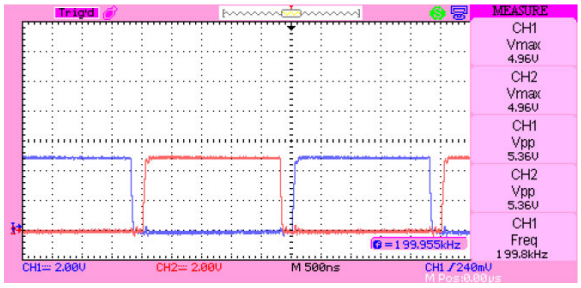


Fig. 7 PWM signal pair with dead time insertion

Fig. 8 A picture of the experimental setup

is stopped and the switches are left in position 1. So, a string with two-parallel arms is considered as a normal string. Fig. 9 shows the results obtained under uniform radiation with no partial shading, whereas Fig. 10 shows the results for the case in which both SMs in the middle of the two arms are approximately 75% shaded artificially, and the overall shading for the whole string is about 25%. Fig. 11 shows the results with the SMs in the middle approximately 35% shaded and about 12% overall shading.

The results listed in Table 2 show the maximum powers and efficiencies. A 96.9% conversion efficiency for the switched SM converter approximately matches the result of the loss analysis with a loss of 3.84%. The extracted power of 74.6% in case of 25% overall shading proves that the proposed topology can be used to extract almost all the power available on the string.

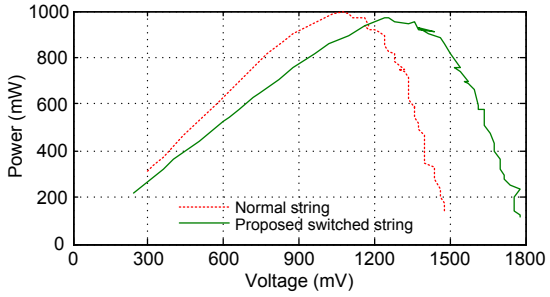


Fig. 9 Experimental results of P-V curves for uniform radiation conditions

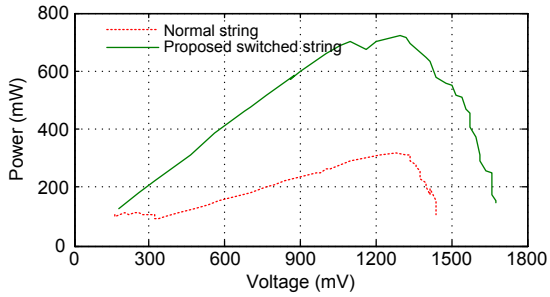


Fig. 10 Experimental results of P-V curves for two sub-modules approximately 75% shaded (25% overall shading)

5 Conclusions

In this paper, we present a new sub-module (SM) level power balancing topology to obtain a convex power curve with increased peak power under partial shading conditions. An array composed of two-arm switched strings was configured in an *N*//*N* parallel-ladder architecture. The switching process between the SMs enables the array to act as a single ideal PV module. This eliminates the need for a string inverter with multiple independent MPPT inputs and requires only a single input string inverter with an LC filter. The parallel-ladder configuration of the SMs requires n capacitors and n+1 switches for the power balancing of n SMs, while the switched capacitor topology proposed by Kesarwani and Stauth (2012) and Stauth *et al*. (2012a; 2012b; 2013) requires $2n-1$ capacitors and $2n$ switches. This advantage results in reduced power electronics losses, less cost, and a smaller size of the converter circuit. The configuration also increases the power balancing capability between the SMs since each capacitor is supported by a PV element for the two positions of the switches, whereas in the earlier similar counterparts the capacitor was supported by the PV element for one position of the switch. The string level application is possible with the proposed topology. The SSL and FSL loss mechanism expressions for an *N*//*N* arbitrarily sized string were obtained to calculate the total insertion loss associated with the switched capacitor converter. For the uniform radiation condition, the topology allows stopping the switching in absence of shading,

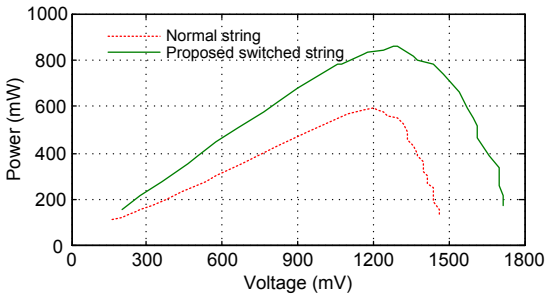


Fig. 11 Experimental results of P-V curves for two sub-modules approximately 35% shaded (12% overall shading)

Table 2 Experimental results for maximum powers and efficiencies

Configuration	Power (mW)			CE	EPE	
	UR	25% OS	12% OS		25% OS	12% OS
Normal string	999	320	593	100%	32.0%	59.4%
3//3 sw string	969	723	856	96.9%	74.6%	88.3%

UR: uniform radiation; OS: overall shading; CE: conversion efficiency; EPE: extracted power efficiency

which decreases the insertion loss to a negligible level in comparison to the total string power. The proposed topology was simulated in PSpice and tested on a prototype. The results proved that, with the proposed topology, it is possible to extract almost all the power available on the partially shaded string and transfer it to the load side. The design and test of the miniature sized switched capacitor DC-DC converter at the 'true sub-module level', which can be placed into the junction box of the PV module, and the dual output version of the proposed topology, which allows differential power processing, are left for future studies.

References

Chang, A.H., Leeb, S.B., 2014. Differential diffusion charge redistribution for photovoltaic cell-level power balancing. Int. Conf. on Renewable Energy Research and Application, p.576-582. http://dx.doi.org/10.1109/ICRERA.2014.7016450

Chang, A.H., Avestruz, A.T., Leeb, S.B., 2014. Capacitor-less photovoltaic (PV) cell-level power balancing using diffusion charge redistribution. 29th Annual IEEE Applied Power Electronics Conf. and Exposition, p.712-720. http://dx.doi.org/10.1109/APEC.2014.6803386

Chang, A.H., Avestruz, A.T., Leeb, S.B., 2015. Capacitor-less photovoltaic cell-level power balancing using diffusion charge redistribution. *IEEE Trans. Power Electron.*, **30**(2):537-546. http://dx.doi.org/10.1109/TPEL.2014.2340403

Choi, B., Clement, D., Maksimovic, D., 2014. A CMOS controller for submodule integrated converters in photovoltaic systems. IEEE 15th Workshop on Control and Modeling for Power Electronics, p.1-6. http://dx.doi.org/10.1109/COMPEL.2014.6877133

Giral, R., Ramos-Paja, C.A., Gonzalez, D., *et al*., 2010. Minimizing the effects of shadowing in a PV module by means of active voltage sharing. IEEE Int. Conf. on Industrial Technology, p.943-948. http://dx.doi.org/10.1109/ICIT.2010.5472551

Gokdag, M., Akbaba, M., 2014. Symmetric ladder connection design using diffusion charge redistribution for solar cell-level MPPT with reduced insertion loss. SOLARTR Conf. & Exhibition, p.720-726.

Kerekes, T., 2009. Analysis and Modeling of Transformerless Photovoltaic Inverter Systems. PhD Thesis, Aalborg University, Denmark.

Kesarwani, K., Stauth, J.T., 2012. A comparative theoretical analysis of distributed ladder converters for sub-module PV energy optimization. IEEE 13th Workshop on Control and Modeling for Power Electronics, p.1-6. http://dx.doi.org/10.1109/COMPEL.2012.6251780

Kim, K.A., Shenoy, P.S., Krein, P.T., 2012. Photovoltaic differential power converter trade-offs as a consequence of panel variation. IEEE 13th Workshop on Control and Modeling for Power Electronics, p.1-7. http://dx.doi.org/10.1109/COMPEL.2012.6251789

Levron, Y., Clement, D., Maksimovic, D., *et al*., 2013. Nonlinear control design for the photovoltaic isolated-port architecture with submodule integrated converters. IEEE Energy Conversion Congress and Exposition, p.2398-2405. http://dx.doi.org/10.1109/ECCE.2013.6647008

Levron, Y., Clement, D., Choi, B., *et al*., 2014. Control of submodule integrated converters in the isolated-port differential power-processing photovoltaic architecture. *IEEE J. Emerg. Sel. Top. Power Electron.*, **2**(4):821-832. http://dx.doi.org/10.1109/JESTPE.2014.2326972

Olalla, C., Clement, D., Choi, B.S., *et al*., 2013. A branch and bound algorithm for high-granularity PV simulations with power limited SubMICs. IEEE 14th Workshop on Control and Modeling for Power Electronics, p.1-6. http://dx.doi.org/10.1109/COMPEL.2013.6626429

Olalla, C., Deline, C., Maksimovic, D., 2014a. Performance of mismatched PV systems with submodule integrated converters. *IEEE J. Photovolt.*, **4**(1):396-404. http://dx.doi.org/10.1109/JPHOTOV.2013.2281878

Olalla, C., Deline, C., Maksimovic, D., 2014b. Modeling and simulation of conventionally wired photovoltaic systems based on differential power processing SubMIC-enhanced PV modules. IEEE 15th Workshop on Control and Modeling for Power Electronics, p.1-9. http://dx.doi.org/10.1109/COMPEL.2014.6877127

Olalla, C., Deline, C., Clement, D., *et al*., 2015. Performance of power-limited differential power processing architectures in mismatched PV systems. *IEEE Trans. Power Electron.*, **30**(2):618-631. http://dx.doi.org/10.1109/TPEL.2014.2312980

Pilawa-Podgurski, R.C.N., Perreault, D.J., 2013. Submodule integrated distributed maximum power point tracking for solar photovoltaic applications. *IEEE Trans. Power Electron.*, **28**(6):2957-2967. http://dx.doi.org/10.1109/TPEL.2012.2220861

Qin, S.B., Pilawa-Podgurski, R.C.N., 2013. Sub-module differential power processing for photovoltaic applications. 28th Annual IEEE Applied Power Electronics Conf. and Exposition, p.101-108. http://dx.doi.org/10.1109/APEC.2013.6520193

Qin, S.B., Cady, S.T., Domínguez-García, A.D., *et al*., 2013. A distributed approach to MPPT for PV sub-module differential power processing. IEEE Energy Conversion Congress and Exposition, p.2778-2785. http://dx.doi.org/10.1109/ECCE.2013.6647061

Seeman, M.D., Sanders, S.R., 2006. Analysis and optimization of switched-capacitor DC-DC converters. IEEE Workshops on Computers in Power Electronics, p.216-224. http://dx.doi.org/10.1109/COMPEL.2006.305678

Shenoy, P.S., Johnson, B., Krein, P.T., 2012a. Differential power processing architecture for increased energy production and reliability of photovoltaic systems. 27th Annual IEEE Applied Power Electronics Conf. and Exposition, p.1987-1994. http://dx.doi.org/10.1109/APEC.2012.6166095

Shenoy, P.S., Kim, K.A., Krein, P.T., 2012b. Comparative analysis of differential power conversion architectures and controls for solar photovoltaics. IEEE 13th Workshop on Control and Modeling for Power Electronics, p.1-7. http://dx.doi.org/10.1109/COMPEL.2012.6251782

Shenoy, P.S., Kim, K.A., Johnson, B.B., *et al*., 2013. Differential power processing for increased energy production and reliability of photovoltaic systems. *IEEE Trans. Power Electron.*, **28**(6):2968-2979. http://dx.doi.org/10.1109/TPEL.2012.2211082

Stauth, J.T., Kesarwani, K., Schaef, C., 2012a. A distributed photovoltaic energy optimization system based on a sub-module resonant switched-capacitor implementation. 15th Int. Power Electronics and Motion Control Conf., p.1-6. http://dx.doi.org/10.1109/EPEPEMC.2012.6397417

Stauth, J.T., Seeman, M.D., Kesarwani, K., 2012b. A resonant switched-capacitor IC and embedded system for sub-module photovoltaic power management. *IEEE J. Solid-State Circ.*, **47(**12):3043-3054. http://dx.doi.org/10.1109/JSSC.2012.2225731

Stauth, J.T., Seeman, M.D., Kesarwani, K., 2013. Resonant switched-capacitor converters for sub-module distributed photovoltaic power management. *IEEE Trans. Power Electron.*, **28(**3):1189-1198. http://dx.doi.org/10.1109/TPEL.2012.2206056