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A novel ternary half adder and multiplier based on carbon nanotube field effect transistors

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Abstract: A lot of research has been done on multiple-valued logic (MVL) such as ternary logic in these years. MVL reduces the number of necessary operations and also decreases the chip area that would be used. Carbon nanotube field effect transistors (CNTFETs) are considered a viable alternative for silicon transistors (MOSFETs). Combining carbon nanotube transistors and MVL can produce a unique design that is faster and more flexible. In this paper, we design a new half adder and a new multiplier by nanotechnology using a ternary logic, which decreases the power consumption and chip surface and raises the speed. The presented design is simulated using CNTFET of Stanford University and HSPICE software, and the results are compared with those of other studies.

Key words: CNTFET-based design; Ternary; Half adder; Multiplier; Multiple-valued logic (MVL)
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1 Introduction

Moore (1965) predicted that the number of transistors on a chip would be duplicated every two years, but the reduction of transistor dimensions in CMOS technology due to limitations such as consuming power, reliability, production costs, and the transistor size will be ended very soon. Carbon nanotube transistors are good substitutes for complex circuits based on silicon transistors. Carbon nanotubes, which are made of carbon plates with one atom diameter and as an empty cylinder, were detected in 1991 by Ijima from the NEC Company (Iijima, 1991). CNTFETs are very worthy because of their special mechanical and electronic properties. Circuits designed based on carbon nanotube field effect transistors (CNTFETs) consume less power and are much faster than conventional silicon FET-based circuits. Moreover, the existence of the same motilities for n- and p-type CNTFETs makes the transistor sizing of complex circuits much simpler. Furthermore, CNTFETs have higher ON current than MOSFETs for the same OFF current.

Specialists have used binary logic in computational circuits for many decades. Using circuits with more than two logic levels, named multiple-valued logic (MVL) circuits, is one of the proposed methods. Recently, MVL has attracted the attention of many researchers.

MVL reduces the number of required operations for a special mathematical function and reduces the circuit area as well. Compared to the counterpart binary circuits (Lin *et al.*, 2011), using MVL one can reduce the chip area, the number of transistors, and power consumption. In CNTFET circuits, specialists can achieve different threshold voltages by controlling carbon nanotube diameters. These features can be helpful during the process of designing voltage-mode MVL circuits (Raychowdhury and Roy, 2005; Keshavarzian and Navi, 2009; Azimi *et al.*, 2014).

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In this paper, we implement a ternary half adder and a ternary multiplier with CNTFETs.

2 Carbon nanotube field-effect transistor

Carbon nanotubes are composed of carbon plates with the thickness of one atom and in the form of a thin sheet of a cylindrical graphic (Haselman and Hauck, 2010). Their useful cylinders are divided into two types, multi-walled carbon nanotubes (MWCNTs) and single-walled carbon nanotubes (SWCNTs) (Martel *et al*., 1998; Sharifi *et al*., 2015).

SWCNT shows conductivity or semi-conductivity properties according to the angle of atom arrangement along the tube (Tabrizchi *et al*., 2016).

Chiral vector is determined by (n_1, n_2) indexes which indicate the direction of CNT's wrapping. If n_1=n_2 or n_1−n_2=3i (i is an integer), the carbon nanotube is metallic. Otherwise, it is semiconducting. The diameter of CNTFET (D_{CNT}) is calculated based on the following equation (Moaiyeri *et al*., 2011):

$$D_{\mathrm{CNT}}=\frac{a}{\pi}\sqrt{n_1^2+n_1n_2+n_2^2}, \tag{1}$$

where a is the distance between neighboring atoms, which is approximately 0.144 nm. The threshold voltage of CNTFET is calculated as (Moaiyeri *et al*., 2011)

$$V_{\mathrm{TH}}\approx\frac{0.43}{D_{\mathrm{CNT}}/\mathrm{nm}}\ \mathrm{eV}. \tag{2}$$

The transistors based on carbon nanotubes or CNTFETs were introduced as ideal substitutes for silicon transistors due to their unique features such as small size, high speed, low power consumption, and their similar function to MOSFETs (Raychowdhury and Roy, 2004).

The operational basis of CNTFETs is the same as that of silicon transistors containing a semiconductive nanotube (which acts as a guiding channel) and a connection bridge between the drain and the source. The transistor is electrostatically ON and OFF through a gate. There are three different groups of CNTFETs. The first group is called Schottky barrier (SB) transistors. SB-CNTFET conductivity is controlled based on direct tunneling as an SB on source and channel connection (Heinze *et al*., 2002). The second group is CNTFETs-like MOSFETs transistors. These transistors have unipolar behaviors and a higher comparability compared to SB-CNTFETs. They also have a much higher current due to the lack of an SB in ON mode (Javey *et al*., 2005; Alkaldy *et al*., 2014). The third group is band-to-band tunneling CNTFETs. These transistors have super cut-off characteristics and low ON currents. They are very appropriate for designing ultra-low power and sub-threshold circuit (Javey *et al*., 2005; Raychowdhury and Roy, 2007). Fig. 1 shows the structure of the transistors based on carbon nanotubes (Moaiyeri *et al*., 2011).

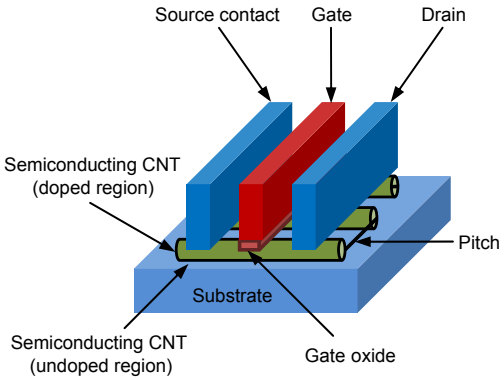

Fig. 1 Transistor structure based on CNTFET

In this study we use MOSFET-like CNTFETs to design circuits, because of their aforementioned advantages and their operational similarity to MOSFETs.

3 Review of multiple-valued logic

Traditional VLSI circuits are based on binary logic (there are only two possible values, 0 and 1). However, in recent years there have been considerable improvements in integrated circuit technology, where more than two discrete levels of signals are employed. MVL provides several potential advantages over binary circuits. In a VLSI circuit, approximately 70% of the area is devoted to interconnection, 20% to insulation, and 10% to devices (Butler, 1991). Using logic with more than two levels has been proposed as a solution to reduce these

interconnections (Etiemble and Israel, 1988). In recent decades, MVL, such as ternary logic, has been highly thought of. MVL reduces the number of necessary operations to implement a function, and reduces the chip area as well.

MVL has better characteristics compared to conventional binary logic. MVL allows more data to be transmitted on wires. It leads to high speed transfers and reduces the complexity of internal connections. Circuits will also be beneficial in terms of reduced area.

The chip area of VLSI circuits is indicated by the connections. The general area of inner connections is specified by their length. Since the length of the connections is indicated by the connection complexity, it is obvious that using MVL is very useful for implementing massive VLSI circuits.

The input values are presented by different voltage levels. Table 1 shows the ternary values.

Table 1 Logic symbols

Logic value	Voltage level
0	0
1	$V_{DD}/2$
2	V_{DD}

Ternary inverter is the basic ternary logic gate that has one input, and it can be standard ternary inverter (STI), negative ternary inverter (NTI), or positive ternary inverter (PTI):

$$\begin{aligned} &\mathrm{STI}=2-\mathrm{input},\\ &\mathrm{NTI}=\begin{cases}2, & \text{if input}=0,\\ 0, & \text{if input}\neq 0,\end{cases}\\ &\mathrm{PTI}=\begin{cases}2, & \text{if input}\neq 2,\\ 0, & \text{if input}=2.\end{cases}\end{aligned} \tag{3}$$

Table 2 shows the truth table of the ternary inverter.

Table 2 Truth table of the ternary inverter

Input	STI	NTI	PTI
0	2	2	2
1	1	0	2
2	0	0	0

4 Proposed designs

The diameters of the CNTs determine the appropriate threshold voltages (Lin *et al*., 2009; Tabrizchi *et al*., 2016). Eq. (2) indicates that in CNTFET design, the threshold voltage is inversely related to the chirality vector.

In the proposed design, the diameters of CNTs are 1.487, 1.096, and 0.783 nm, and the chirality of the CNTs would be (19, 0), (14, 0), and (10, 0), respectively. As a result, by changing the chirality vector, the threshold voltage will also change. From Eq. (2), threshold voltage values are 0.293, 0.398, and 0.557 V, respectively.

4.1 Proposed ternary half adder

Half adder is a combinational circuit that adds two ternary inputs and represents ternary Sum and Carry in output. The truth table of the ternary half adder is shown in Table 3.

Table 3 Truth table of the ternary half adder

A	*B*	Sum	Carry
0	0	0	0
0	1	1	0
0	2	2	0
1	0	1	0
1	1	2	0
1	2	0	1
2	0	2	0
2	1	0	1
2	2	1	1

Fig. 2 shows the proposed ternary half adder, which consists of transmission gates and CNT transistors to provide Sum and Carry.

In designing the Carry circuit (Fig. 2b), the diameters of T_1 and T_2 transistors are both 0.783 nm and their threshold voltages are both 0.557 V; therefore, p-type transistor (PCNTFET) is turned on with 0 and n-type transistor (NCNTFET) is turned on with 2. In both cases, 0 is transmitted to the output. Similarly, if A=0, in T_2 both transistors are ON; therefore, the output voltage will be equal to 0. The threshold voltages of T_3 and T_4 are both 0.293 V; when the input voltage of A is 0 or 1, T_3 is ON, and if A is 1 or 2, T_4 is ON. While A=1, T_3 and T_4 are ON simultaneously. In this case, if B=0 or 1, Out2 will be 0; otherwise, it will

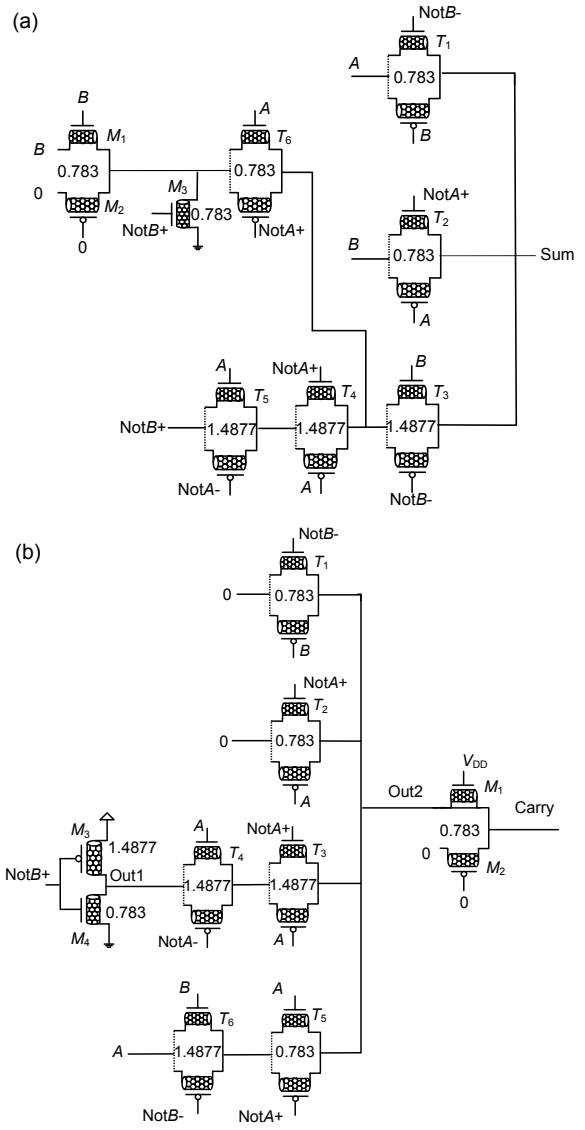

Fig. 2 Proposed CNTFET based ternary half adder: (a) Sum; (b) Carry

be 2. If A=2 and B=1 or 2, then T_5 and T_6 are ON respectively and Out2 will be logic 2 since Out2 is connected to one resistive divider between M_1 and M_2; consequently, when Out2 is equal to 2, Carry is 1.

In the Sum circuit design, when either of the inputs A and B is the logic 0, Sum will be equal to the other input by T_1 or T_2. When B input is 1 or 2, if A=1, the output will be equal to positive not B (Not$B$+) through T_3, T_4, and T_5. If A=2, T_6 is ON; if B=1 or 0, M_3 is ON. Therefore, the output reaches GND (logic 0). In this case, if B=2, M_1 and M_2 are ON and M_3 is OFF. Thus, with a resistive divider between M_1 and M_2, the output logic is equal to 1.

Simulation results and transient responses for the proposed half adder are shown in Table 4 and Fig. 3, respectively.

Table 4 Simulation results of the proposed ternary half adder

Design	Worst case delay ($\times10^{-11}$ s)	Average power (μW)	PDP ($\times10^{-16}$)
Proposed THA (CNT)	4.9691	0.76144	0.37837
Proposed THA (CMOS)	86.808	0.95131	8.2581
THA of Moaiyeri *et al.* (2011)	4.9763	4.2851	2.1324
THA of Lin *et al.* (2011)	5.9442	3.8611	2.2951
THA of Keshavarzian and Sarikhani (2014)	15.453	2.1651	3.3458
THA of Mirzaee *et al.* (2013)	70.285	14.876	104.55

4.2 Proposed ternary multiplier

Multipliers are known as the main keys of many arithmetic systems. The efficiency of the systems is evaluated mainly by the capability of their multipliers, since multipliers are generally the slowest components of a system while occupying the most space (Thapliyal and Ranganathan, 2013; Kotiyal *et al.*, 2015). The truth table of the ternary multiplier is shown in Table 5.

Fig. 4 (see p.428) shows the proposed ternary multiplier, which consists of transmission gates and CNT transistors to provide Product and Carry.

In the Product circuit design, due to the truth table, if one of the inputs is 0, the output will be equal to 0 by T_1 or T_2. When either of the inputs is logic 1, the Product will be equal to the other input; for example, when A=1, T_3 and T_4 are ON, and B is transmitted to the output. If both A and B are equal to 2, T_7 and T_8 will be ON and the Carry will be used to calculate the Product.

In designing Carry, when one of the inputs is less than logic 2, Carry will be zero. The diameters of all the transistors of transmission gates (T_1, T_2, T_3, and T_4) are 1.4877 nm and their threshold voltages are 0.293 V. When A=0 or 1, T_1 is ON and transfers 0; when B=0 or 1, T_2 is ON and passes 0. T_3 and T_4 will be ON only if A=2 and B=2, and Out1 is pulled up to 2. In the output of the design, M_1 and M_2 are always ON. When Out1=0, Carry is equal to 0; when Out1=2, Carry will be at logic 1.

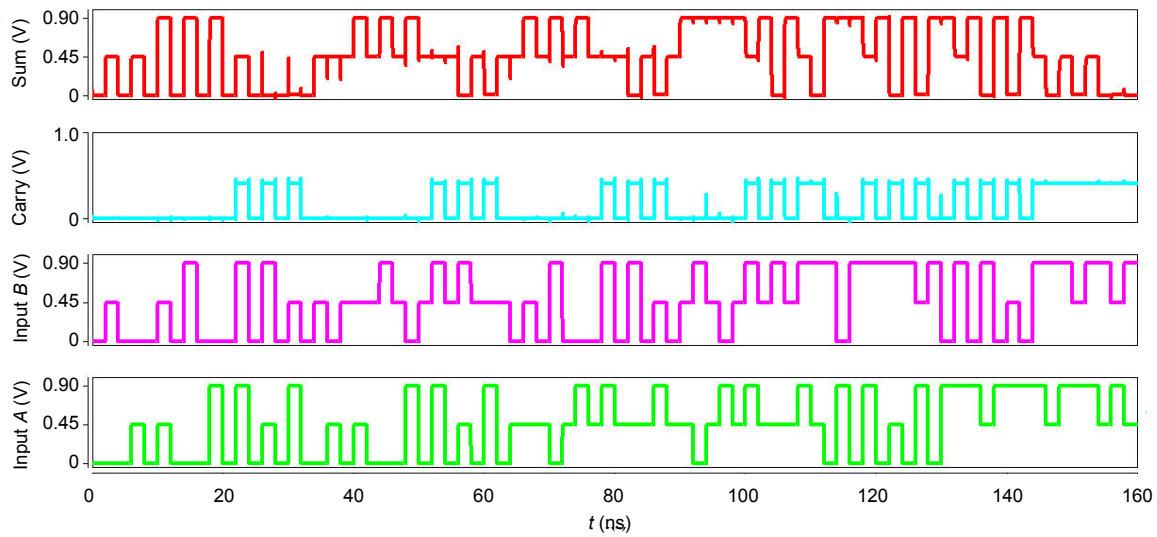

Fig. 3 Transient responses of the proposed ternary half adder

Table 5 Truth table of the ternary multiplier

A	*B*	Product	Carry
0	0	0	0
0	1	0	0
0	2	0	0
1	0	0	0
1	1	1	0
1	2	2	0
2	0	0	0
2	1	2	0
2	2	1	1

Simulation results and transient responses of the proposed ternary multiplier are shown in Table 6 and Fig. 5 (see p.429), respectively.

Table 6 Simulation results of the proposed ternary multiplier

Design	Worst case delay ($\times10^{-11}$ s)	Average power (μW)	PDP ($\times10^{-16}$)
Proposed TMUL (CNT)	9.7985	0.16515	0.16183
Proposed TMUL (CMOS)	20.576	1.0751	2.2122
TMUL of Moaiyeri *et al*. (2011)	5.8222	1.0137	0.59022
TMUL of Lin *et al*. (2011)	5.6958	2.9938	1.7052

5 Design methodology

In comparison to designing binary circuits, designing MVL circuits is more complicated and needs more transistors. In this study, designing ternary arithmetic circuits based on CNTFETs is introduced. The procedure is as follows:

In the first step, if one of the inputs is fixed and changing the other input does not influence the output, output is determined by one of the inputs.

In the next step, if one of the inputs is fixed and output is equal to the other input, the output is determined by the second input.

In these states we can implement output based on inputs directly. Therefore, we can remove this step.

Finally, the circuit is designed for the cases that have not been removed.

The advantages of this model lie in a smaller number of transistors and less power of a circuit. Note that this kind of design is very practical for CMOS transistors as shown by the aforementioned results. The disadvantages of this model are its low noise acceptance and longer delay in the case of ripple effect. By adding some buffers in every level, however, one can reduce the delay.

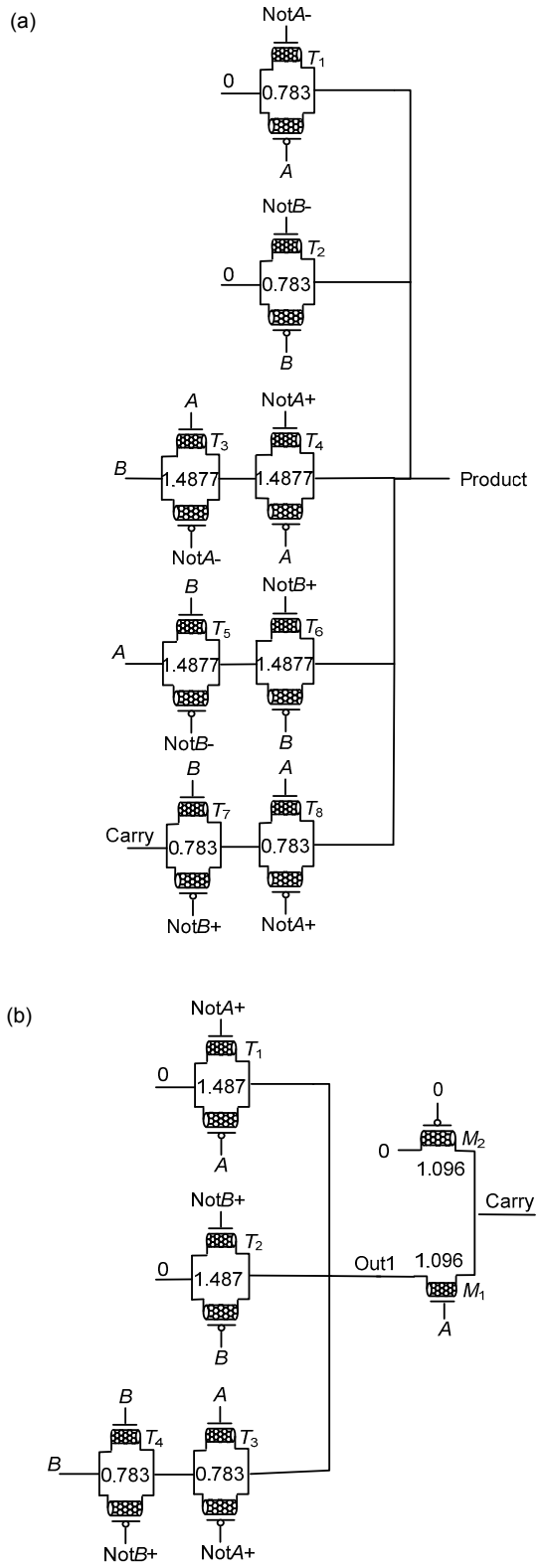

Fig. 4 Proposed CNTFET based ternary multiplier: (a) Product; (b) Carry

6 Simulation results and comparisons

In this section, the proposed structures are compared with some existing designs (Lin *et al*., 2011; Moaiyeri *et al*., 2011; Mirzaee *et al*., 2013; Keshavarzian and Sarikhani, 2014). All designs are simulated exhaustively using the Synopsys HSPICE 2008 simulator with 32 nm technology, including non-idealities (Deng and Wong, 2007a; 2007b). This standard model has been developed for unipolar, MOSFET-like CNTFET devices, in which each transistor may have one or more CNTs. In addition, this model considers these cases: SB effects, parasitic, including CNT, source/drain, gate resistances and capacitances, and also CNT charge screening. Some of the parameters of the CNTFET model used in simulations are listed in Table 7.

All designs are simulated under the same test conditions (temperature is 27 °C, load capacitor is 1 fF, V_{DD}=0.9 V, and operating frequency is 250 MHz). To compare the mentioned designs, the test bench demonstrated in Fig. 6 is used to simulate a real environment. In this test bench, a complete input pattern with all the possible transitions (Figs. 3 and 5) is fed to the circuits. The delays of all transitions from one input to another are examined and the maximum delay is reported as the delay of each circuit. Avoiding underestimation and measuring the input pattern ensure that the average power consumption is a precise reading of the power consumption of the circuit. At each simulation stage, one of these parameters changes; for example, in Figs. 7 and 8, the load capacitor and V_{DD} are constant values and temperature has been changed between 10 and 90 °C. Designs are simulated at various temperatures to evaluate their sensitivity to temperature variations. Figs. 9–12 show the simulation results with different load capacitors from 0 to 4 fF and different supply voltages from 0.8 to 1.0 V. According to the results, the proposed designs have lower power delay product (PDP) at all temperatures, supply voltages, and load capacitors compared to the other designs.

Simulation results show that at different temperatures, supply voltages, and load capacitors, the proposed circuits have better worst delay, average power, and PDP.

One of the most critical parameters in designing nanoscale circuits is process variation. Since process

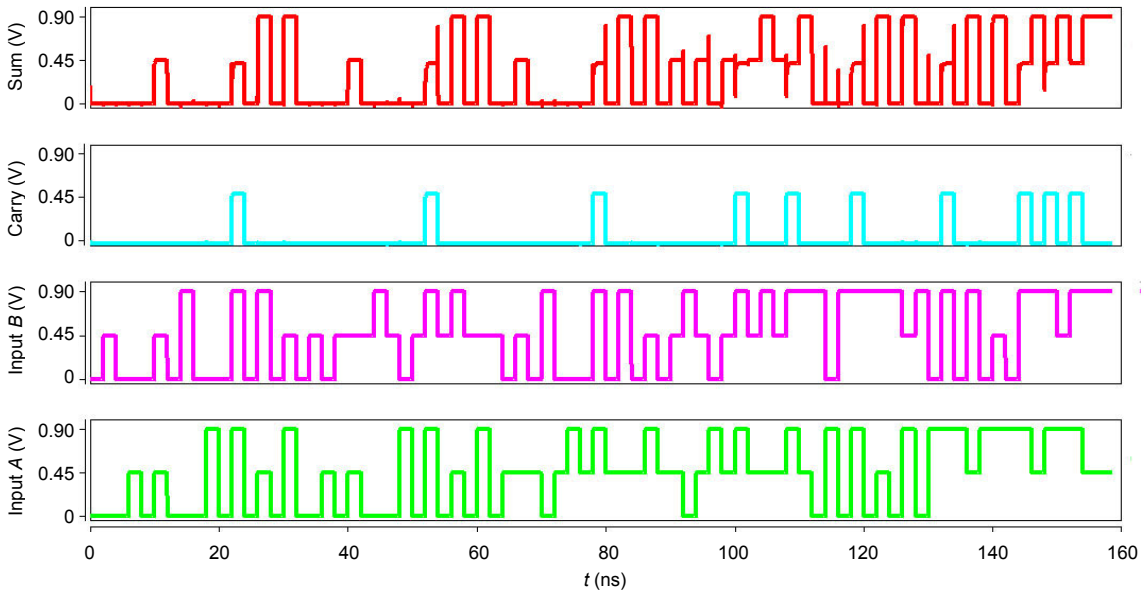

Fig. 5 Transient responses of the proposed ternary multiplier

Table 7 CNTFET model parameters

Parameter	Meaning	Value
L_{ch}	Physical channel length	32 nm
$L_{g\,eff}$	Mean free path in the intrinsic CNT channel	100 nm
L_{ss}	Length of the doped CNT source-side extension region	32 nm
L_{dd}	Length of the doped CNT drain-side extension region	32 nm
K_{gate}	Dielectric constant of high-k top gate dielectric material	16
T_{ox}	Thickness of high-k top gate dielectric material	4 nm
C_{sub}	Coupling capacitance between the channel region and the substrate	20 pF/m
EFI	Fermi level of the doped S/D tube	6 eV

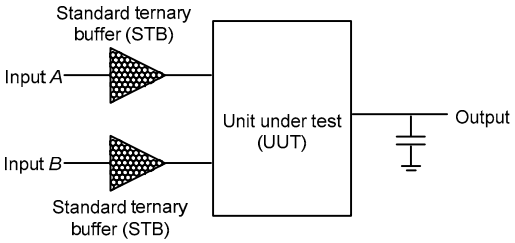

Fig. 6 Test bench circuit

variation negatively impacts some important metrics such as robustness, power consumption, and delay, it has turned into a serious challenge in designing VLSI circuits. Process variation is a result of deviations in the diameter of nanotubes and mismatches in the number of tubes. Here, Monte Carlo simulation has been conducted to estimate the process variation with ±5 to ±15 Gaussian distribution and ±σ level variation. Figs. 13–16 show the results of these simulations for the proposed ternary half adder and multiplier in terms of delay, power consumption, and PDP, respectively.

7 Conclusions

This paper has presented the ways of designing a novel ternary half adder and multiplier based on carbon nanotube field effect transistors (CNTFETs). As mentioned before, optimizing the circuit speed and its area is an extremely important issue in designing circuits. Each of the proposed ternary circuits has obtained transmission gates and CNT transistors. In all simulations the proposed design has been compared to the previous designs. Simulation results show that the proposed circuits have achieved higher speed, lower power consumption, and reduced area.

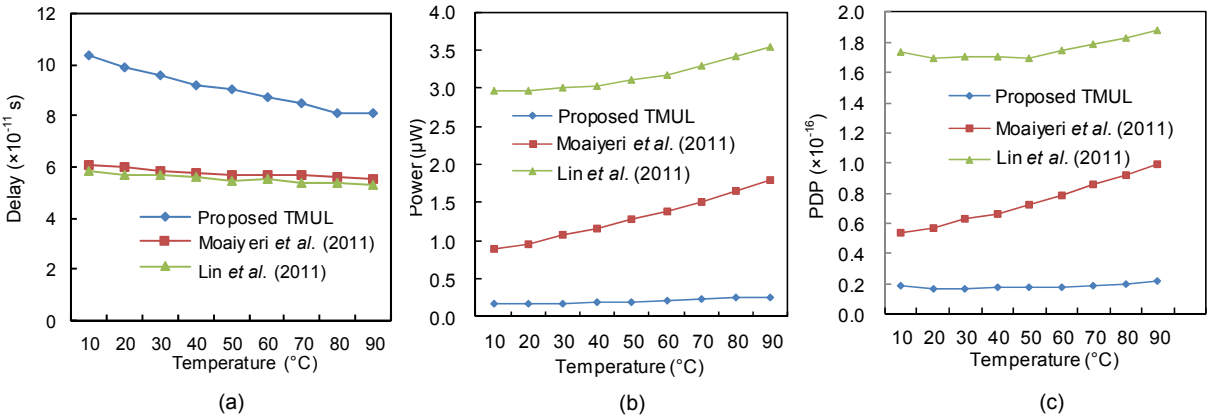

Fig. 7 Transient worst case delay (a), average power (b), and PDP (c) of the CNTFET-based ternary multiplier with different temperatures

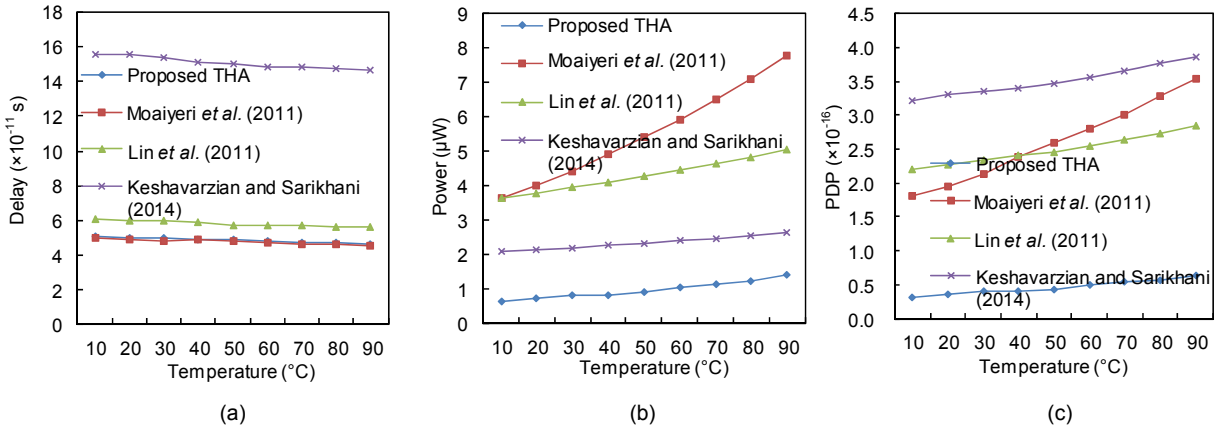

Fig. 8 Transient worst case delay (a), average power (b), and PDP (c) of the CNTFET-based ternary half adder with different temperatures

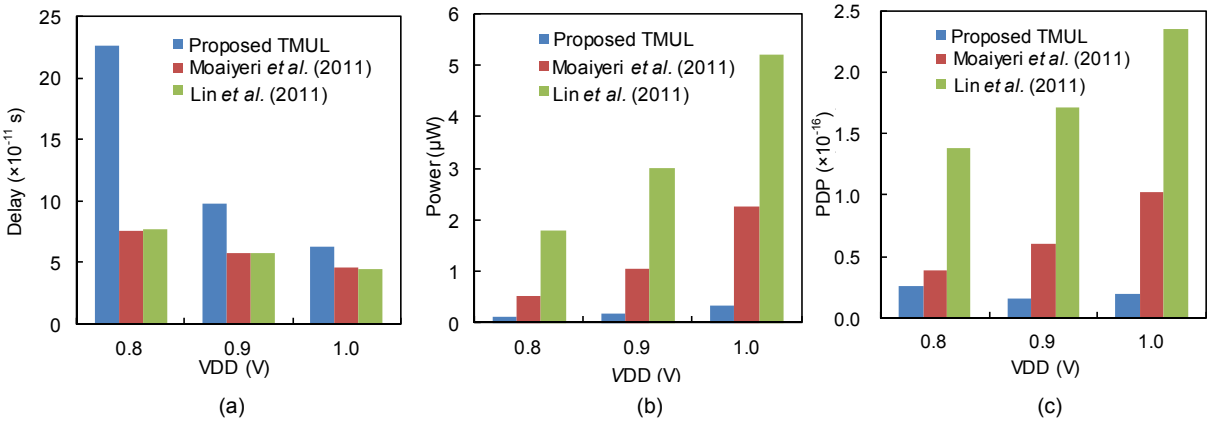

Fig. 9 Transient worst case delay (a), average power (b), and PDP (c) of the CNTFET-based ternary multiplier with different supply voltages

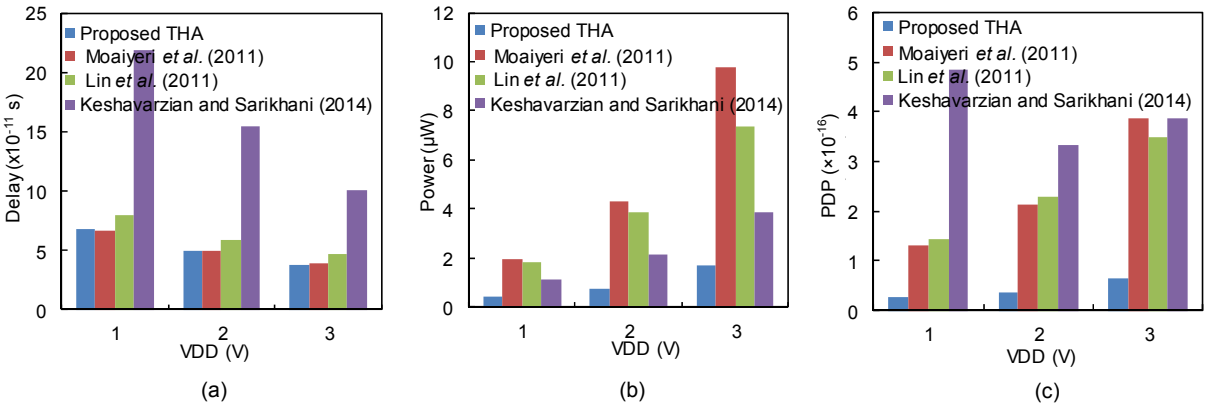

Fig. 10 Transient worst case delay (a), average power (b), and PDP (c) of the CNTFET-based ternary half adder with different supply voltages

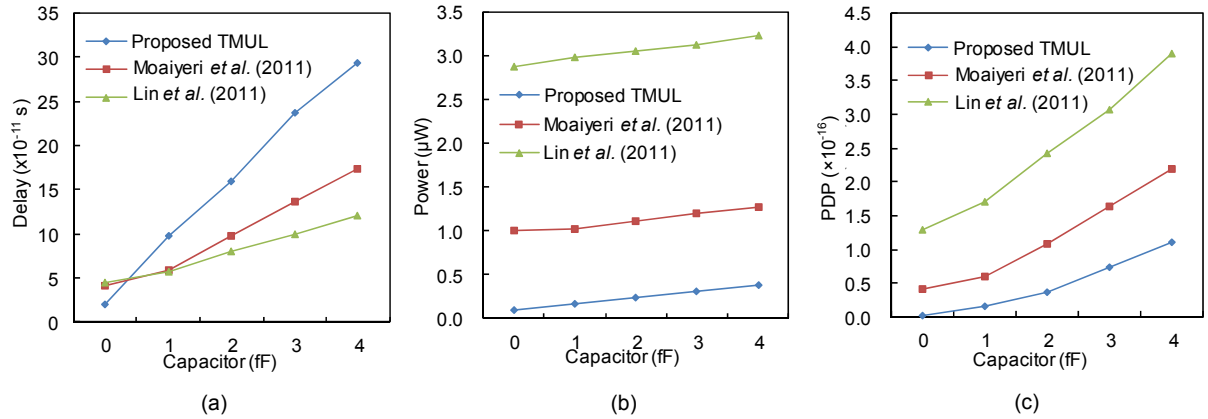

Fig. 11 Transient worst case delay (a), average power (b), and PDP (c) of the CNTFET-based ternary multiplier with different load capacitors

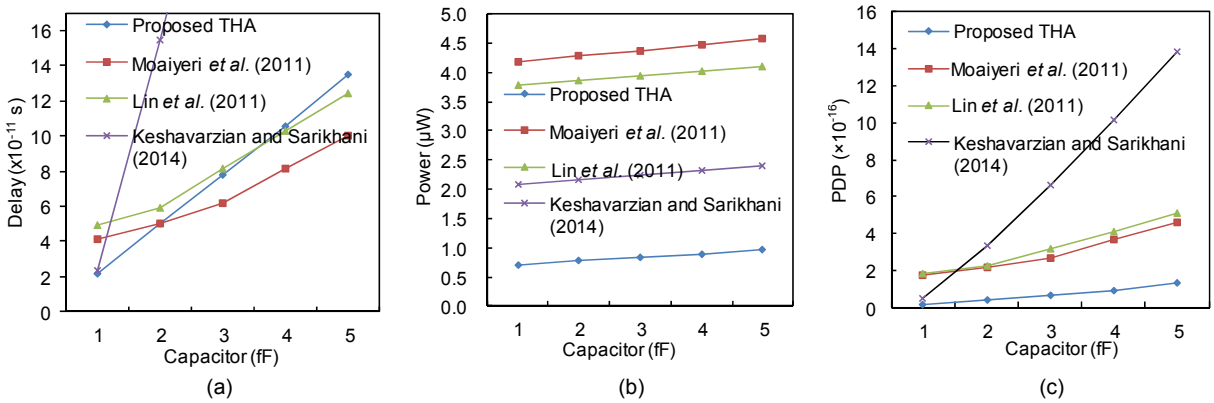

Fig. 12 Transient worst case delay (a), average power (b), and PDP (c) of the CNTFET-based ternary half adder with different load capacitors

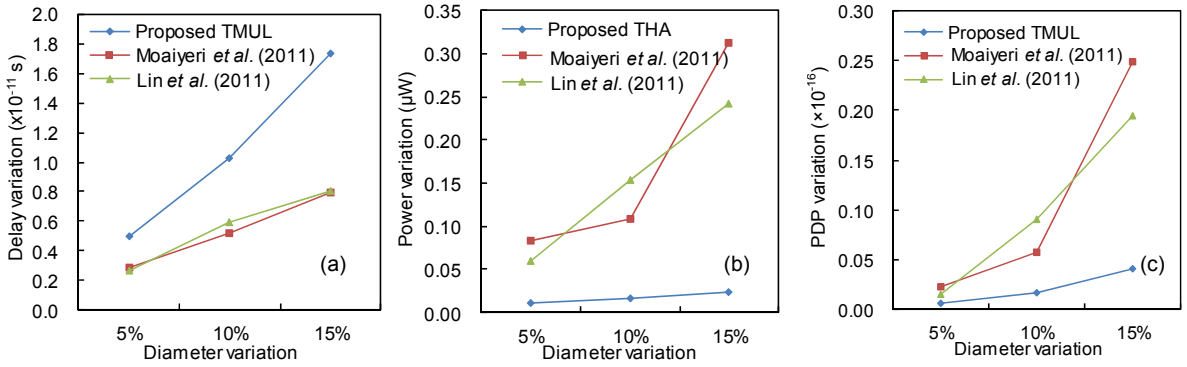

Fig. 13 Delay (a), power consumption (b), and PDP (c) of the proposed CNTFET-based ternary multiplier in terms of different diameter variations

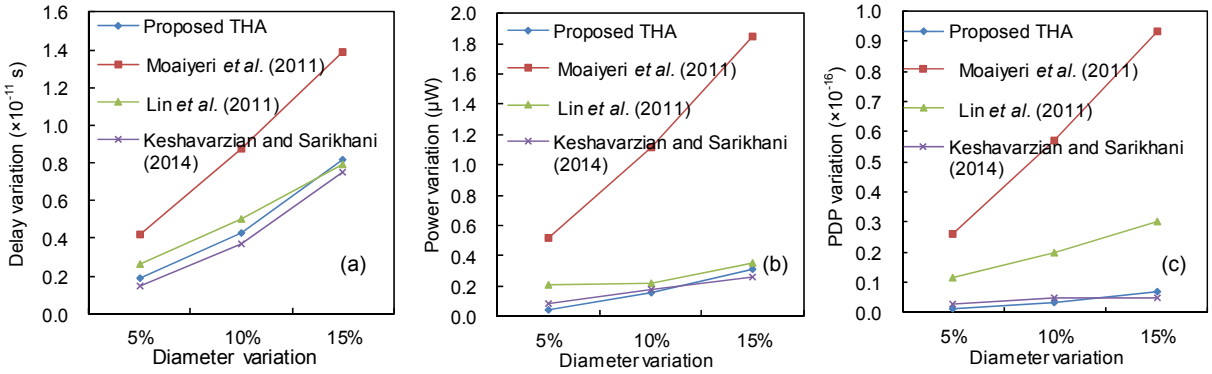

Fig. 14 Delay (a), power consumption (b), and PDP (c) of the proposed CNTFET-based ternary half adder in terms of different diameter variations

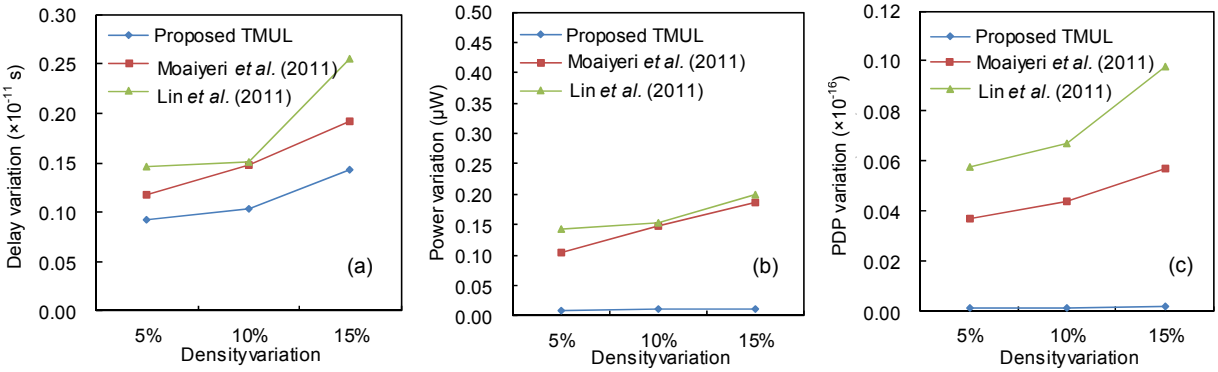

Fig. 15 Delay (a), power consumption (b), and PDP (c) of the proposed CNTFET-based ternary multiplier in terms of different density variations

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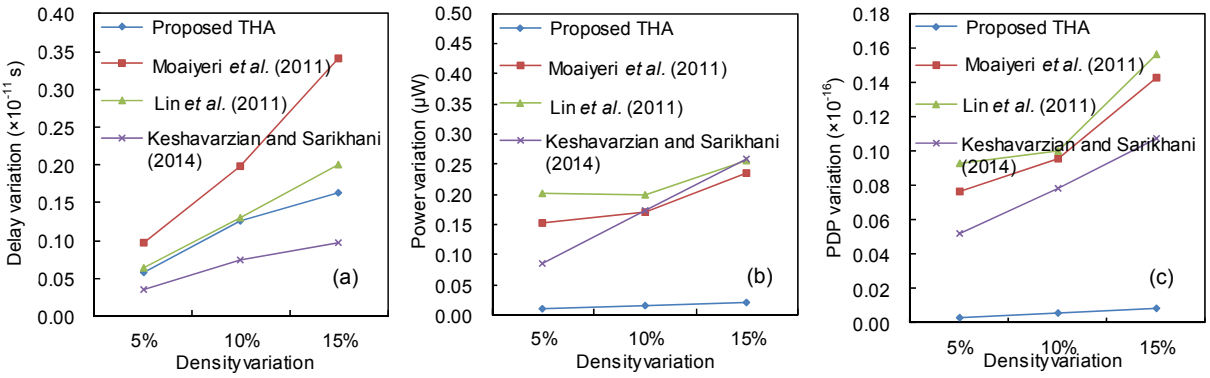

Fig. 16 Delay (a), power consumption (b), and PDP (c) of the proposed CNTFET-based ternary half adder in terms of different density variations

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