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Wide-range tracking technique for process-variation-robust clock and data recovery applications*

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Abstract: A wide-range tracking technique for clock and data recovery (CDR) circuit is presented. Compared to the traditional technique, a digital CDR controller with calibration is adopted to extend the tracking range. Because of the use of digital circuits in the design, CDR is not sensitive to process and power supply variations. To verify the technique, the whole CDR circuit is implemented using 65-nm CMOS technology. Measurements show that the tracking range of CDR is greater than $\pm 6\times10^{-3}$ at 5 Gb/s. The receiver has good jitter tolerance performance and achieves a bit error rate of $<10^{-12}$. The re-timed and re-multiplexed serial data has a root-mean-square jitter of 6.7 ps.

Key words: Clock and data recovery; Digital loop filter; Phase interpolator
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1 Introduction

With the rapid development of integrated circuit (IC) applications such as microprocessors, optical transmission links, and chip-to-chip communications, input-output (IO) bandwidth is becoming the bottleneck of the overall system. As serial transmission becomes the major approach for high-speed interfaces, this issue underlines the existing challenges in the design of a robust transceiver in a complex environment.

A simplified block diagram of clocking architectures for common serial links is shown in Fig. 1a. It consists of a transmitter, a channel, and a receiver. The synchronous system shares a global frequency source (top of Fig. 1a), its transmitter and receiver have the same frequency and phase (top of Fig. 1b), and the phase error is zero (Fig. 1c). In the mesochronous system (middle of Fig. 1a), every participant has the same frequency but an unknown phase. The phase error between the transmitter and the receiver is constant over time. The more complex and common situation is the plesiochronous system (bottom of Fig. 1a). There is a constant frequency offset between the transmitter and the receiver, which results in a linear ramp phase error trajectory (shown in red in Fig. 1c). The frequency offset is usually of an order of 10^{-4}. In some extreme cases, such as with a poor-quality oscillator and high temperature difference, the offset could be up to $\pm5\times10^{-3}$. Since the receiver is responsible for recovering the clock and data from the incoming serial data in these systems, a robust transceiver is the key while designing a receiver suitable for different clocking architectures, especially for a plesiochronous system with a large frequency offset.

There are two methods to implement clock and data recovery (CDR): analog (Anand and Razavi, 2001; Coban *et al*., 2005) and digital (Sidiropoulos

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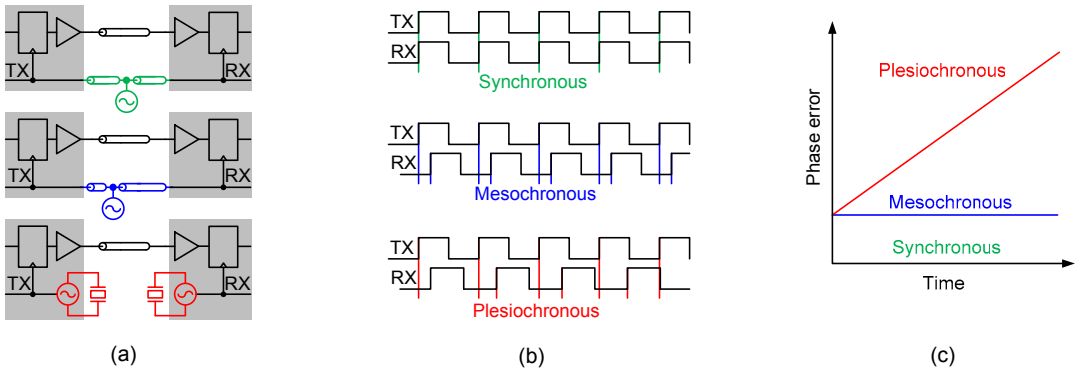


Fig. 1 Clocking architecture (a), timing relationship (b), and phase error trajectory (c) of a common serial link
References to color refer to the online version of this figure

and Horowitz, 1997; Tamura *et al*., 2001; Leibowitz *et al*., 2007; Sarvari *et al*., 2010; Abiri *et al*., 2011; Kalantari and Buckwalter, 2013; Niu *et al*., 2013; Yang *et al*., 2013). A conventional analog CDR usually suffers from current mismatch in the charge pump, a large analog loop filter (LF), and sensitivity to process, voltage, and temperature (PVT) variations. On the other hand, digital CDRs are promising architectures for high-speed interfaces compared to their analog counterparts due to robustness to variations and scalability with advanced technology. However, to save area, digital methods often use low-bit digital-to-analog circuits (DAC), which makes it hard to deal with large frequency offsets with low jitter.

In this paper we propose a wide-tracking-range CDR circuit. By comprehensively analyzing the second-order bang-bang (BB) CDR, a digital CDR controller is adopted to extend the tracking range to compensate for the large frequency offset in a plesiochronous clocking system. A symmetrical latch is proposed to overcome the nonsymmetry problem of the conventional set-reset (SR) latch. Meanwhile, a phase interpolator (PI) with clock condition circuit is proposed to improve the jitter performance of the receiver. Finally, a dithering source is designed to achieve 8-bit resolution out of the 6-bit phase DAC, which saves the area with a higher resolution.

2 Clock and data recovery architecture

CDR adopts a dual-loop architecture (Sidiropoulos and Horowitz, 1997) to provide a large gain of the phase detector (PD), and thus is easy to cooperate with a digital controller which is less affected by PVT. It is composed of a continuous-time linear equalizer (CTLE), samplers, demultiplexers, a digital controller, and a PI. CTLE is used to compensate for the loss of an attenuated signal through the channel. Two samplers sample the center of the incoming signal using 0° and 180° clocks, while the other two sample the edge of the signal using 90° and 270° clocks. The 2-bit data and edge signals are then converted to 10-bit, 500 Mb/s parallel data (D) and edge (E) signals by demultiplexers. The second-order CDR digital controller receives demultiplexed D and E samples and drives the PI to adjust the four quadrature clocks to the center of the data. To characterize the jitter performance of CDR, the sampled data is serialized and transmitted by pre-emphasis current mode logic (CML) buffer.

3 Second-order CDR system analysis

In a plesiochronous system, there is a frequency offset between the transmitter and the receiver, which results in a large accumulated phase offset. As described by Razavi (2003), the first-order BB CDR has its limitation for such a deterministic phase offset. Therefore, a second-order BB CDR is used (Fig. 2).

Fig. 3 shows the system block diagram of the implemented CDR in the phase/frequency domain. The input f_{in} has a small phase deviation $\Phi(t)$, and also a small difference Δf compared with the reference frequency f_{ref}. The slicer limits the phase error Φ_e between the phase of input data Φ_d and the phase of output clock Φ_{PI} to either ε=1 if Φ_e>1 or ε=−1 if Φ_e<1.

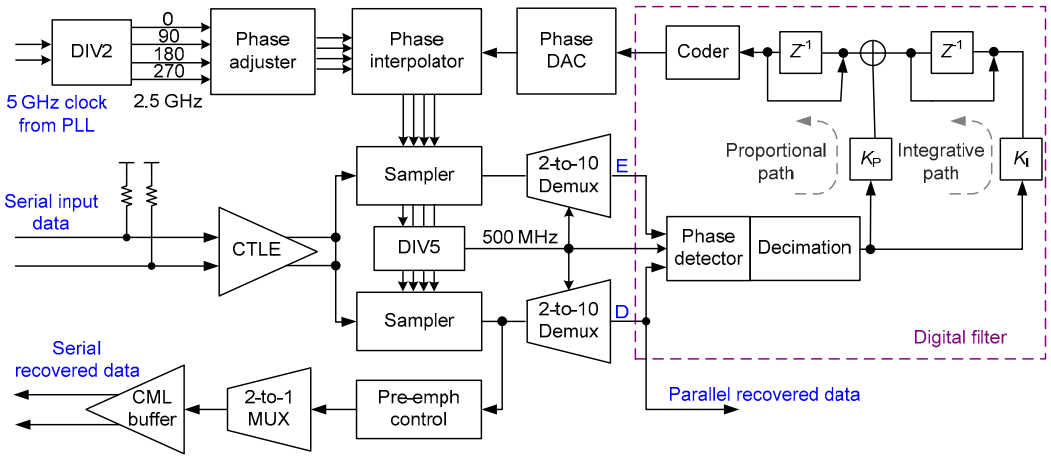


Fig. 2 Receiver architecture

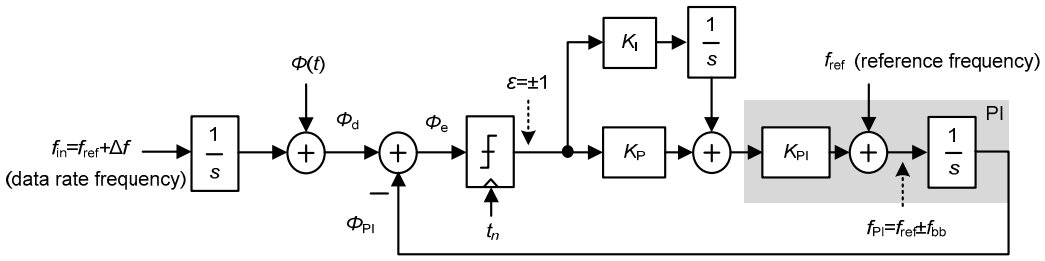


Fig. 3 System view of the implemented second-order bang-bang (BB) clock and data recovery (CDR)

The phase step of the proportional path in one update time (t_{update}=1/(2mf_{ref}), where the factor 2 corresponds to half rate operation, and m is the demux factor) is $\Phi_{bb}=2\pi K_P K_{PI} t_{update}$, while the phase step of the integrative path is $\Phi_{bb\text{-}I}=2\pi K_I K_{PI}\cdot t_{update}^2/2$. The ratio of these two is the stability factor of the loop (Razavi, 2003):

$$\xi=\frac{\Phi_{bb}}{\Phi_{bb\text{-}I}}=\frac{2K_P}{K_I t_{update}}. \tag{1}$$

Assuming that the nth sampling time is $t_n=n\cdot t_{update}$, and that the polarity of the loop phase offset is constant, PI adjusts the phase of the clock in one direction, i.e., ε=1 or ε=−1. The relationship of the PI's output clock phase between t_{n+1} and t_n is

$$\begin{aligned}\Phi_{PI}(t_{n+1})=\Phi_{PI}(t_n)&+\int_{nt_{update}}^{(n+1)t_{update}}2\pi\cdot\varepsilon K_P K_{PI}\mathrm{d}t\\&+\int_{nt_{update}}^{(n+1)t_{update}}2\pi\cdot\varepsilon K_I K_{PI}\mathrm{d}t,\end{aligned} \tag{2}$$

which, when simplified, becomes

$$\Phi_{PI}(t_{n+1})=\Phi_{PI}(t_n)+\varepsilon\cdot\Phi_{bb}\left(1+\frac{1}{\xi}+\frac{2n}{\xi}\right). \tag{3}$$

For ε=1 and using induction, the output phase of PI at t_{n+1} is

$$\Phi_{PI}(t_{n+1})=\Phi_{bb}\left(n+\frac{n^2}{\xi}\right). \tag{4}$$

Therefore, the slope of the output phase can be obtained by substituting $n=t/t_{update}$ and differentiating

$$\Phi'_{PI}(t_{n+1})=2\pi\cdot f_{bb}\left(1+\frac{2n}{\xi}\right), \tag{5}$$

where f_{bb} is the frequency step of the proportional path in one update time, $f_{bb}=K_P K_{PI}$. The tracking range condition yields

$$-f_{bb}\left(1+\frac{2n}{\xi}\right)<\Delta f<f_{bb}\left(1+\frac{2n}{\xi}\right). \tag{6}$$

The tracking range of the second-order BB CDR loop is larger than that of the first-order loop ($-f_{bb}<\Delta f<f_{bb}$) due to the integrative path. Assuming $\Delta f=0$, for $\Phi(t)=A\sin(2\pi f_{mod}t)$, the maximum derivative of the input data phase deviation, $\mathrm{d}[\Phi(t)]/\mathrm{d}t$, must be smaller than the tracking range. Thus, from Eq. (5), the slew-rate-limited phase modulation amplitude expressed in unit interval (UI) is

$$A\le\frac{f_{bb}}{f_{mod}}\left(1+\frac{2n}{\xi}\right). \tag{7}$$

Thus, the second-order BB CDR loop extends the slew rate limit by a factor of $1+2n/\xi$.

From the results above, it can be observed that the frequency tracking range and slew rate limit of the CDR loop are extended by the integrative path, and the loop dynamics is controlled by two degrees of freedom, f_{bb} and ξ (Razavi, 2003).

4 Circuit implementation

4.1 Sampler design

The high data stream from CTLE is sampled by samplers, and converted to serial data and edge streams. To improve the sensitivity of the receiver with a small delay, most samplers use sense-amplifier based flip-flop (SAFF) (Tamura *et al*., 2001; Leibowitz *et al*., 2007). A typical SAFF consists of the sense amplifier (SA) and the salve SR latch, as shown on the left of Fig. 4. However, the falling edge of the typical SR latch output signals Q and QB will always be delayed with respect to the rising edge (Nikolic *et al*., 2000). This causes the determined jitter and limits the performance of the receiver.

To overcome the problem of non-symmetry and process variation effects of the SR latch, we propose a symmetrical latch, which is shown on the right of Fig. 4. The two cross-coupled latch units operate as follows: When input SET is low and RESET is high, the Q output is set to low and QB is set to high at the same time. Conversely, when input SET is high and RESET is low, the Q output is set to high and QB is set to low. When the two input signals are both high, it holds the status, while the low level at both input signals is forbidden. The SET and RESET signals of the proposed latch arrive at the inputs of the latch at the same time, which is different from a typical SR latch where the signal is always delayed by the NAND gate. Fig. 5 shows a comparison between the output of the SR latch (middle) and the proposed symmetrical latch (bottom) with the same SET and RESET signals (top). We can see that the output symmetry of the proposed latch outputs Q and QB is improved.

4.2 Digital CDR controller

The digital CDR controller consists of a phase detector (PD), a digital filter, a resolution-improvement unit (RIU), and a binary-to-thermometrical encoder (Fig. 6). Since the demultiplexers lower the data and edge signals to 500 Mb/s, the digital controller is implemented by automatic place-and-route using standard 65-nm CMOS technology.

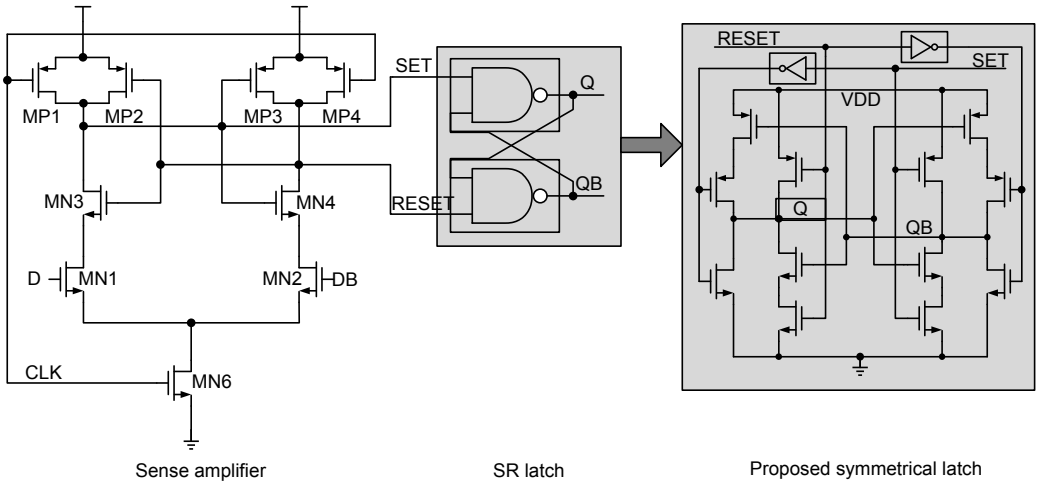


Fig. 4 Typical SAFF and the proposed symmetrical latch

The BB PD is applied to generate parallel early–late phase error signals. The decimation is able to produce a single, multibit sum signal of the parallel phase errors. As described in Section 3, to extend the tracking range of CDR, the digital filter employs a second-order structure. We need an 8-bit binary code to achieve a 1.5625 ps phase step size of PI at 2.5 GHz. Therefore, the frequency resolution f_{res} can be expressed as

$$f_{\text{res}} = \frac{S_{\text{step}}}{N \cdot \text{UI}}, \tag{8}$$

where S_{step} is the step size, N is the number of UIs that pass before a step occurs, and UI is the UI size. In our design, with N=10 and UI=200 ps, the f_{bb} of CDR is 7.8125×10^{-4}.

The proportional path of the digital filter tracks the instantaneous phase error, while the integrative path compensates for the 5×10^{-3} offset difference between the local reference clock and the incoming data. The integrative path accumulates the continuous stream of the sum signal, and drives the PI toward the frequency lock. Considering that only the top 8 bits of

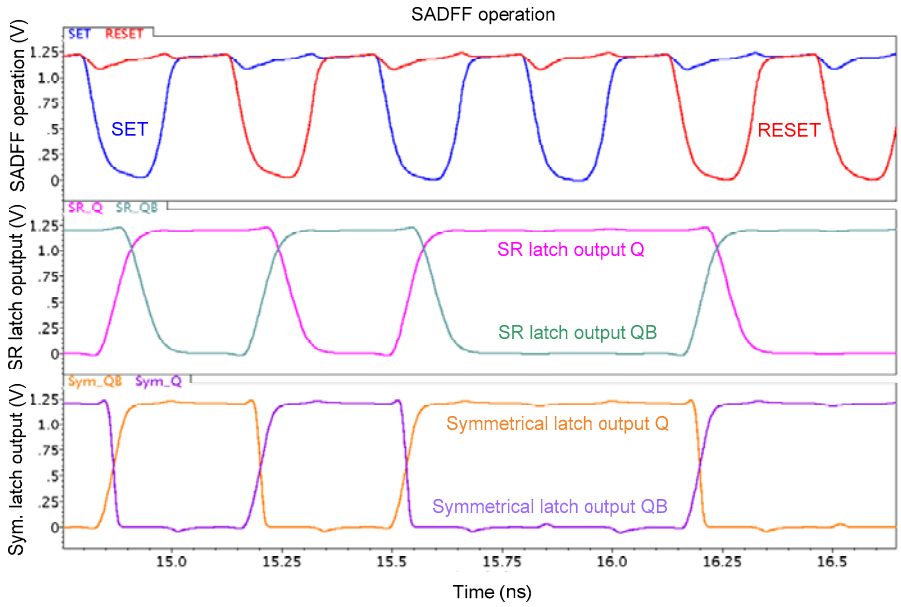


Fig. 5 Comparison between a typical SR latch and the proposed symmetrical latch output

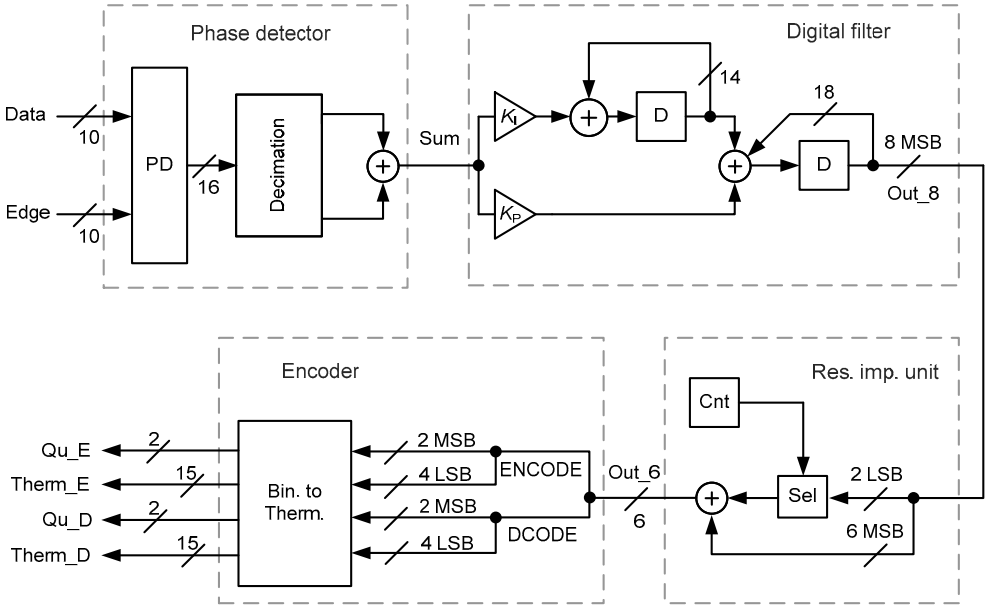


Fig. 6 Digital CDR controller architecture

the 18-bit output integrator in the digital filter is sent to the RIU, we obtain an effective gain of 2^{-10}. Thus, the tracking range of CDR is

$$\Delta f = 2^{-10} \cdot f_{\mathrm{bb}} \cdot 2^{W_{\mathrm{I}}-1}, \tag{9}$$

where W_{I} is the width of the integrator in the integrative path. Using a 14-bit integrator, the tracking range of CDR is up to 6.25×10^{-3}.

The 8-bit binary code drives the phase DAC to achieve a 1.5625 ps step size of PI. However, the 8-bit DAC will occupy a large area. In this work, we add a dithering source to achieve 8-bit resolution out of the 6-bit phase DAC. The dither output code is dynamically modulated by the lower 2 bits of the input 8-bit code (Fig. 7). This dither code is then added to the upper 6 bits, which makes the average step equal to one-fourth of the LSB.

4.3 Phase interpolator

PI performs phase mixing by the weighted summation of the PLL quadrature clock pair (Yang *et al*., 2013). It mixes the two quadrature differential clocks $C_{\mathrm{I}}=A\sin(\omega t)$ and $C_{\mathrm{Q}}=A\sin(\omega t+\pi/2)$, where A is the amplitude of the clock. Therefore, the overall interpolation range of 2π is divided into four quadrants, as shown on the left side of Fig. 8. The PI output can be expressed as

$$C_{\mathrm{PI}} = \alpha_{\mathrm{I}} C_{\mathrm{I}} + \alpha_{\mathrm{Q}} C_{\mathrm{Q}}. \tag{10}$$

Each quadrant covers $\pi/2$, so the weighting factors α_{I} and α_{Q} are always positive.

The signal Qu from the digital controller selects the quadrant of the phase and interpolates between them to generate 16 phase positions within each quadrant using the thermometer code. There are two PIs in our CDR, one for data phase interpolation and the other for the edge phase.

The interpolator uses a current-steering DAC, which supplies tail currents to the differential pairs to process the quadrant clock phases and drive a common resistive load (Fig. 8). The DAC employs 16 switch cells for each quadrant. The currents of two differential pair clocks controlled by the DAC are complementary. It means that the sum of two currents remains constant, and thus the output amplitude of the interpolator is constant. Since the slew rate of the input clock signal influences the operation of PI (Weinlader, 2001), an input buffer is placed at its input. An AC-coupled duty-cycle correction output buffer follows the interpolator. It cancels the common output mismatch and duty-cycle distortion, and

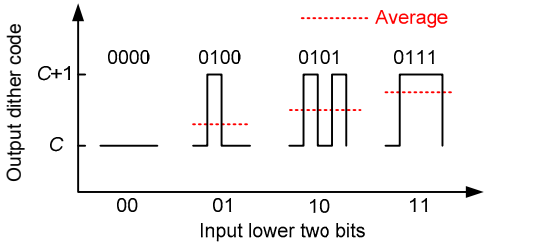


Fig. 7 Concept of phase DAC resolution improving dither

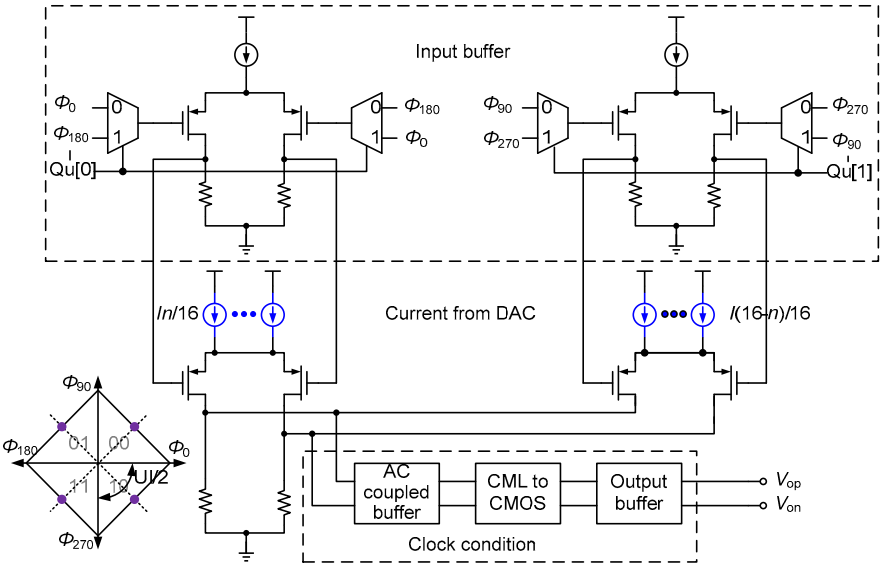


Fig. 8 Architecture of the phase interpolator

amplifies the CML output to the CMOS level. The comparison between the PI with and without output buffer is shown in Fig. 9. The output buffer makes the duty-cycle distortion be reduced from 55.04% to 50.08%. Post simulation shows that the proposed PI has good linearity with 1.01 LSB integral nonlinearity (INL) and 1.27 LSB differential nonlinearity (DNL).

5 Measurement results

The receiver has been implemented in 65-nm CMOS technology. Fig. 10 shows a photomicrograph of the cell. The module occupies an area of 0.147 mm^2 with a 0.082 mm^2 core area. The macro cell is fed by an internal I/Q half-rate differential reference clock. The measured power consumption of the receiver core is about 41 mW with a 1.2 V power supply at 5 Gb/s.

A pseudo-random bit sequence (PRBS) of length 2^7–1 is sent to the chip, and the recovered data is buffered by the CML buffer through a 10-cm FR4 PCB trace, an SMA connector, and a 1.5-m RG58 cable. Fig. 11 shows the eye diagram of the output. The root-mean-square (RMS) jitter is only 7.85 ps for 2.5 Gb/s and 6.70 ps for 5 Gb/s. The tracking range of the receiver is $\pm6\times10^{-3}$ for 2.5 Gb/s and $\pm6\times10^{-3}$ for 5 Gb/s. This frequency tracking range is measured without any degradation of the bit error rate (BER) from its nominal value of 10^{-12}.

Fig. 12 shows the jitter tolerance test results. It can be seen that the proposed second-order CDR system effectively tracks both low- and high-frequency jitter. The maximum jitter tolerance value is 5.5 UI peak-to-peak at 0.2 MHz with BER=10^{-12} for 5 Gb/s operation, while the minimum value is 0.32 UI peak-to-peak at 10 MHz.

The performances of the overall CDR of this work and some prior works are summarized in Table 1. As the analysis above shows, the use of the second-order digital filter achieves a tracking range of $\pm6\times10^{-3}$, while the output RMS jitter is only 6.7 ps at 5 Gb/s. Meanwhile, the dither code makes the area much smaller. Furthermore, it consumes less power (at least 25% less) than reported in other works.

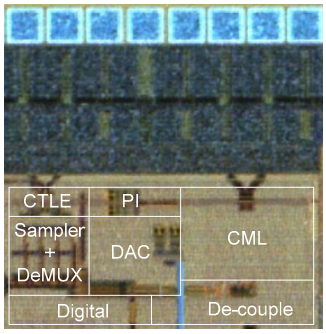


Fig. 10 Photo of the receiver macro

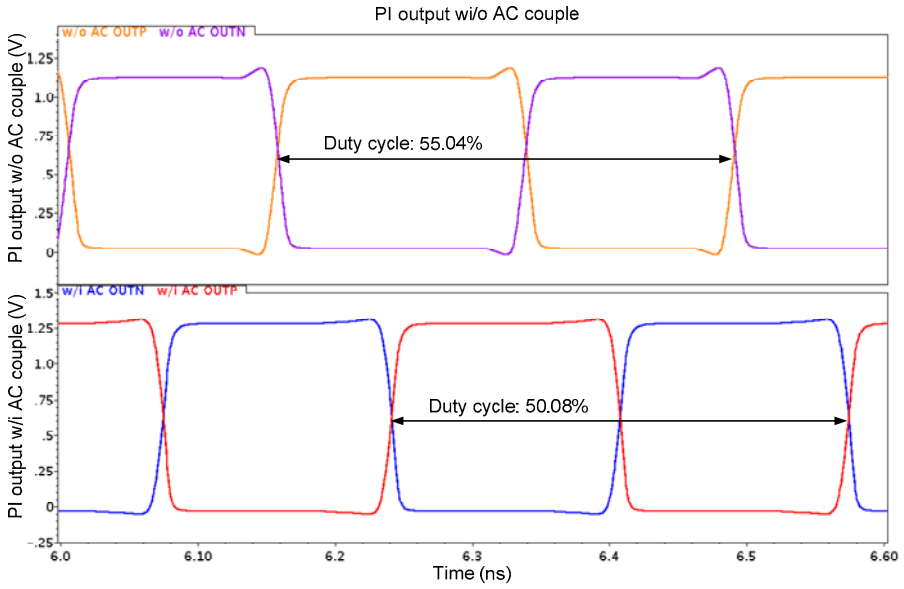
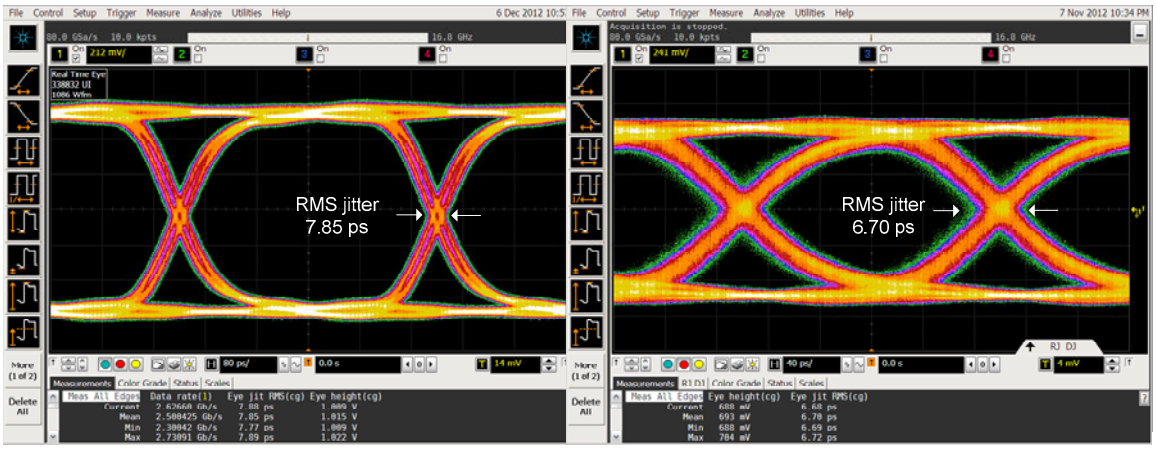


Fig. 9 Comparison between output duty-cycle distortion with and without output buffer



(a) (b)

Fig. 11 Eye diagram of recovered serial data through CML buffer at 2.5 Gb/s (a) and 5 Gb/s (b)

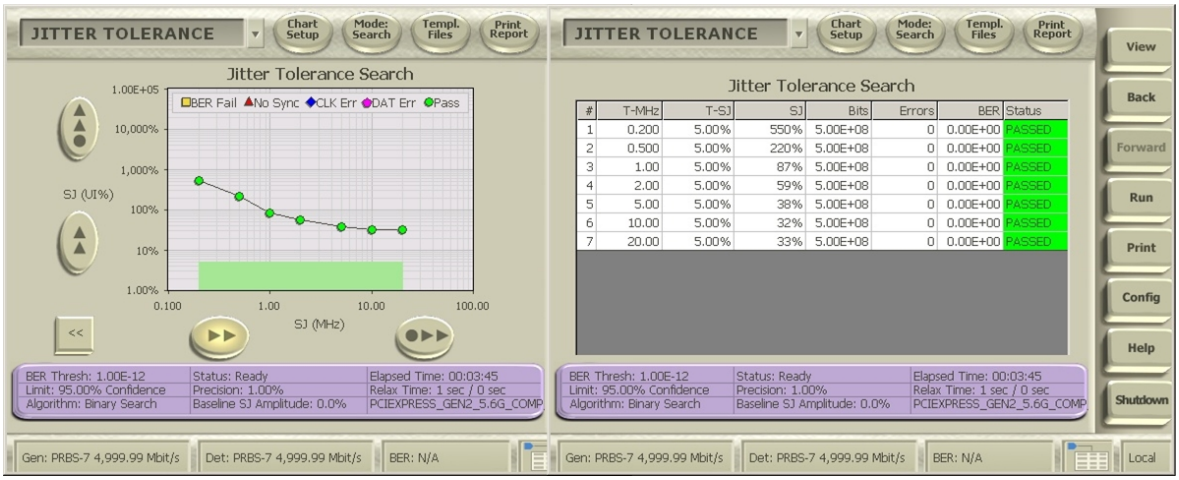


Fig. 12 Sinusoidal jitter tolerance measurement

Table 1 Receiver performance summary

Parameter	Value					
	Coban *et al.* (2005)	Agrawal *et al.* (2009)	Kalantari and Buckwalter (2013)	Abiri *et al.* (2011)	Sarvari *et al.* (2010)	This work
Technology (CMOS)	150 nm	130 nm	130 nm	65 nm	65 nm	65 nm
Supply voltage (V)	1.2	1.45	1.2	1.2	1.2	1.2
Operating frequency (Gb/s)	2–3.2	5	5–7	5	5	5
Maximum frequency offset ($\times10^{-6}$)	±1200	±5000	±200	–	200	±6000
Bit error rate	–	10^{-12}	10^{-12}	10^{-12}	10^{-12}	10^{-12}
High frequency jitter tolerance (UI)	0.5	–	0.4	0.2	0.24	0.32
Power consumption (mW)	73.2	54.2	67.9	114	211.2	40.68
Active die area (mm^2)	0.43	0.35	1.025	0.4	0.374	0.082

6 Conclusions

We have presented a 5 Gb/s receiver with a wide-tracking-range CDR circuit. A digital CDR controller, which is not sensitive to process variations, is adopted to extend the tracking range. Meanwhile, a PI with clock condition circuit is adopted to improve the jitter performance. Finally, a dithering source is designed to achieve 8-bit resolution out of the 6-bit phase DAC, which saves the area with higher resolution. The whole receiver circuit is implemented in 65-nm CMOS. The second-order digital filter has a $\pm 6\times 10^{-3}$ tracking range. Measurements show that CDR has good jitter tolerance performance with BER$<10^{-12}$. The extremely compact receiver with relatively low power consumption is thus suitable for high-density, robust serial link applications.

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