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Reversible binary subtractor design using quantum dot-cellular automata

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Abstract: In the field of nanotechnology, quantum dot-cellular automata (QCA) is the promising archetype that can provide an alternative solution to conventional complementary metal oxide semiconductor (CMOS) circuit. QCA has high device density, high operating speed, and extremely low power consumption. Reversible logic has widespread applications in QCA. Researchers have explored several designs of QCA-based reversible logic circuits, but still not much work has been reported on QCA-based reversible binary subtractors. The low power dissipation and high circuit density of QCA pledge the energy-efficient design of logic circuit at a nano-scale level. However, the necessity of too many logic gates and detrimental garbage outputs may limit the functionality of a QCA-based logic circuit. In this paper we describe the design and implementation of a DG gate in QCA. The universal nature of the DG gate has been established. The QCA building block of the DG gate is used to achieve new reversible binary subtractors. The proposed reversible subtractors have low quantum cost and garbage outputs compared to the existing reversible subtractors. The proposed circuits are designed and simulated using QCA Designer-2.0.3.

Key words: Quantum dot-cellular automata (QCA); Reversible logic; DG gate; Binary subtractor; Quantum cost
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1 Introduction

The world is moving from large circuitry fields to small circuitry fields. This causes higher complexity in device fabrication. Shrinking transistor sizes and power dissipation are the major barriers in the development of smaller and more powerful circuits. At least when the transistor size approaches the atomic scale, according to Moore's law, duplication of transistor density will not be possible. However, when scaling comes down to the subatomic level, many problems occur. Physical limits like quantum effects and nondeterministic behavior of small current, and such technological limits as high power consumption and design complexity, may hold back the future program of circuit scaling in conventional microelectronics. Hence, an alternative technology is required for future design. Quantum dot-cellular automata (QCA) is a transistorless, most promising nanotechnology that can be used to build nano-circuit (Lent and Tougaw, 1997; Orlov *et al*., 1997). The conventional computer is irreversible in nature; i.e., once a logic block generates the output bits, the input bits are lost. As an example, for a binary AND gate, when inputs are (1, 0) or (0, 1), we obtain a single '0' output, and the other bit '1' is destroyed. A single bit of information that is lost generates heat energy $k_B T \ln 2$, where k_B is the Boltzmann constant and T the absolute computing temperature (Landauer, 1961). A possible solution is reversible computing, where no bit is lost during computation. Hence, loss is minimized; i.e., a logically reversible circuit can consume less energy than any conventional circuit (Arjmand *et al*., 2013; Kianpour and Sabbaghi-

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Nadooshan, 2014). The currently used complementary metal oxide semiconductor (CMOS) technology consumes very low energy, lower than those required by any other technology. However, it has different problems, such as low device density and high current leakage (ITRS, 2005). Thus, reversible logic design in CMOS produces complexities. QCA can be used as an alternative solution to this problem because of its high device density and high switching speed. In QCA, information is stored based on the polarization of the cell and the message is passed without an interconnecting wire as in a traditional system (Lent *et al*., 1993; Zhang *et al*., 2004; Yang *et al*., 2012; Das and De, 2015; Farazkish and Khodaparast, 2015; Lakshmi *et al*., 2015). Hence, ohmic loss as in a current-carrying wire does not take place. In this study, we have achieved the design and implementation of DG gate based reversible binary subtractors using QCA. Implementation and simulation of the proposed circuits are performed using QCA Designer-2.0.3. The subtractor is a major component used in the oscillator and for code conversion. In particular, to perform digital signal processing (DSP) in nano-communication systems, a dedicated subtractor unit is essential. Thus, this study focuses on low power dissipation faster subtractor design through QCA.

Extensive literature has been reported that characterizes the design of reversible logic circuits in QCA. Nevertheless, there is still a scope to add a new building block for QCA-based reversible logic computing. However, the promising technological basis of the reversible logic-computing paradigm is still unsolved. Keeping in mind the inherent properties of QCA, we have proposed reversible logic based new subtractors based on QCA. This work can be used to implement dedicated low power and faster subtractor units for DSP for nanocommunication systems. We have made the following contributions: (1) realization of a reversible DG gate using QCA; (2) investigation of the universal nature of the DG gate; (3) estimation of quantum cost of the DG gate; (4) DG gate based design of a reversible binary half-subtractor and full-subtractor and their implementation in QCA; (5) outline of comparative study with prior work; (6) estimation of the quantum cost of the proposed reversible QCA subtractors compared with conventional designs; (7) fault analysis and defect coverage of a single missing/additional cell for the proposed circuit.

2 Background materials

2.1 QCA overview

A QCA cell consisting of four quantum dots (Lent and Tougaw, 1997) is shown in Fig. 1a. The dots provide a barrier to hold electrons within it. The dots are connected via a tunneling wire. Electrons can tunnel through these four dots via the tunneling wire (Gladshtein, 2013; Ghosh *et al*., 2014a; Hashemi and Navi, 2014). Two extra electrons are added to each QCA cell. The electrons occupy the antipodal position due to their mutual electrostatic repulsion. So, depending on the position of electrons in a QCA cell, two different structures may exist, termed 'polarization of the cell' and denoted by P (Das and De, 2016e; 2016f). As shown in Figs. 1b and 1c, the value of P can be +1 or −1. P=+1 and P=−1 indicate the logic values '1' and '0', respectively. P=0 indicates an unpolarized cell (Janez *et al*., 2012; Arjmand *et al*., 2013; Ghosh *et al*., 2014b), i.e., containing no information.

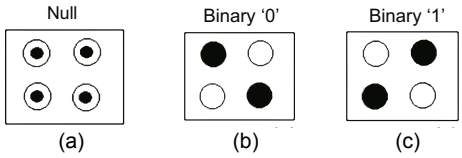

Fig. 1 Different QCA cell polarizations: (a) P=0; (b) P=−1; (c) P=+1

The fundamental logic gate for the QCA device is the three-input majority gate (MV) (Fig. 2). The output of MV depends on its input majority (Das K and De, 2010a; 2011; Das JC and De, 2012; Das K *et al*., 2013; Das JC *et al*., 2015). Let A, B, C be the inputs to MV. Then the Boolean expression for MV can be written as

$$M(A,B,C) = AB + BC + CA. \tag{1}$$

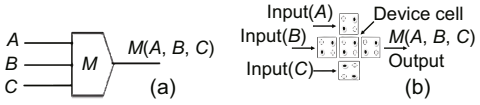

Fig. 2 The majority gate: (a) QCA schematic; (b) QCA layout

By setting one of the inputs of MV to logic value '0' or '1', a logical AND-gate or OR-gate can be made, respectively. The QCA schematic and QCA layout of the AND-gate and OR-gate are shown in

Figs. 3a and 3b, respectively (Das K and De, 2010b; 2011; Das JC and De, 2012; 2016d; Das K *et al*., 2013; Das JC *et al.*, 2015). The corresponding Boolean expressions are

$$M(A,B,0)=A.B, \tag{2}$$

$$M(A,B,1)=A+B. \tag{3}$$

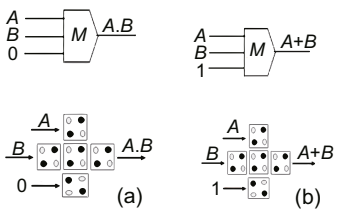

Fig. 3 The QCA logic AND-gate (a) and OR-gate (b)

The QCA wire can be made by arranging the QCA cells consecutively. The flow of binary information through the QCA wire takes place by the electrostatic interaction between cells. The QCA wire is essential for carrying the information from one position to another within a QCA circuit. There are two types of QCA wire (Fig. 4). In 90° QCA wire, the entire array of QCA cells has identical polarization. In 45° QCA wire, the polarization alternates at every consecutive cell (Das K and De, 2010a; 2011; Das JC and De, 2012; Karim and Walus, 2014; Das K *et al*., 2013; Das JC *et al.*, 2015).

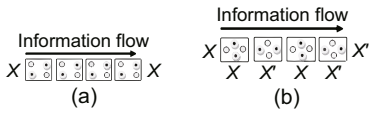

Fig. 4 The QCA 90° wire (a) and QCA 45° wire (b)

The QCA inverter can be made by placing QCA cells at 45°, i.e., with corners in a position where they touch each other (Das and De, 2012; Karim and Walus, 2014; Das *et al*., 2015). Due to the electrostatic interaction between cells, the logic values '0' and '1' are inverted to '1' and '0', respectively. These two basic types of QCA inverters are shown in Fig. 5 (Das *et al*., 2013; Hayati and Rezaei, 2014).

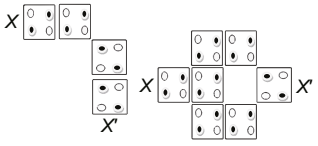

Fig. 5 QCA inverters

QCA clocking consists of four-phase lagging by $\pi/2$ (Hennessy and Lent, 2001; Das and De, 2015), as shown in Fig. 6. This clocking scheme produces a new way to design logic circuits that are different from the CMOS circuit. In the 'switch phase', electrons start tunneling between dots, as the dots are influenced by the electrons of their neighboring cells. The QCA cell switches to a polarized state from an unpolarized state, and the barrier of the dot is raised. In the 'hold phase', a barrier of the dots is in the higher state, and electrons cannot tunnel between dots. The cells maintain their current state, i.e., fixed polarization. In the 'release phase', a barrier of the dots is lowered, electrons can tunnel between dots, and the state of the cell becomes unpolarized. In the 'relax phase', the barrier remains lowered and the cells stay in an unpolarized state (Dey *et al*., 2012; Pradhan and De, 2013; Das and De, 2015).

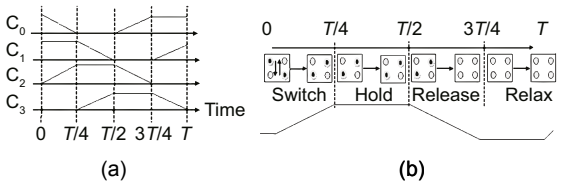

Fig. 6 Four-phase clocking (a) and QCA operation during one clock phase (b)

2.2 Half-subtractor

A half-subtractor performs subtraction of two bits, produces their differences, and specifies if there is any borrow. Let D be the difference of the two input bits X, Y. The output borrow B=0 as long as $X \geq Y$. B will be 1 if X=0 and Y=1 (Mano and Ciletti, 2011). The output D is the result of the arithmetic operation $2B+X-Y$. The Boolean functions of the two outputs are

$$D = X'Y + XY', \tag{4}$$

$$B = X'Y. \tag{5}$$

2.3 Full-subtractor

A full-subtractor performs the subtraction of two bits and checks whether the lower significant stage may borrow 1 or not (Vankamamidi *et al*., 2005). The Boolean functions for the difference bit and borrow bit are

$$D = X'Y'Z + X'YZ' + XY'Z' + XYZ, \tag{6}$$

$$B = X'Y + X'Z + YZ, \tag{7}$$

where X, Y, and Z are minuend, subtrahend, and previous borrow, respectively.

2.4 Related work

Several studies have been conducted on QCA reversible logic design. The detection of multiple faults in the 1D array of reversible QCA gates was described by Ma *et al*. (2009). Thapliyal and Ranganathan (2010) designed concurrently testable conservative reversible latches, such as the SR latch, D latch, JK latch, and T latch, for molecular QCA. The defect analysis for the QCA circuit due to a single missing or an additional cell was performed by Thapliyal and Ranganathan (2010). Saravanan and Kalpana (2013) proposed a systematic and novel approach to incorporate reversible logic in QCA. Thapliyal and Ranganathan (2009a; 2009b) proposed a novel conservative reversible logic gate termed 'conservative QCA (CQCA)'. Further, this CQCA gate was used to design molecular QCA based concurrently testable circuits. The faulty output patterns caused by defects in the QCA Fredkin gate and CQCA gate have also been explored by Thapliyal and Ranganathan (2009a; 2009b). A novel conservative logic gate (CLG) was proposed by Das and De (2010b). A 3×3 QCA tile was used to achieve the nanostructure of CLG. Ottavi *et al*. (2011) described the design of ultra-low-power and high throughput pipelined architecture for QCA. A ripple carry adder and an XOR-tree parity checker were initially used to evaluate this pipelined architecture in terms of power consumption and throughput. Thapliyal *et al*. (2013) described the design of testable latches, such as double-edge triggered flip-flop and master-slave flip-flop, using conservative reversible logic gates. Two test vectors, all 0's and all 1's, were employed to evaluate the design. Besides, a new conservative gate, namely, the multiplexer conservative QCA (MX-CQCA) gate, was proposed by Thapliyal *et al*. (2013). The MX-CQCA gate is similar to the Fredkin gate and is irreversible in nature. It can function like a 2:1 multiplexer. The MX-CQCA gate outshines the Fredkin gate in terms of the number of MVs, circuit density, and speed. Shah *et al*. (2012) implemented a QCA-based multifunction reversible gate (BVMF). This BVMF gate can function as a comparator. It also outlines how a multifunction reversible gate can be organized to work as a universal gate. Das and De (2015) explored the design and implementation of a binary incrementer based on reversible logic and its incorporation in QCA.

3 Reversible DG gate and its quantum dot-cellular automata implementation

DG gate, invented by Dehghan *et al*. (2014), is a new reversible gate. A DG gate consists of three inputs and three outputs. The mapping from input to output is $P=A$, $Q=(A\oplus B)'$, and $R=(A.(B'))\oplus C$, where inputs are denoted by A, B, and C. The corresponding outputs are denoted by P, Q, and R. The block diagram is shown in Fig. 7. The truth table is outlined in Table 1.

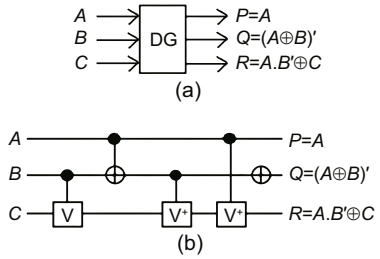

Fig. 7 The reversible DG gate: (a) block diagram; (b) quantum realization

Table 1 Truth table of the DG gate

Input			Output		
A	B	C	P	Q	R
0	0	0	0	1	0
0	0	1	0	1	1
0	1	0	0	0	0
0	1	1	0	0	1
1	0	0	1	0	1
1	0	1	1	0	0
1	1	0	1	1	0
1	1	1	1	1	1

The majority gate expressions for different outputs of the proposed reversible QCA DG gate are drawn as

$$P = A, \tag{8}$$

$$Q = (M(M(A',B,0),M(A,B',0),1))', \tag{9}$$

$$R = M(M((M(A,B',0))',C,0), M(M(A,B',0),C',0),1). \tag{10}$$

The schematic of the QCA design for the DG gate and the corresponding QCA layout are shown in Figs. 8a and 8b, respectively.

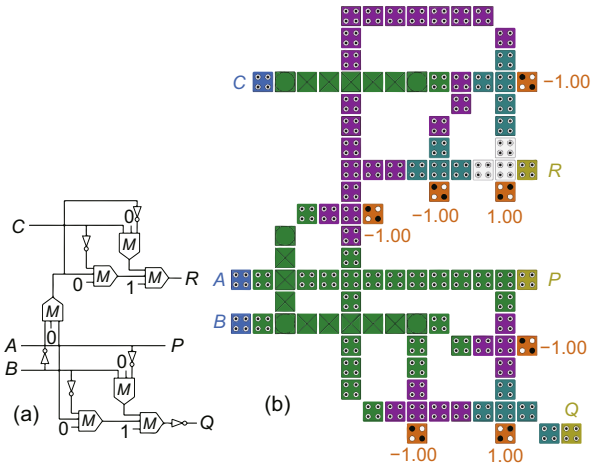

Fig. 8 The reversible DG gate: (a) QCA schematic; (b) QCA layout

3.1 Universatility of the DG gate

The universal NAND gate can be realized using the DG gate (Fig. 9). If input C of the DG gate is fixed to logic 1, and input B is in the complemented form, then output line R generates $(AB)'$. Output at P and Q lines is considered a garbage output. Since the NAND gate is a universal logic gate, it exhibits the universal scenery of the DG gate. The truth table for the DG gate based NAND gate is derived in Table 2.

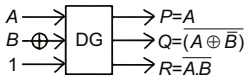

Fig. 9 The NAND gate using the DG gate

Table 2 The truth table of the NAND gate using the DG gate

Input		Output		
A	B	P (Gar)	Q (Gar)	R=$(AB)'$
0	0	0	0	1
0	1	0	1	1
1	0	1	1	1
1	1	1	0	0

The majority gate expressions for the outputs of the DG gate based NAND gate can be drawn as

$$P = A, \tag{11}$$

$$Q = (M(M(A', B', 0), M(A, B, 0), 1))', \tag{12}$$

$$R = M(M((M(A, B, 0))', 1, 0), M(M(A, B, 0), 0, 0), 1). \tag{13}$$

The schematic of the QCA design for the DG gate based NAND gate is shown in Fig. 10a, and the corresponding QCA layout in Fig. 10b.

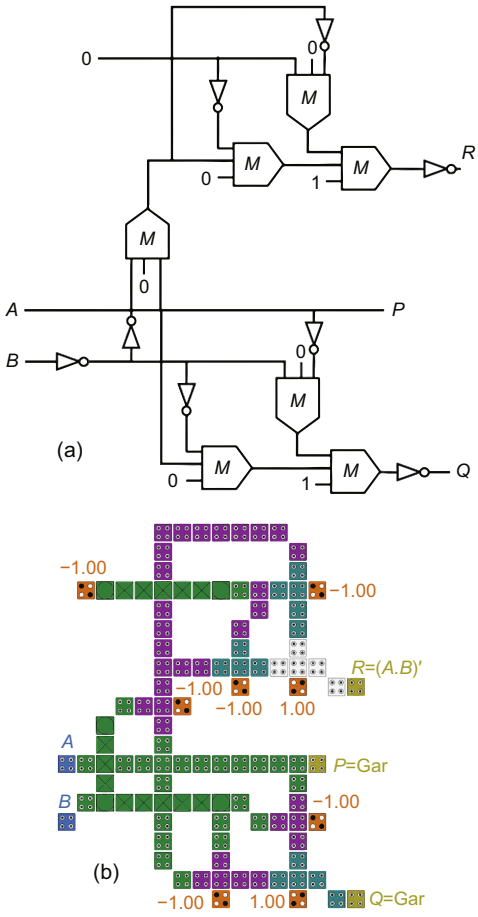

Fig. 10 The NAND gate using the DG gate: (a) QCA schematic; (b) QCA layout

3.2 Quantum cost of the DG gate

The quantum cost of any reversible gate is calculated by the number of CNOT gates (2×2 reversible gates) or quantum logic gates and NOT gates (1×1 reversible gates). The Quantum representation of a NOT gate and a CNOT gate is shown in Fig. 11. All reversible 2×2 gates have quantum cost taken as unity. The quantum cost is measured to zero

for all 1×1 reversible gates (Smolin and DiVincenzo, 1996; Hung *et al*., 2006). The reversible 1×1 gate, such as the NOT gate, is represented in V and V^+ form. V holds the square root of the NOT gate, while V^+ indicates its Hermitian. The V and V^+ gates have the following properties: (1) $V\times V$=NOT; (2) $V\times V^+=V^+\times V=\boldsymbol{I}$; (3) $V^+\times V^+$=NOT. The details of V and V^+ were described in Thapliyal and Ranganathan (2009a). Except in a few conditions, the quantum cost of the reversible logic gate can be obtained with the numbers of CNOT, V, and V^+ gates, which are the basic components of any reversible gate.

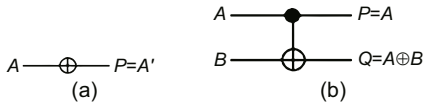

Fig. 11 Quantum representation: (a) NOT gate; (b) CNOT gate

Now consider the quantum representation of the DG gate as shown in Fig. 7b. It can be seen from Fig. 7b that the DG gate requires one controlled V gate, two CNOT gates, and two controlled V^+ gates. Thus, the quantum cost of the DG gate is five.

4 Proposed reversible subtractor

4.1 Reversible half-subtractor

If out of three inputs A, B, and C of the DG gate, as shown in Fig. 7a, input C is fixed to 0 and the positions of A and B are interchanged, then the outputs will be $P=A$, $Q=(A\oplus B)'$, and $R=BA'$. Output Q is again transmitted through the reversible NOT gate to produce the difference bit, and the corresponding borrow bit is generated at output line R. The block diagram of the proposed reversible half-subtractor is shown in Fig. 12. The output at P is considered a garbage value. The Truth table of the DG gate based reversible half-subtractor is shown in Table 3.

The majority gate based output expressions for a proposed reversible half-subtractor can be drawn as

$$P=B, \tag{14}$$

$$\begin{aligned} Q&=(M(M(B',A,0),M(B,A',0),1)')'\\ &=M(M(B',A,0),M(B,A',0),1), \end{aligned} \tag{15}$$

$$\begin{aligned} R=M(&M((M(B,A',0))',0,0),\\ &M(M(B,A',0),1,0),1). \end{aligned} \tag{16}$$

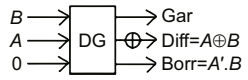

Fig. 12 The proposed reversible half-subtractor

Table 3 The truth table of the proposed reversible half-subtractor

Input		Output		
A	B	P (Gar)	Q (Diff)	R (Borr)
0	0	0	0	0
0	1	1	1	1
1	0	0	1	0
1	1	1	0	0

The schematic of the QCA design for the proposed reversible half-subtractor is shown in Fig. 13a, and the corresponding QCA layout in Fig. 13b.

4.2 Reversible full-subtractor

Table 4 presents the truth table of the proposed reversible full-subtractor. From this truth table, the equations for the difference bit and borrow bit can be derived as Diff=$A\oplus B\oplus C$ and Borr=$A'B\oplus((A\oplus B)'.C)$. Thus, using only two DG gates and two reversible NOT gates, the reversible full-subtractor can be achieved (Fig. 14). The proposed full-subtractor has two garbage outputs.

The majority gate expressions of different outputs for the proposed reversible full-subtractor are described as

$$\mathrm{Gar}_1=B, \tag{17}$$

$$\mathrm{Gar}_2=C, \tag{18}$$

$$\begin{aligned} Q=M(&M(M(M(A',B,0),M(A,B',0),1)',C,0),\\ &M(M(M(A',B,0),M(A,B',0),1),C',0),1), \end{aligned} \tag{19}$$

$$\begin{aligned} R=M(&M(M((M(M(A,B',0),M(A,B',0),1))',\\ &C,0)',M(A',B,0),0),M(M((M(M(A',B,0),\\ &M(A,B',0),1))',C,0),(M(A',B,0))',0),1). \end{aligned} \tag{20}$$

The schematic of the QCA design for the proposed reversible full-subtractor is given in Fig. 15a, and the corresponding QCA layout is given in Fig. 15b.

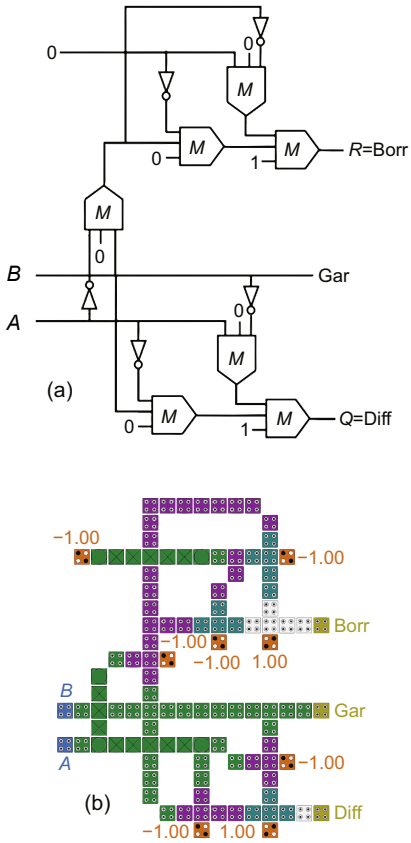

Fig. 13 The DG gate based reversible half-subtractor: (a) QCA schematic; (b) QCA layout

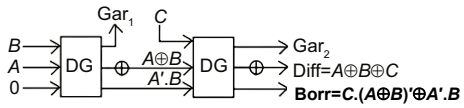

Fig. 14 The proposed reversible full-subtractor

Table 4 The truth table of the proposed reversible full-subtractor

Input			Output			
A	*B*	*C*	Gar_1	Gar_2	Diff	Borr
0	0	0	0	0	0	0
0	0	1	0	1	1	1
0	1	0	1	0	1	1
0	1	1	1	1	0	1
1	0	0	0	0	1	0
1	0	1	0	1	0	0
1	1	0	1	0	0	0
1	1	1	1	1	1	1

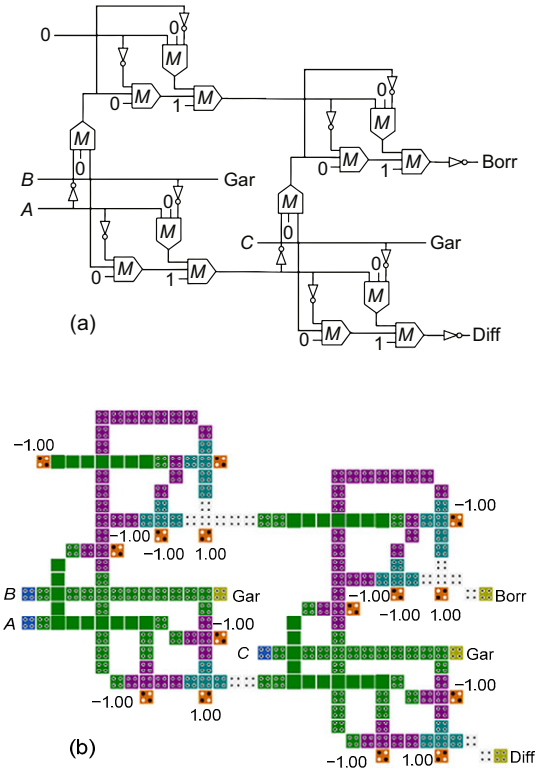

Fig. 15 The proposed reversible full-subtractor: (a) QCA schematic; (b) QCA layout

5 Results and discussions

All the proposed circuits are implemented and simulated using the QCA Designer tool and verified with theoretical values. The following parameters are used during simulation: cell width 20 nm, cell height 20 nm, dot diameter 5 nm, convergence tolerance 0.001000, number of samples 12 800, relative permittivity 12.900, radius of effect 65 nm, clock low 3.80000×10^{-23} J, clock high 9.80000×10^{-22} J, layer separation 11.50000 nm, clock amplitude factor 2.0000, and maximum number of iterations per sample 10 000.

In this section, the simulation results of the proposed QCA circuits are explored. Circuit complexity analysis, quantum cost estimation, comparative study with previous design, and fault analysis have also been performed.

5.1 Simulation results of the proposed QCA-based DG gate

Fig. 16a shows the simulation results of the proposed QCA-based DG gate. The simulation results

are compared with the theoretical values of the DG gate (Table 1). From Fig. 16a, it can be seen that the inputs are A=0, B=0, and C=0, and the outputs will be P=0, Q=1, and R=0. When A=0, B=0, and C=1, then P=0, Q=1, and R=1, and so on. Thus, the circuit works efficiently.

5.2 Simulation results of the proposed DG gate based NAND gate

Simulation results of the proposed reversible NAND gate are shown in Fig. 16b. The output at the other output lines is considered a garbage value. These outputs are verified with the theoretical values of the reversible NAND gate (Table 2). From Fig. 16b, it can be seen that when C is permanently fixed at logic value zero, then the output value is R=0 only if A=1 and B=1, and R=1 otherwise. Thus, the circuit functions efficiently.

5.3 Simulation results of the reversible half-subtractor

Fig. 17a shows the simulation results of the proposed reversible half-subtractor. The simulation results are verified with the theoretical values of the reversible half-subtractor (Table 3). The simulation results given in Fig. 17a show that when the value of input C is fixed to 0, then if A=0 and B=0, the output will be Diff=0 and Borr=0. When A=0 and B=1, the output will be Diff=1 and Borr=1, and so on. This reflects that the circuit works efficiently.

5.4 Simulation results of the reversible full-subtractor

The simulation results of the proposed reversible full-subtractor are shown in Fig. 17b. The simulation results describe that if A=0, B=0, and C=0, the output will be Diff=0 and Borr=0. When A=0, B=0, and C=1, the output will be Diff=1 and Borr=1, and so on. The simulation results are tested and verified with the theoretical values of the proposed reversible full-subtractor (Table 4). This evaluation confirms that the design works efficiently and generates the required outputs.

5.5 Circuit complexity

Table 5 shows the design complexity, i.e., the numbers of QCA cells, majority gates, inverters, and clocking zones required to design the proposed circuits. The DG gate, reversible NAND gate, and half-subtractor have the design complexities as follows:

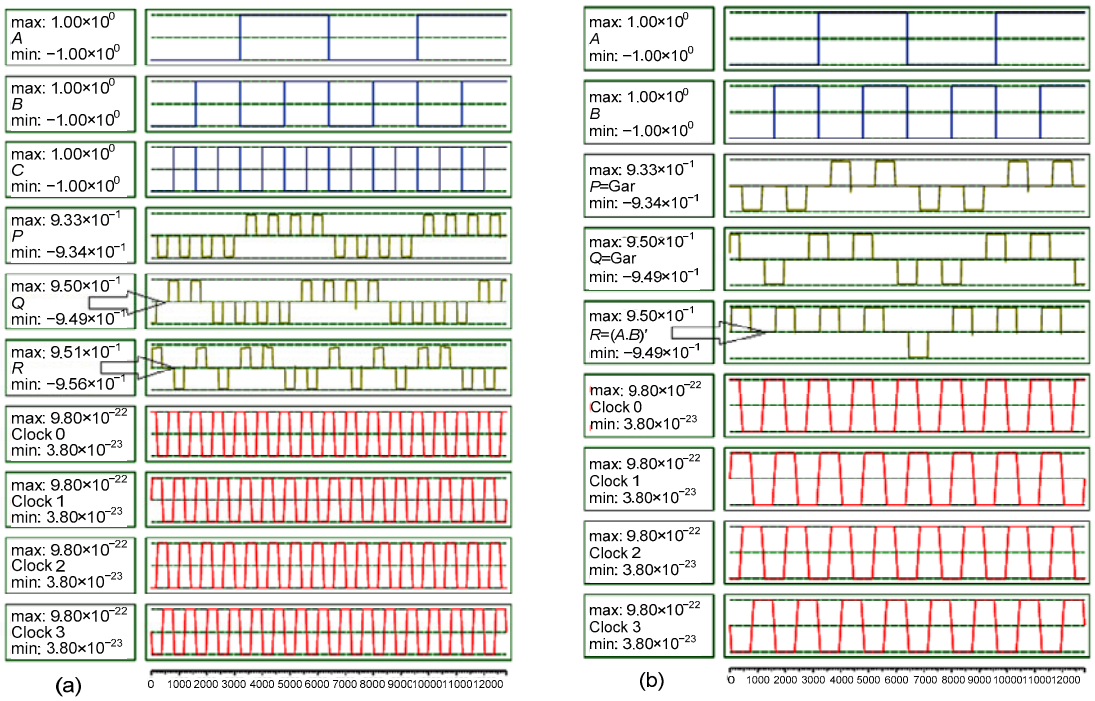

Fig. 16 Simulation results of the reversible QCA DG gate (a) and reversible QCA NAND gate (b)
The arrow indicates that the output would appear after the first clock pulse

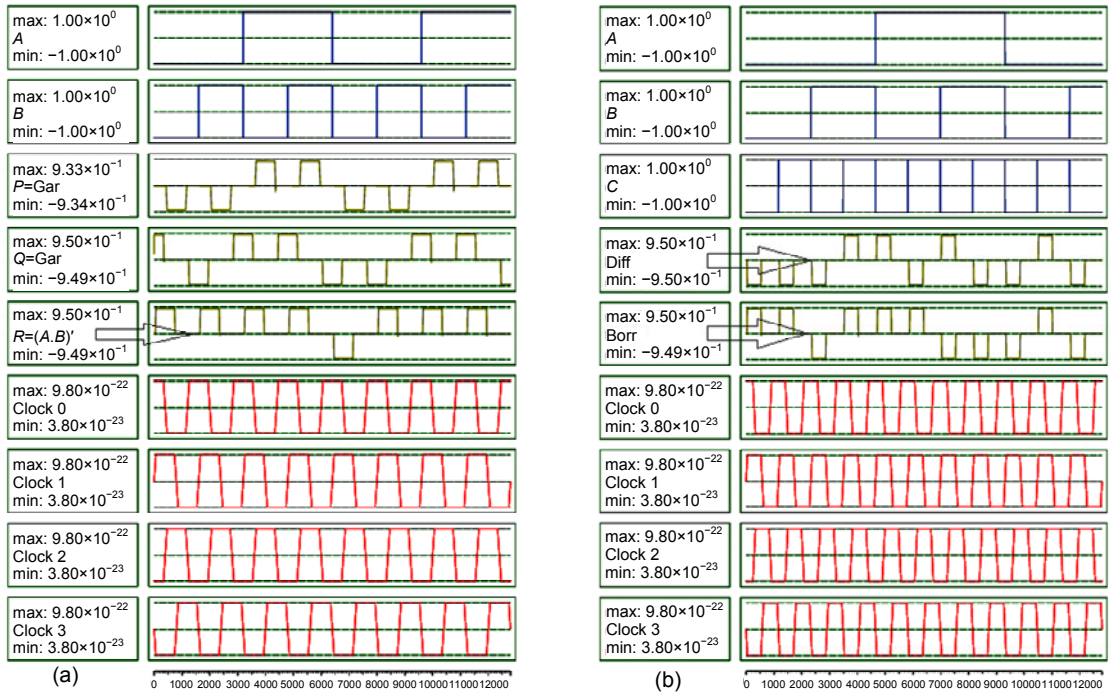

Fig. 17 Simulation results of the reversible half-subtractor (a) and reversible full-subtractor (b)

In (a) the arrow shows that the output for Borr and Diff appears after the first clock pulse; in (b) the arrows show that the difference bit and corresponding borrow bit appear at the third clock pulse

7 MVs, latency of 1.0, 123 or 125 cells, and 103 680 nm² area. The full-subtractor is made using only 14 MVs, 12 inverters, with a latency of 2.0, 247 cells, and 256 608 nm² area.

5.6 Quantum cost of the proposed reversible circuit

The proposed reversible NAND gate and reversible half-subtractor are both made up of only one DG gate, whereas the reversible full-subtractor is composed of two DG gates. Thus, the quantum cost of the reversible NAND gate and reversible half-subtractor will be five (5×1). The quantum cost of the reversible full-subtractor will be 10 (5×2) (Table 6).

5.7 Comparison of the proposed design with those in prior work

The proposed reversible half-subtractor has 16.66% less quantum cost than an existing circuit (Thapliyal *et al*., 2005; Thapliyal and Ranganathan, 2009b) (Table 7). In contrast, the proposed reversible full-subtractor has 41.17% and 16.66% less quantum cost than those proposed by Thapliyal *et al*. (2005) and Thapliyal and Ranganathan (2009b), respectively (Table 8). Similarly, the comparison with respect to garbage values and the required number of reversible gates has been performed.

5.8 Quantum cost of the QCA layout of the proposed reversible circuit

Table 9 shows the quantum cost of the proposed reversible QCA circuit. The QCA layouts of the DG gate, reversible NAND gate, and reversible half-subtractor have the same quantum cost, i.e., 0.104. The quantum cost of the reversible full-subtractor is 1.028.

5.9 Conventional design and QCA-based design

Table 10 illustrates the quantum cost of the traditional design and QCA-based design. The traditional design of the DG gate, reversible NAND gate, and reversible half-subtractor each has a quantum cost of 5, whereas in QCA design, it is 0.104. For the reversible full-subtractor, the values are 10 and 1.028, respectively. The comparison shows that the implementation of QCA has a very low quantum cost compared to the traditional approach. This reflects that the QCA-based design is cost-effective.

Table 5 Circuit complexity

Proposed QCA circuit	Number of MVs and inverters used	Number of QCA cells	Total area (nm^2)	Cell area (nm^2)	Area usage (%)	Latency (clock cycle)
DG gate	7 MVs, 6 inverters	123	103 680	39 852	38.43	1.0
NAND gate	7 MVs, 7 inverters	123	103 680	39 852	38.43	1.0
Half-subtractor	7 MVs, 5 inverters	125	103 680	40 500	39.06	1.0
Full-subtractor	14 MVs, 12 inverters	247	256 608	80 028	31.18	2.0

Table 6 Quantum cost of the proposed reversible building blocks

Proposed reversible circuit	Number of DG gates	Quantum cost	Garbage value	Constant input
DG gate	–	5	–	–
NAND gate	1	5	2	1
Half-subtractor	1	5	1	1
Full-subtractor	2	10	2	1

Table 7 The proposed reversible half-subtractor and existing circuit

Reversible half-subtractor	Number of reversible gates	Quantum cost	Garbage value
Proposed circuit	1	5	1
Existing circuit (Thapliyal *et al*., 2005)	2 (50%)	6 (16.66%)	3 (66.66%)
Existing circuit (Thapliyal and Ranganathan, 2009b)	1 (0%)	6 (16.66%)	1 (0%)

Values in the brackets are improvements of the proposed circuit compared to the respective existing circuit

Table 8 The proposed reversible full-subtractor and existing circuit

Reversible full-subtractor	Number of reversible gates	Quantum cost	Garbage value
Proposed circuit	2	10	2
Existing circuit (Thapliyal *et al*., 2005)	5 (60%)	17 (41.17%)	9 (77.77%)
Existing circuit (Thapliyal and Ranganathan, 2009b)	2 (0%)	12 (16.66%)	2 (0%)

Values in the brackets are improvements of the proposed circuit compared to the respective existing circuit

Table 9 Quantum cost of the proposed reversible QCA circuit

Proposed QCA circuit	Area (μm^2)	Latency (clock cycle)	Quantum cost (area×latency^2)
DG gate	0.104	1.0	0.104
NAND gate	0.104	1.0	0.104
Half-subtractor	0.104	1.0	0.104
Full-subtractor	0.257	2.0	1.028

Table 10 Quantum cost of the traditional design and QCA-based design

Proposed reversible circuit	Quantum cost	
	Traditional	QCA
DG gate	5	0.104
NAND gate	5	0.104
Half-subtractor	5	0.104
Full-subtractor	10	1.028

5.10 Proposed QCA DG gate and existing reversible QCA gate

We have compared the proposed QCA DG gate with existing ones, including the QCA Feynman gate, TR gate, Peres gate, and Fredkin gate, in terms of area, latency, and QCA logic gate (Table 11). The complexity of the proposed QCA DG gate is higher than those of most existing reversible QCA gates. This is because more MVs and inverters are required to implement the QCA DG gate in our proposed gate.

5.11 Fault analysis of the proposed QCA layout of the DG gate

The stuck-at-fault analysis of the proposed DG gate is demonstrated here. Single stuck at fault and multiple stuck at fault have been considered to perform the analysis. To achieve 100% fault coverage simulation, the results are analyzed and the set of minimal test vectors is produced (Ma *et al*., 2009).

Table 12 shows the fault pattern of the DG gate. The test vector set <000, 111> has a fault coverage of 42.86%, and the test vector set <010, 100> has a fault coverage of 57.14%. Thus, the test vector set <000, 111, 010, 100> has a 100% fault coverage. The same test vector set can be employed to perform stuck-at-fault analysis for the proposed subtractors.

5.12 Defect analysis of the proposed QCA DG gate

The analysis is performed for missing/additional QCA cells (Sen *et al*., 2014). To detect possible faults for missing/additional cells, all the cells of different

Table 11 Proposed QCA DG gate and existing reversible QCA gates

Reversible QCA circuit	Number of MVs and inverters used	Number of QCA cells	Total area (μm^2)	Cell area (μm^2)	Area usage (%)	Latency
Proposed DG gate	7 MVs, 6 inverters	123	0.104	0.040	38.43	1.00
Feynman gate (Das and De, 2016a)	3 MVs, 2 inverters	43	0.038	0.014	36.84	0.75
Feynman gate (Debnath *et al*., 2017)	3 MVs, 2 inverters	54	0.037	0.017	46.15	0.75
TR gate (Akter *et al*., 2015)	7 MVs, 4 inverters	113	0.200	0.045	22.50	1.00
TR gate (Bahar *et al*., 2015)	6 MVs, 5 inverters	68	0.079	0.027	34.18	0.75
Fredkin gate (Das and De, 2016c)	6 MVs, 2 inverters	60	0.043	0.020	45.45	0.75
Fredkin gate (Das and De, 2016b)	6 MVs, 2 inverters	88	0.098	0.035	35.71	0.75
Toffoli gate (Das and De, 2016c)	4 MVs, 2 inverters	46	0.036	0.015	41.81	1.00
Peres gate (Abdullah-Al-Shafi, 2016)	7 MVs, 4 inverters	96	0.105	0.039	37.14	0.75
Peres gate (Das and De, 2016c)	7 MVs, 4 inverters	85	0.068	0.028	40.47	1.00
RUG gate (Das *et al*., 2016c)	7 MVs, 4 inverters	106	0.086	0.035	40.15	1.00
NFT gate (Bahar *et al*., 2015)	9 MVs, 3 inverters	128	0.142	0.051	35.91	0.50
BVU gate (Bahar *et al*., 2015)	6 MVs, 4 inverters	82	0.100	0.033	33.00	0.50

Table 12 Fault analysis of the DG gate

I/O	Fault type	Test vector (*ABC*)	Expected output (*PQR*)	Faulty output (*PQR*)
Single stuck at fault				
A	Stuck at 0	111	111	001
A	Stuck at 1	000	010	101
B	Stuck at 0	111	111	100
B	Stuck at 1	000	010	000
C	Stuck at 0	111	111	110
C	Stuck at 1	000	010	011
P	Stuck at 0	111	111	001
P	Stuck at 1	000	010	101
Q	Stuck at 0	111	111	100
Q	Stuck at 1	000	010	000
R	Stuck at 0	111	111	110
R	Stuck at 1	000	010	011
Multiple stuck at fault				
AB	Stuck at 0	100	101	010
AB	Stuck at 1	100	101	110
BC	Stuck at 0	010	000	010
BC	Stuck at 1	010	000	001
AC	Stuck at 0	100	101	010
AC	Stuck at 1	100	101	100
PQ	Stuck at 0	100	101	010
PQ	Stuck at 1	100	101	110
QR	Stuck at 0	010	000	010
QR	Stuck at 1	010	000	001
PR	Stuck at 0	100	101	010
PR	Stuck at 1	100	101	100
ABC	Stuck at 0	010	000	010
ABC	Stuck at 1	010	000	111
PQR	Stuck at 0	100	101	010
PQR	Stuck at 1	100	101	111

layers of the DG gate are marked according to their grid positions (Fig. 18). For example, in layer 1, the cell just to the right side of input cell *C* is marked as *D*3, i.e., *D*th row and 3rd column. To perform this analysis, the proposed QCA DG gate has been simulated on QCADesigner for each single missing/additional cell. From the simulation results, all possible single missing cell-based faults are characterized and outlined in Table 13. For example, for the missing cell at position *A*6, the output is 010. To detect this kind of fault, the test vector 001 can be employed. For test vector 001, the expected output is 011. Thus, comparing the mismatch in the parity bit between the expected output 011 and faulty output 010, the fault for the missing cell at position *A*6 can be detected. Similarly, the faults for other missing cells can be detected by applying suitable test vectors.

All of the possible single additional cell based defects of the proposed QCA DG gate have been characterized in Table 14. For example, if an extra cell is added at position *A*13, the faulty output 010 will be produced. The test vector 001 can be employed to identify the parity mismatch between expected output 011 and faulty output 010. Similarly, the fault for other additional cells can be detected by applying suitable test vectors.

The same procedure can be applied to achieve the defects due to a single missing/additional cell for the proposed subtractors.

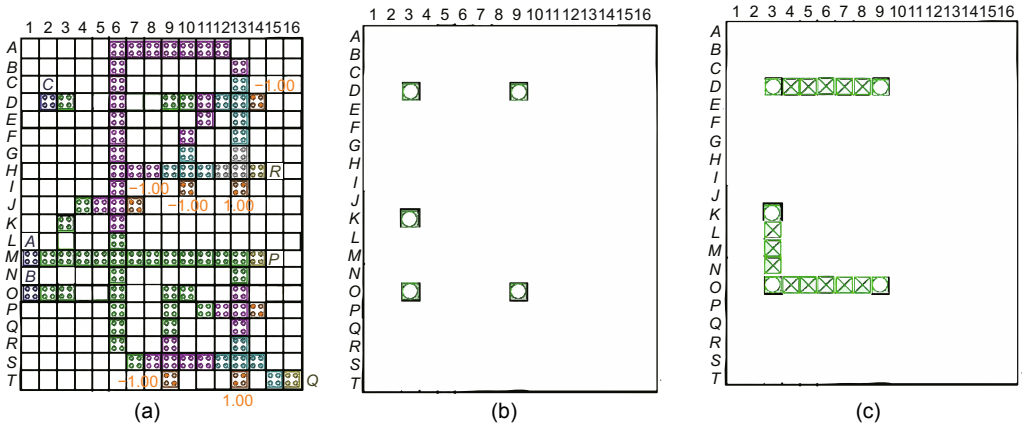

Fig. 18 Different layers of the proposed QCA circuit of the DG gate: (a) layer 1; (b) layer 2; (c) layer 3

Table 13 Fault characterization due to a missing cell

Missing cell position	Test vector (*ABC*)	Expected output (*PQR*)	Faulty output (*PQR*)	Missing cell position	Test vector (*ABC*)	Expected output (*PQR*)	Faulty output (*PQR*)
Layer 1				Layer 1			
*A*6–*A*8, *A*12, *B*6, *B*13	001	011	010	*O*2–*O*3, *O*9–*O*19, *O*13	011	001	011
*A*9–*A*11		Fault free		*P*9, *P*11–*P*12, *Q*9	011	001	011
*C*6, *C*13, *D*3	011	001	000	*Q*13, *S*9–*S*11	000	010	000
*D*6, *D*13, *E*13	000	010	011	*R*6, *R*9, *R*13, *S*7, *S*8	011	001	011
*D*9–*D*12	001	011	010	*S*12	001	011	001
*E*6, *E*11, *F*6	011	001	000	*S*13–*S*14, *T*15	011	001	011
*F*10, *G*10, *H*6–*H*9	100	101	100	Layer 2			
*F*13, *G*13, *H*10–*H*12, *J*6	000	010	011	*D*3	001	011	010
*G*6	011	001	000	*D*9	000	010	011
*H*13, *I*6, *J*4–*J*5	100	101	100	*K*3	100	101	100
*K*3, *K*6, *L*6	100	101	100	*O*3, *O*9	011	001	011
*M*2–*M*5	000	010	101	Layer 3			
*M*6	000	010	011	*D*3, *K*3, *L*3, *N*3	000	010	011
*M*7–*M*11	000	010	100	*D*4–*D*8	001	011	010
*M*12, *N*6, *O*6, *P*6, *Q*6		Fault free		*D*9	000	010	011
*M*13, *P*13	000	010	000	*M*3		Fault free	
*N*13	100	101	111	*O*3–*O*9	011	001	011

Table 14 Fault characterization due to an additional cell

Additional cell position	Test vector (*ABC*)	Expected output (*PQR*)	Faulty output (*PQR*)	Additional cell position	Test vector (*ABC*)	Expected output (*PQR*)	Faulty output (*PQR*)
*A*13, *C*14	001	011	010	*O*11, *P*10	010	000	010
*E*10, *F*11, *I*11, *I*7	100	101	100	*Q*14	100	101	111
*J*3	111	111	110	*R*7, *S*6	010	000	010
*K*4, *K*7	100	101	100	*S*15	001	011	001
*L*5, *L*7	101	100	101	*T*10	010	000	010
*N*8	111	111	101	*T*14	101	100	110
*N*9, *N*10	010	000	010				

6 Conclusions

In this paper, a new reversible binary subtractor has been achieved through QCA technology. The simulation results demonstrate that all the circuits work efficiently and produce proper results. The proposed circuits are optimized and more cost effective than the state-of-the-art circuits. QCA-based design of reversible circuits has a lower quantum cost than traditional design. The defect analysis is useful for fault-free implementation of the designs. The proposed reversible subtractors can be useful in achieving nanoscale, faster, dedicated units of the subtractor for digital signal processing for nano-communication. The proposed circuit can also be used as a future implementation of a QCA nano processor and quantum computers. This work can be considered an important contribution to the QCA-based reversible logic community, along with design and implementation of binary subtractors.

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