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# Two-step gate-recess process combining selective wet-etching and digital wet-etching for InAlAs/InGaAs InP-based HEMTs*

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**Abstract:** A two-step gate-recess process combining high selective wet-etching and non-selective digital wet-etching techniques has been proposed for InAlAs/InGaAs InP-based high electron mobility transistors (HEMTs). High etching-selectivity ratio of InGaAs to InAlAs material larger than 100 is achieved by using mixture solution of succinic acid and hydrogen peroxide ($H_2O_2$). Selective wet-etching is validated in the gate-recess process of InAlAs/InGaAs InP-based HEMTs, which proceeds and automatically stops at the InAlAs barrier layer. The non-selective digital wet-etching process is developed using a separately controlled oxidation/de-oxidation technique, and during each digital etching cycle 1.2 nm InAlAs material is removed. The two-step gate-recess etching technique has been successfully incorporated into device fabrication. Digital wet-etching is repeated for two cycles with about 3 nm InAlAs barrier layer being etched off. InP-based HEMTs have demonstrated superior extrinsic transconductance and RF characteristics to devices fabricated during only the selective gate-recess etching process because of the smaller gate to channel distance.

**Key words:** High electron mobility transistors (HEMTs); Gate-recess; Digital wet-etching; Selective wet-etching
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## 1 Introduction

InP-based high electron mobility transistors (HEMTs) have demonstrated high frequency, low noise, and high gain performances, due to high sheet carrier density, high peak drift velocity, and high electron mobility in the InGaAs channel region. Consequently, they have become significantly competitive candidates for various high speed circuits (Zhong *et al*., 2015; Varonen *et al*., 2016), millimeter-wave systems (Reck *et al*., 2016), and even THz applications (Deal *et al*., 2011a; 2014; Rodwell, 2014; Leong *et al*., 2015). These remarkable device performances are attributed mainly to the progress in epitaxial and manufacture technology, especially the gate-recess process. Both lateral width and vertical depth of gate-recess are decisive factors to device performances by impacting various parameters, including parasitic capacitance and resistance, carrier concentration, and modulation capability of gate voltage. An inappropriate gate-recess process, however, may cause large gate-leakage currents and an anomalous phenomenon like kink effect in DC characteristics (Zhong *et al*., 2012a).

It is well-known that the InAlAs/InGaAs heterojunction structure without the InP etching-stopping layer is a very attractive option for InP-based HEMT

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to obtain high gain and good frequency performances. Usually, the thicknesses of InGaAs cap and InAlAs barrier layers are merely several dozens of nanometers. Therefore, good selectivity is necessary to make gate-recess etching stop automatically at the InAlAs barrier layer, and only then can the gate electrode be placed directly on the barrier layer. Additionally, good selectivity prompts the uniformity of device parameters for different process-batches, such as drain-source current ($I_{DS}$), pinch-off voltage ($V_p$), transconductance, and frequency performances. Consequently, high selective wet-etching should be adopted in the gate-recess process of InAlAs/InGaAs InP-based HEMTs. Many excellent InAlAs/InGaAs InP-based HEMTs have been reported using selective gate-recess etching, e.g., the current gain cutoff frequency ($f_T$) of 610 GHz, the maximum oscillation frequency ($f_{max}$) of 1.5 THz for 30 nm InP HEMTs (Deal *et al*., 2011b) and $f_T$=600 GHz, $f_{max}$=1.5 THz for 25 nm InP HEMTs (Mei *et al*., 2015). However, the distance between the gate and the channel is determined only by the thickness of the InAlAs barrier layer in the high selective gate-recess etching process. Thus, alternative non-selective digital wet-etching is intensely required to further improve the flexibility and controllability of the fabrication process.

Ordinarily, the wet-etching process combines oxidation and de-oxidation into a single chemical etching system. The non-selective digital wet-etching process is based on the idea of separately controlling oxidation and de-oxidation chemical reactions; i.e., the two chemical reactions are separated into two distinct processes (Cao *et al*., 2004). The first oxidation step forms a fixed depth of surface oxide film due to the self-limiting nature of surface oxidation. The second de-oxidation step is to remove the newly formed surface oxide film. Thus, the etching depth is dependent on the diffusion limited thickness of the surface oxidation layer, which is not directly related to the length of time for the sample being exposed to the de-oxidation solution. In this manner, a stable etching depth can be obtained by repeating these two steps. Nonetheless, it is a time-consuming and tedious process to remove material layers with several dozens of nanometers only by non-selective digital wet-etching.

In this paper, a two-step gate-recess process, in which high selective wet-etching and non-selective digital wet-etching techniques are coupled, is proposed for InAlAs/InGaAs InP-based HEMTs. High selective wet-etching is developed to get rid of InGaAs cap material under the gate region till the InAlAs barrier layer, and the lateral gate-recess width can be optimized by controlling the etching time. Moreover, the non-selective digital wet-etching process is developed and incorporated into the fabrication of InP-based HEMTs. Consequently, InP-based HEMTs have demonstrated superior extrinsic transconductance and radio frequency (RF) characteristics to devices obtained just during the selective gate-recess etching process.

## 2 Device structure

Fig. 1 shows a cross-sectional schematic of the InAlAs/InGaAs InP-based HEMT. The epitaxial structure is designed and optimized with the parameters listed in Table 1. The layers consist of an InAlAs buffer, an InGaAs channel, an unstrained InAlAs spacer layer, a Si-doping plane which provides two-dimensional electron gas (2DEG), a 12 nm unstrained lnAlAs Schottky barrier layer, and a composite InGaAs cap layer consisting of a heavily Si-doped $In_{0.6}Ga_{0.4}As$ cap layer with a narrow band-gap, and a Si-doped $In_{0.53}Ga_{0.47}As$ transition layer. The composite cap layers are designed to improve ohmic contact characteristics. All InAlAs layers are lattice matched with the InP substrate.

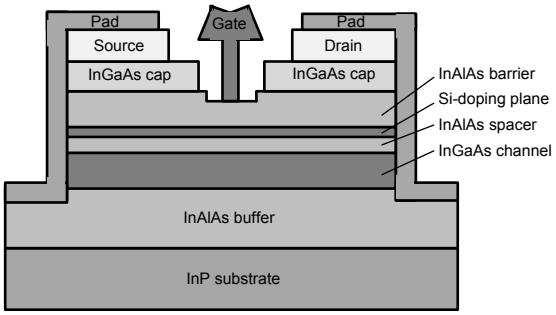


**Fig. 1 Cross-sectional schematic of InAlAs/InGaAs InP-based HEMT**

## 3 Gate-recess process

### 3.1 High selective wet-etching technique

The etching process of arsenide compound can be divided into oxidation and de-oxidation steps.

**Table 1 Parameters of device epitaxial layer structure***

| Layer | Material | Doping | Thickness (nm) |
|---|---|---|---|
| Cap layer | $In_{0.6}Ga_{0.4}As$ | $Si:N^{++}$ $3\times10^{19}$ $cm^{-3}$ | 15 |
| Cap layer | $In_{0.53}Ga_{0.47}As$ | $Si:N^{+}$ $5\times10^{18}$ $cm^{-3}$ | 15 |
| Barrier layer | $In_{0.52}Al_{0.48}As$ | Undoped | 12 |
| Si-doping plane | – | $5\times10^{12}$ $cm^{-2}$ | – |
| Spacer layer | $In_{0.52}Al_{0.48}As$ | Undoped | 3 |
| Channel | $In_{0.53}Ga_{0.47}As$ | Undoped | 15 |
| Buffer layer | $In_{0.52}Al_{0.48}As$ | Undoped | 500 |
| Substrate | InP | – | – |

* See Fig. 1

Therefore, InAlAs/InGaAs etching can be performed by using an aqueous mixture of hydrogen peroxide ($H_2O_2$) and organic acid, such as succinic acid and citric acid. Based on experience, the etching rate and selectivity are dependent closely on the composition and PH value of the solution. In this study, the mixture solution of succinic acid and $H_2O_2$ was adopted to remove the InGaAs cap layer without destroying the InAlAs barrier layer. Succinate powder was dissolved into 50 mL de-ionized water till saturation. $H_2O_2$ was then added to make the proportion ratio be 5:1 with the saturated succinic acid solution. The PH value of the solution was adjusted to 5 by adding ammonium hydroxide solution ($NH_4OH$).

The InGaAs/InP and InAlAs/InP samples were lithographic with resist lines as mask protection, and then they were simultaneously put into the prepared etchant for 5 min. Specifically, the etchant bath temperature was set as 20 °C to achieve a tradeoff between selectivity and roughness. The cross-section of the etched samples was observed by using a scanning electron microscope (SEM) (Fig. 2). The InGaAs/InP sample has exhibited a vertical etching depth of 306 nm and a horizontal etching width of 833 nm (Fig. 2a). The etching rate of InGaAs is about 61 nm/min. However, there is merely a slight corrosion sign for the InAlAs material (Fig. 2b). The etching selectivity ratio of InGaAs material to InAlAs material is more than 100 by this mixture solution. The low etching speed of InAlAs material is probably due to the formation of the aluminum oxide layer which behaves as an etching-stopper layer. Further study should be conducted to confirm this. Additionally, the etching rate of InGaAs material in the horizontal direction is found to be much higher than that in the vertical direction owing to the weak interface between resist and surface.

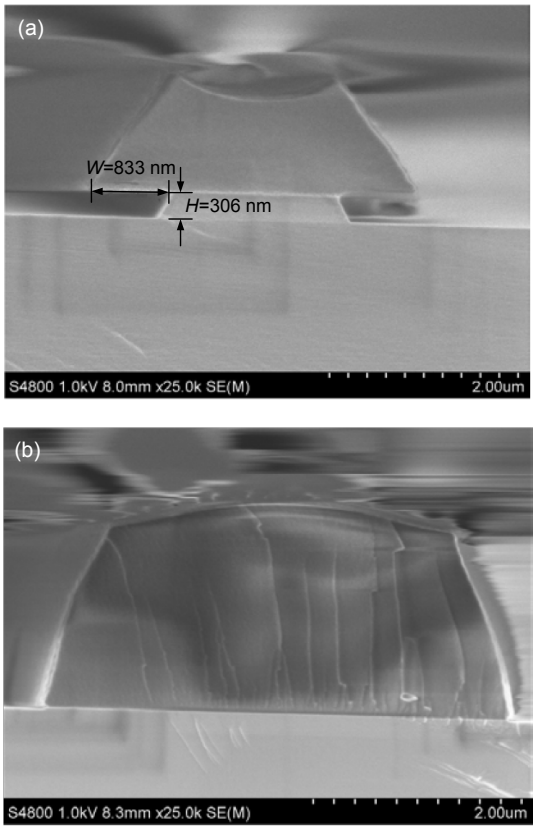


**Fig. 2 The SEM photography of cross-sectional samples after high selective wet-etching for 5 min: (a) InGaAs/InP sample; (b) InAlAs/InP sample**

Selective wet-etching was confirmed in the gate-recess process of InAlAs/InGaAs InP-based HEMTs, and the T-gate patterns with a near 100 nm gate-foot length were defined by electron beam lithography in a tri-layer of PMMA/Al/UVIII. Specifically, selective wet-etching was performed with a slight ultrasonic vibration to pump out intermediate products rapidly from the small gate-recess region. $I_{DS}$ was measured for different gate-recess etching durations of 0, 5, 15,

30, 60, 90, and 120 s with drain-source voltage ($V_{DS}$) changing from 0 to 2.5 V (Fig. 3). The $I_{DS}$ decreased initially with the thinning of cap layer from 0 to 30 s, and the value approximately kept constant for an etching duration larger than 30 s. A slight decrease trend can still be detected for the etching duration of 120 s, which can be caused by the slight etching of the InAlAs barrier layer. Basically, the gate-recess etching process will proceed and automatically stop at the InAlAs barrier layer, and the lateral gate-recess width can be optimized by controlling the etching time.

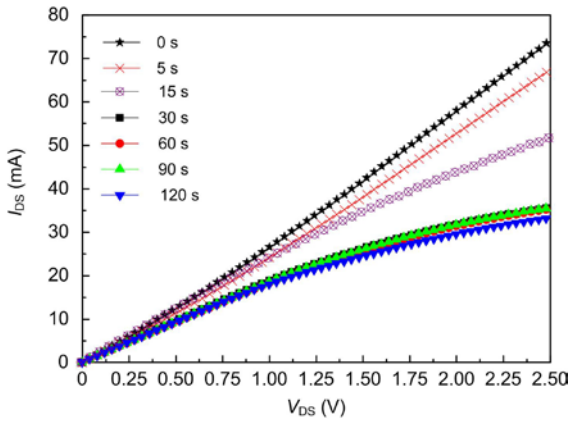


**Fig. 3 The drain-source current ($I_{DS}$) versus drain-source voltage ($V_{DS}$) for different gate-recess etching durations**

### 3.2 Digital wet-etching technique

As presented above, the non-selective digital wet-etching process is based on the idea of separately controlling oxidation and de-oxidation chemical reactions. Therefore, the two chemical reactions can be separated into two distinct processes. In the experiment, $H_2O_2$ was used as the oxidizing agent, and the mixed solution of phosphoric acid and water was adopted as the de-oxidation etchant with a composition of 1:10. At the start, resist mask of lines was formed on the InAlAs/InP epitaxial wafer. Then, the prepared sample was oxidized for 30 s, resulting in an oxide layer formed on the surface, which can prevent against further contact of the oxidizing agent with InAlAs material. Subsequently, the oxidized wafer was put into the phosphoric acid solution for 30 s, and the surface oxide layer would be removed without underneath layers being attacked. Specifically, a surface cleaning step must be performed between the two processing steps to avoid the cross-contamination of the two solutions. The oxidation and de-oxidation chemical reactions were repeated 50 times, and the cross-section of the etched sample has demonstrated a vertical etching depth of 62.8 nm and a horizontal etching width of 893 nm (Fig. 4). It can be concluded that an only about 1.2 nm InAlAs layer can be etched by each oxidation and de-oxidation cycle, which is decided by the diffusion limited thickness of oxidized InAlAs material for each oxidation process.

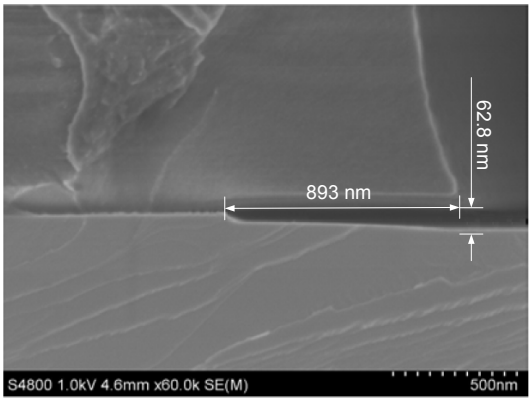


**Fig. 4 The cross-section of the InAlAs/InP sample after 50 digital wet-etching cycles**

## 4 Results and discussion

The two-step gate-recess process combining high selective wet-etching and non-selective digital wet-etching techniques has been successfully incorporated into the fabrication of InAlAs/InGaAs InP-based HEMTs. The device fabrication process is almost the same as in our previous study (Zhong *et al.*, 2012b). The lateral gate-recess width was optimized to be about 300 nm to obtain excellent RF characteristics and avoid kink effect by controlling the first-step selective gate-recess etching time. Subsequently, the digital wet-etching process of oxidation and de-oxidation chemical reactions was repeated twice, which etched off an about 3 nm InAlAs barrier layer. The extrinsic transconductance ($g_m$) and frequency performances were measured for InP-based HEMTs before and after the digital gate-recess etching process (Figs. 5 and 6). The gate-source voltage ($V_{GS}$) varied from −1.5 to 0.6 V in Fig. 5.

After second-step digital gate-recess etching, a distinct shift of $V_p$ toward positive value was observed from −0.5 to −0.3 V, together with the maximum transconductance ($g_{m,max}$) increasing from 765 to

909 mS/mm. The positive variation of $g_{m,max}$ and $V_p$ can be attributed to the increased channel modulation capability of gate voltage with a smaller gate to channel distance. However, the measured full channel current had an obvious decrease trend, from 591 to 570 mA/mm, because of the lower carrier concentration. As shown in Fig. 6, the frequency performance will surely improve with transconductance proportionally. Exactly, $f_T$ increases from 150 to 170 GHz, and $f_{max}$ changes from 201 to 240 GHz.

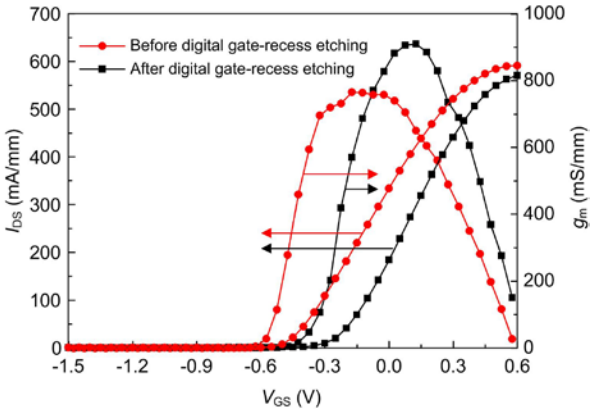


**Fig. 5 The transfer characteristic curves of InP-HEMTs before and after digital gate-recess etching**

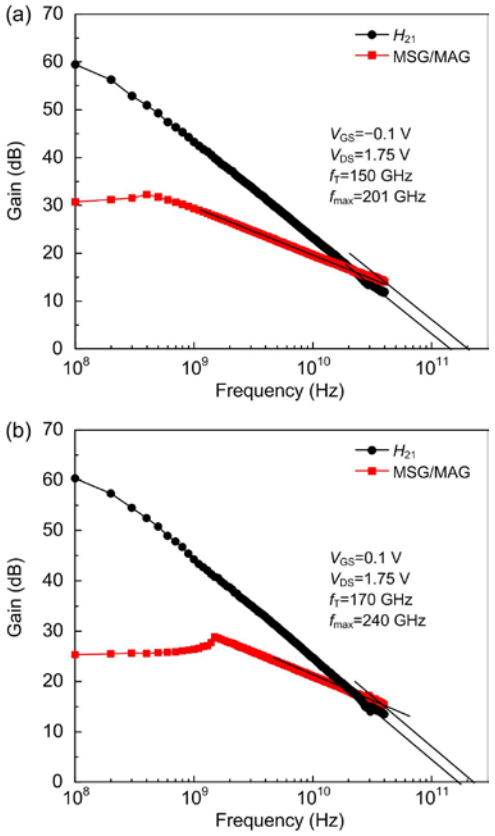


**Fig. 6 $H_{21}$ and MAG/MSG versus the frequency of InP-based HEMTs before (a) and after (b) digital gate-recess etching**

## 5 Conclusions

In this paper, a two-step gate-recess process which combines high selective wet-etching and non-selective digital wet-etching techniques has been proposed for InAlAs/InGaAs InP-based HEMTs. High selective wet-etching is developed to get rid of the InGaAs cap material without influencing the InAlAs barrier layer, and the etching selectivity ratio of InGaAs material to InAlAs material has exceeded 100 by using the mixture solution of succinic acid and $H_2O_2$. The lateral gate-recess width can be optimized by controlling the etching time to gain excellent RF characteristics and avoid kink effect. Moreover, the non-selective digital wet-etching process is developed using a separately controlled oxidation/de-oxidation technique, and during each digital etching cycle 1.2 nm InAlAs material is removed. The two-step gate-recess etching technique has been successfullly incorporated into InP-based HEMTs fabrication. InP-based HEMTs have demonstrated superior extrinsic transconductance and RF characteristics to devices obtained just by the selective gate-recess etching process.

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