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A multi-modular shunt active power filter system and its novel fault-tolerant strategy based on split-phase control and real-time bus communication*

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Abstract: We first present a new multi-modular shunt active power filter system suitable for large-capacity compensation. Each module in the system has the same circuit topology, system functionality, and controller design, to achieve coordination control among the modules. The module's reference signals are obtained by multiplying the total reference signal by the respective distribution coefficient. Next, a novel fault-tolerant approach is proposed based on split-phase control in the *a*-*b*-*c* frame and real-time bus communication. When a phase fault occurs, instead of halting the whole module, the proposed strategy isolates only the faulted bridge arm, and then recalculates the distribution coefficients and transfers the compensation capacity to the same phases of the other normal modules, resulting in a continuous operation of the faulted module and optimization of the remaining usable power devices. Through steady-state analysis of the post-fault circuit, the system stability and control reliability are proven to be high enough to guarantee its engineering application value. Finally, a prototype is established and experimental results show the validity and feasibility of the proposed multi-modular system and its fault-tolerant control strategy.

Key words: Shunt active power filter; Fault-tolerant topology; Split-phase control; Bus communication
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1 Introduction

With the wide application of power electronic devices, problems in power quality are becoming increasingly serious. Some effective measures must be implemented to improve power quality. A shunt active power filter (SAPF) is a preferred solution for not only its compensation for reactive and harmonic currents drawn by distorting and nonlinear loads, but also its suppression of neutral line current initiated by an unbalanced load (Akagi, 2005; Sun et al., 2015; Guzman et al., 2016). However, an SAPF has the disadvantages of high cost and an unstable reliability. The capacity problem also restricts its development (Khadem et al., 2014).

For large-capacity harmonic compensation, there are several methods including hybrid APF, adopting a multilevel topology, or applying multiple circuit techniques. The preeminent advantage of hybrid APFs is the reduction in active part capacity, which is suitable for high-voltage large-capacity conditions. However, the cooperation between the active and passive parts increases the complexity of the control strategy, and the design of the passive part depends on the specific application, leading to a lack of universality (Bhattacharya et al., 2012; Lee et al., 2015). Multilevel topology has been widely used in high-voltage reactive power compensation (Lim and

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Azli, 2007). For an SAPF, a diode-clamping three-level topology is the most frequently used structure in industrial applications. Due to the limitations of semiconductor power devices, this kind of topology is applicable for only small power capacity situations. The multiple circuit technique can not only decrease the power loss by improving the equivalent switching frequency, but also reduce the output harmonics to optimize the compensation performance. However, this approach has some defects that hinder its development in the APF field, such as poor dynamic response, complicated coordination among modules, and a lack of redundancy (Chen et al., 2012). Comparatively speaking, the multi-modular parallel technique can achieve a combination control for the whole system and guarantee the independence and redundancy for each module (Wang et al., 2015).

Large-capacity multi-modular SAPFs usually adopt insulated gate bipolar transistor (IGBT) as the power device, which always works at a high frequency and in high-temperature conditions so that the power semiconductor and its control circuit are prone to faults (Sjolte et al., 2014). However, in some applications, the continuous operation of a multi-modular SAPF system is of great importance and must be ensured. This is particularly the case in military, aerospace, and manufacturing industries, which are increasingly adopting SAPF to improve the overall system efficiency and performance. Once the SAPF system stops running, the power quality will deteriorate instantaneously and some safety-critical devices such as steering, fuel pumps, and electric arc furnace will no longer operate normally and thus potential safety hazard will exist.

In recent years, the need for these fault-tolerant systems has inspired many researchers, and various types of inverter circuits and control strategies have been proposed, trying to create systems that are tolerant to one or more types of faults (Karimi et al., 2009; Naidu et al., 2010; Errabelli and Mutschler, 2012; Gou et al., 2016; Zhou et al., 2016). However, most works focused on the fault tolerance of single-module, three-phase AC motor drives, rather than multi-modular SAPF systems. The significant differences between motor drives and SAPFs are crucial because they mean that the direct use of some existing techniques will lead to unexpected problems, such as the injection of zero-sequence currents into a three-phase SAPF in which the neutral point is connected, and the lack of a load neutral point when applying the three-phase four-leg fault-tolerant topology to achieve redundancy.

In addition, most existing studies just attempt to achieve fault tolerance inside a single module, which means that the specific characteristics of multi-modular SAPF systems are not considered. The advantages of structural consistency and functional compatibility among modules are not fully exploited. It is a goal of this study to contribute to the systematic analysis of multi-modular SAPF systems, which will support the development of a fault-tolerant SAPF system to extend the redundancy from internal fault tolerance to mutual fault tolerance.

2 Configuration and working principle of a multi-modular SAPF system

The configuration of the multi-modular SAPF system adopted in this study is shown in Fig. 1. The whole system consists of a centralized monitoring unit and N identical modules, meaning that the circuit topology, control system, and functionality of all the modules are completely the same. Note that i_s, i_L, and $i_{C,j}$ are the grid current, load current, and compensation current of module j respectively, i_o is the neutral current, u_s is the grid voltage, v_{dc1} and v_{dc2} are the voltages of two split capacitors respectively, v_{dc} is the total DC-link voltage, and L_1, L_2, C_f, and R_d are the inverter side inductor, grid side inductor, filter capacitor, and damping resistance, respectively.

The module control system consists of a sampling unit, a digital signal processor (DSP) based controller, and a communication unit. The sampling unit samples the instantaneous values of the load currents, grid currents, grid voltages, output currents, and DC-link voltage, and implements adjustments to meet the requirements of the DSP input. The DSP controller carries out the detection of load harmonics, tracking of reference signals, and modulation of drive signals, and deals with various faults. The communication unit executes the RS485 communication with the system monitor.

The working principle of the whole system is such that the monitoring unit detects the operating states of all modules through the RS485 bus and

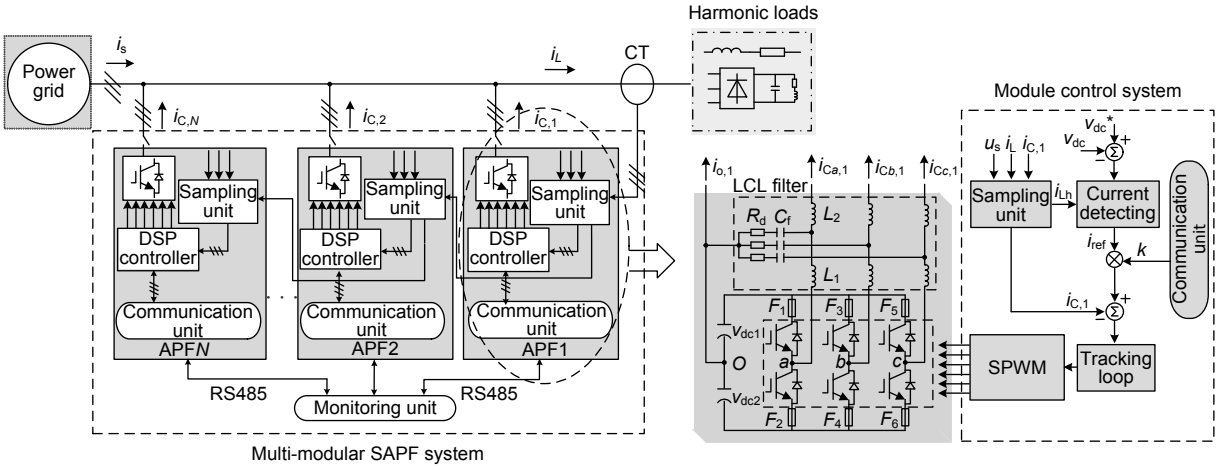

Fig. 1 Configuration of the multi-modular shunt active power filter (SAPF) system

transmits a specific distribution coefficient k_j (j=1, 2, …, N) to all modules by the broadcast mode. Each module extracts the harmonic currents after sampling the load current. Then each module's reference signal can be obtained by multiplying the harmonic currents by the respective coefficient k_j. Then the controller delivers the reference signal to the current tracking unit and the modulation unit generates the pulse width modulation (PWM) signals for the IGBTs. Once one module quits or breaks down, the coefficient k_j will be renewed and the remaining modules will adjust their compensation capacities to suppress the load harmonics as much as possible.

Fig. 2 presents the mechanism for compensation capacity allocation. The monitoring unit acts as a bus master and provides instructions to the bus slavers. Inside a single module, the DSP controller contains two TMS320F2812 chips. DSP1 receives the revised parameters from DSP2 and runs the main loop program. DSP2 takes charge of uploading the module states to the monitor and receiving the distribution coefficient from the monitor. The program flow diagrams of DSP1 and DSP2 are illustrated in Figs. 3 and 4, respectively.

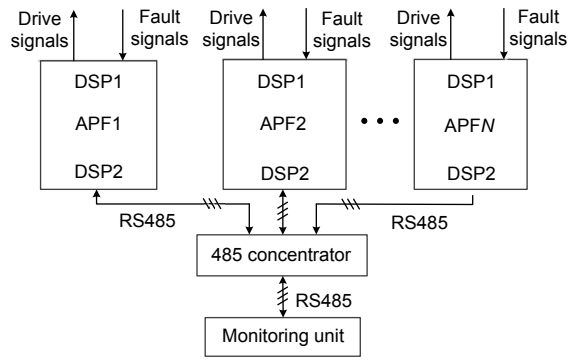

Fig. 2 Mechanism for the compensation capacity allocation

The coefficient calculation process is analyzed as follows. According to Kirchhoff's current law (KCL), it can be derived that

$$i_{\mathrm{s}} = i_{\mathrm{L}} - i_{\mathrm{C}} = i_{\mathrm{L1}} + i_{\mathrm{Lh}} - \sum_{j=1}^{N} i_{\mathrm{C},j}, \tag{1}$$

where i_{L1} and i_{Lh} are the fundamental component and harmonic components of the load current, respectively.

Assuming that the detecting unit and tracking unit of the controller work ideally, to make the waveform of the grid current close to be sinusoidal, the system needs characteristically to satisfy the following condition:

$$\begin{aligned}\sum_{j=1}^{N} i_{\mathrm{C},j} &= i_{\mathrm{C},1} + i_{\mathrm{C},2} + \cdots + i_{\mathrm{C},N} = i_{\mathrm{ref},1} + i_{\mathrm{ref},2} + \cdots + i_{\mathrm{ref},N} \\ &= k_1 \cdot i_{\mathrm{Lh}} + k_2 \cdot i_{\mathrm{Lh}} + \cdots + k_N \cdot i_{\mathrm{Lh}} = i_{\mathrm{Lh}}.\end{aligned} \tag{2}$$

It can be deduced from Eq. (2) that

$$k_1 + k_2 + \cdots + k_N = 1. \tag{3}$$

Note that the value of k_j determines the compensation capacity of module j. To avoid the situation where some modules always reach their full

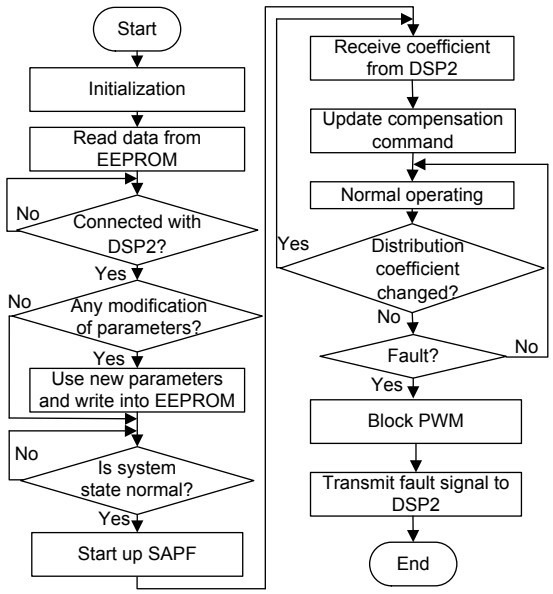

Fig. 3 DSP1 program flow diagram

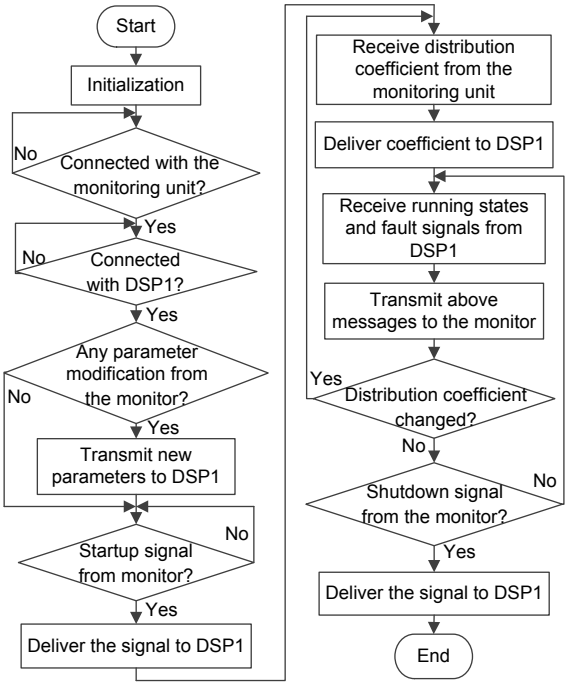

Fig. 4 DSP2 program flow diagram

power capacity and reduce the difficulty in calculating and updating coefficients, an equalization control strategy is adopted, which divides the total compensation capacity equally into N pieces to make each module undertake an equivalent compensation mission. Thus, the coefficient k_j can be expressed as

$$k_1 = k_2 = \cdots = k_N = 1/N. \tag{4}$$

3 Fault-tolerant control strategy for a multi-modular SAPF system

Take the SAPF system with two modules as an example and perform the following analysis. The system structure is shown in Fig. 5. Under normal conditions, two modules operate independently and share the loads averagely. When a fault occurs (assuming that the lower IGBT of phase *a* module 2 breaks down), the conventional disposal method will block all the PWM signals and halt module 2. Then it makes module 1 output the double currents. This leads to the waste of usable phases *b* and *c* in module 2. Furthermore, by transferring the whole three-phase compensation capacity to module 1, the power dissipation and temperature rise in module 1 will increase sharply, which may cause some safety problems.

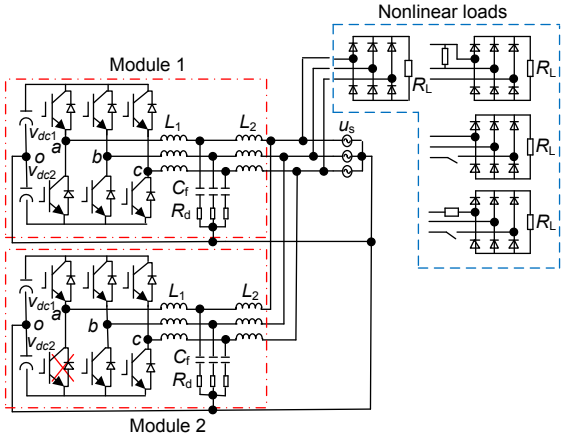

Fig. 5 Structure of the SAPF system with two modules

In this study, the characteristics mentioned for a multi-modular SAPF system are used and a novel fault-tolerant strategy is proposed, which uses the remaining power devices and maintains the continuous operation of a faulted module without adding any auxiliary component. The detailed process is as follows:

1. Extend the coefficient from k_j to $k_{a,j}$, $k_{b,j}$, and $k_{c,j}$, which means decoupling the three-phase compensation capacity allocation into three independent single-phase allocations.

2. Isolate the faulted phase (phase *a*) and just block the faulted phase's own PWM signal. The other two phases' PWM signals will still be under normal modulation.

3. Transmit the phase fault signal to the

monitoring unit by RS485 bus communication.

4. The monitoring unit figures out which phase has broken down according to the identification code. Then change the faulted phase's coefficient $k_{a,j}$ from $1/N$ to $1/(N-1)$ (N is 2 in this case), while the other two phases' coefficients ($k_{b,j}$ and $k_{c,j}$) remain the same as $1/N$.

5. Transmit the updated coefficients to each module by the broadcast mode in the next communication cycle.

6. After receiving the renewed coefficients, the remaining modules' compensation capacities for the faulted phase (phase a) will increase from $i_{\mathrm{Lh}a}/N$ to $i_{\mathrm{Lh}a}/(N-1)$, while the other two phase compensation capacities will have the same pre-fault values as $i_{\mathrm{Lh}b}/N$ and $i_{\mathrm{Lh}c}/N$, respectively.

Viewed from the grid side, the total three-phase output currents can be derived as follows:

$$\begin{aligned} i_{Ca} &= \sum_{j=1}^{N-1} i_{\mathrm{C}a,j} = i_{\mathrm{C}a,1} + i_{\mathrm{C}a,2} + \cdots + i_{\mathrm{C}a,N-1} \\ &= i_{\mathrm{ref}a,1} + i_{\mathrm{ref}a,2} + \cdots + i_{\mathrm{ref}a,N-1} \\ &= \sum_{j=1}^{N-1} k_{a,j} \cdot i_{\mathrm{Lh}a} = (N-1) \cdot \frac{1}{N-1} \cdot i_{\mathrm{Lh}a} = i_{\mathrm{Lh}a}, \end{aligned} \tag{5}$$

$$\begin{aligned} i_{Cb} &= \sum_{j=1}^{N} i_{\mathrm{C}b,j} = i_{\mathrm{C}b,1} + i_{\mathrm{C}b,2} + \cdots + i_{\mathrm{C}b,N} \\ &= i_{\mathrm{ref}b,1} + i_{\mathrm{ref}b,2} + \cdots + i_{\mathrm{ref}b,N} \\ &= \sum_{j=1}^{N} k_{b,j} \cdot i_{\mathrm{Lh}b} = N \cdot \frac{1}{N} \cdot i_{\mathrm{Lh}b} = i_{\mathrm{Lh}b}, \end{aligned} \tag{6}$$

$$\begin{aligned} i_{Cc} &= \sum_{j=1}^{N} i_{\mathrm{C}c,j} = i_{\mathrm{C}c,1} + i_{\mathrm{C}c,2} + \cdots + i_{\mathrm{C}c,N} \\ &= i_{\mathrm{ref}c,1} + i_{\mathrm{ref}c,2} + \cdots + i_{\mathrm{ref}c,N} \\ &= \sum_{j=1}^{N} k_{c,j} \cdot i_{\mathrm{Lh}c} = N \cdot \frac{1}{N} \cdot i_{\mathrm{Lh}c} = i_{\mathrm{Lh}c}. \end{aligned} \tag{7}$$

It can be seen from Eqs. (5)–(7) that the total output currents of the SAPF system are still equal to the actual harmonic currents after the fault occurs, which means that the load harmonics can still be offset effectively based on this fault-tolerant strategy.

Furthermore, the proposed fault-tolerant strategy is applicable for the situation where faults appear in several different modules or different phases simultaneously. Assuming that phase a of module 2 has broken, phase b of module 1 malfunctions at the next moment. According to the conventional method, the whole system will collapse. However, based on the proposed strategy, two faulted phases will be isolated and three phases of the post-fault system will be reconfigured by the central control as follows: post-fault phase c still consists of bridge arm c from the two modules; post-fault phases a and b consist of only bridge arms a and b from the unfaulted modules, respectively. Expanding to the system with N modules, if there are x modules with phase a faults, y modules with phase b faults, and z modules with phase c faults, similarly, these broken phases will be isolated first and then the corresponding coefficients of the remaining phases will be updated through the RS485 bus communication as

$$k_{a,1} = k_{a,2} = \cdots = k_{a,(N-x)} = 1/(N-x), \tag{8}$$

$$k_{b,1} = k_{b,2} = \cdots = k_{b,(N-y)} = 1/(N-y), \tag{9}$$

$$k_{c,1} = k_{c,2} = \cdots = k_{c,(N-z)} = 1/(N-z), \tag{10}$$

where $x<N$, $y<N$, and $z<N$.

Theoretically, as long as at least one complete three-phase configuration exists after a fault occurs, the system can still maintain operation and try to guarantee the compensation performance as much as possible. However, it is noteworthy that the compensation capacity of the faulted phases cannot be superimposed on the remaining normal phases unconditionally. The maximum capacities of the power device and DC-link capacitors should be considered and the post-fault reference signals should be limited if necessary.

From the above analysis, the proposed fault-tolerant control strategy achieves essentially fault tolerance by transferring the compensation capacity in terms of the specific phase. Its realization is attributed to the decoupling control of the three-phase four-wire SAPF (Fig. 6). The cascade mode in the outer voltage loop and inner current loop is adopted in this control strategy. A phase locked loop (PLL) is used to precisely track the phase and frequency of the grid voltage, thus realizing frequency adaptability and synchronization with the grid. The discrete Fourier transformation (DFT) algorithm is used to extract the harmonic components of the load currents. By setting up different harmonic orders, the detection results will consist of different harmonics, leading to the

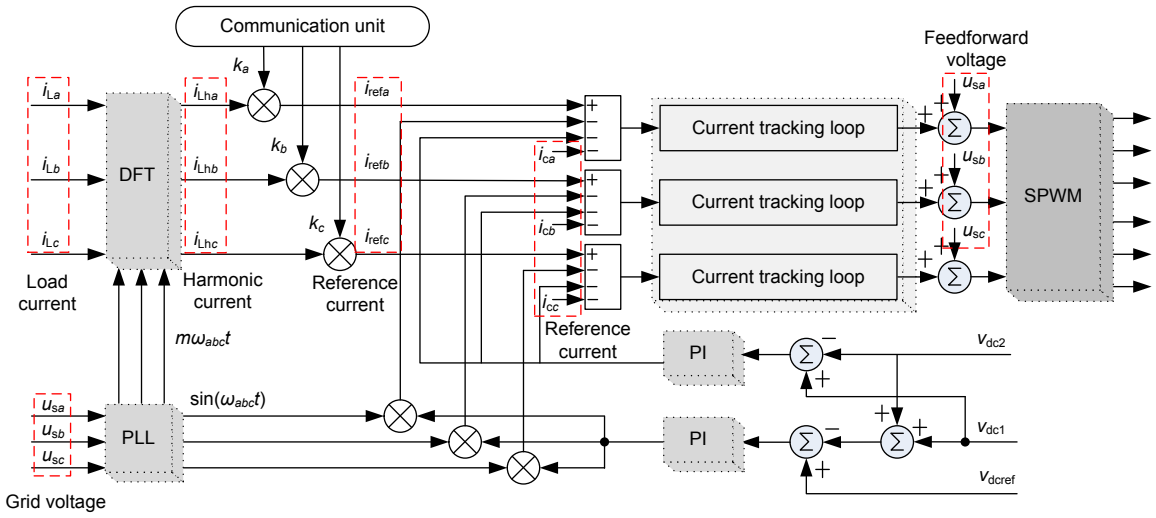

Fig. 6 Control block diagram of a single SAPF module in the *a-b-c* frame

selected compensations (Zhang et al., 2008). Then the detected harmonic currents will be multiplied by the distribution coefficient k from the communication unit to achieve the reference currents. The outer voltage loop combines two parts, the stabilization loop and the equalization loop. The former is to maintain the total voltage of the DC-bus and the latter is to equalize the voltages of the two split capacitors v_{dc1} and v_{dc2}. In the control of the stabilization loop, the DC-link voltage which is sampled simultaneously is compared with a reference. Then the error signal regulated by a proportional-integral (PI) controller is multiplied by the sinusoidal signal that is synchronous with the corresponding phase of the grid voltage. Then it is added to the three-phase reference currents as a part of the active components. In the control of the equalization loop, the voltage difference signal between C_{dc1} and C_{dc2} is superimposed on the reference currents as an element of a zero sequence. The function of the current loop is to track the reference signals precisely, thus contributing to the generation of the best PWM signals. A detailed control block for the current tracking loop will be discussed in the next section. The feedforward voltage is used to offset the fluctuation in the grid voltage and improve the dynamic performance (Xu et al., 2014).

Note that the control strategy inside a single module is carried out in the *a-b-c* frame, rather than in the traditional *d-q* frame. Due to the three-phase four-wire configuration, the control system can be decoupled easily into three single phases in the *a-b-c* frame and then split-phase control can be achieved. This is the reason why the coordination control among the modules can just be implemented in one specific phase and why the faulted phase compensation capacity can be transferred without affecting the other normal phases.

4 Stability analysis of a fault-tolerant system

4.1 Steady-state analysis of a post-fault circuit

Due to the consistency of the module structure and functionality, the same paralleled bridge arms and output filters can be merged. Still take the SAPF system with two modules as an example and assume that phase a of module 2 breaks down at a certain moment. After a faulted phase isolation, the equivalent inductances of phases b and c are still L_1 and L_2, respectively, while the equivalent inductance of phase a is double. For a capacitor, the value is just the opposite. Thus, the filter capacitor of phase a will be half. The equivalent post-fault circuit is shown in Fig. 7, where u_{ia}, u_{ib}, and u_{ic} are the inverter output voltages, i_{1a}, i_{1b}, and i_{1c} are the inverter side inductor currents, i_{2a}, i_{2b}, and i_{2c} are the grid side inductor currents, and i_{cfa}, i_{cfb}, and i_{cfc} are the filter capacitor currents.

4.2 System stability analysis under a fault-tolerant operation

The control system stability depends mainly on the stability of the current tracking loop. To achieve both steady-state accuracy and good dynamic

performance, a compound current control strategy is adopted, combining the traditional PI control with the improved repetitive control (Olm et al., 2011; Ramos and Costa-Castello, 2012). The control block diagram is shown in Fig. 8.

Here, $r(z)$, $e(z)$, $y(z)$, and $d(z)$ are the reference signal, error signal, output signal, and disturbance signal, respectively. M is the sampling number, d is the delay number, $S(z)$ is the compensator for repetitive control, and Q is an attenuation factor.

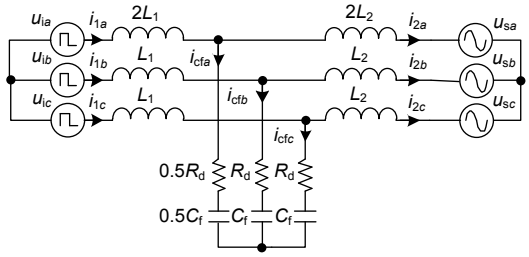

Fig. 7 Equivalent post-fault circuit after isolating phase *c* of module 2

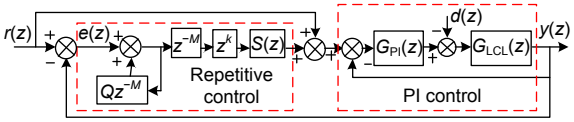

Fig. 8 Control block diagram of the inner current controller

The control object of the current double-loop is the LCL filter, whose transfer function can be expressed as

$$G_{\mathrm{LCL}}(s)=\frac{R_{\mathrm{d}}C_{\mathrm{f}}s+1}{L_1L_2C_{\mathrm{f}}s^3+(L_1+L_2)R_{\mathrm{d}}C_{\mathrm{f}}s^2+(L_1+L_2)s}. \tag{11}$$

Transforming it into the z-domain, the closed-loop transfer function of the inner PI loop can be deduced as

$$G_{\mathrm{PIb}}(z)=\frac{G_{\mathrm{PI}}(z)G_{\mathrm{LCL}}(z)}{1+G_{\mathrm{PI}}(z)G_{\mathrm{LCL}}(z)}. \tag{12}$$

The open-loop frequency characteristics of the pre- and post-fault inner PI loops are compared in Fig. 9. It can be seen that the resonance frequency decreases from 3.43 kHz to 3.06 kHz after adopting the proposed fault-tolerant strategy. However, the amplitude gain in the low-frequency band decreases from −8.26 dB to −11.6 dB, which means that the amplitude margin can be increased from 8.26 dB to 11.6 dB, which contributes to enhancing the system stability. Because the controller's pass-band is usually limited within 2.5 kHz, the advantage of the amplitude gain decrease in the low-frequency band is more significant than the disadvantage of the resonance frequency decrease. Thus, the inner PI loop can remain stable under a fault-tolerant operation.

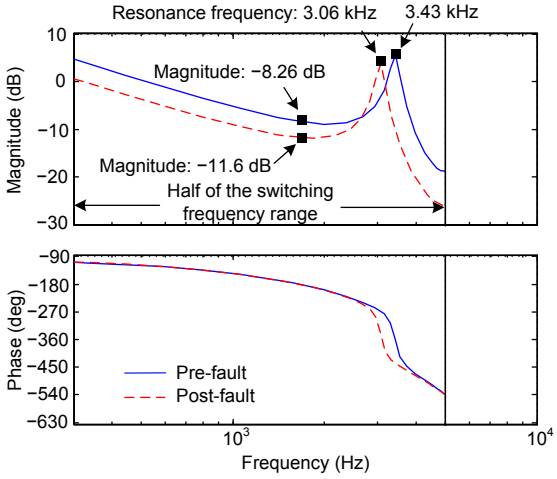

Fig. 9 Open-loop frequency characteristics of pre- and post-fault inner PI loops

As for the stability of the outer repetitive control loop, according to Fig. 8, the steady-state error expression of the double-loop can be derived as

$$\Phi_{\mathrm{er}}(z)=\frac{e(z)}{r(z)}=\frac{(z^M-Q(z))(1-G_{\mathrm{PIb}}(z))}{z^M-Q(z)+z^dS(z)G_{\mathrm{PIb}}(z)}. \tag{13}$$

It shows that the steady-state error depends on two factors: $G_{\mathrm{PIb}}(z)$, which has been just analyzed, and $z^dS(z)G_{\mathrm{PIb}}(z)$. Fig. 10 shows the pre- and post-fault frequency characteristics of $z^dS(z)G_{\mathrm{PIb}}(z)$. The increase in inductance does not make an evident difference on the amplitude characteristic of $z^dS(z)G_{\mathrm{PIb}}(z)$. However, its phase characteristic shows an obvious lag in the frequency band from 100 Hz to 2 kHz. Several order harmonics are compared in Table 1. This kind of phase lag will lead to the harmonic tracking deviation and deteriorate the compensation performance to some extent.

The frequency characteristic of the steady-state error (Eq. (13)) is illustrated in Fig. 11. It indicates that the amplitude gains for harmonic components decrease a little, which means that the corresponding tracking error increases slightly (Table 2). For exam-

ple, the magnitude of the 5th harmonic changes from −32.6 dB to −28.5 dB. However, −28.5 dB is still large enough for the controller to track the reference signal. Thus, the compensation accuracy of the 5th harmonic can still be guaranteed.

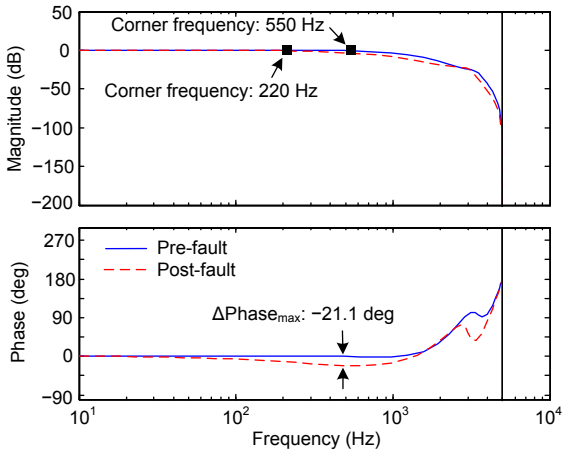

Fig. 10 Frequency characteristics of $z^d S(z)G_{\mathrm{PIb}}(z)$

Table 1 Harmonic phases of pre- and post-fault inner PI loops

Status	Phase (deg)				
	3rd	5th	7th	11th	13th
Pre-fault	0.277	0.28	0.189	−0.32	−0.63
Post-fault	−9.68	−14.9	−18.5	−21.4	−21.2

Table 2 Harmonic tracking errors of pre- and post-fault inner PI loops

Status	Magnitude (dB)				
	3rd	5th	7th	11th	13th
Pre-fault	−37.1	−32.6	−29.6	−25.4	−23.8
Post-fault	−33	−28.5	−25.6	−21.6	−20

In addition, according to the small-gain theorem (Liu and Jiang, 2015), a sufficient condition to keep the system stable can be derived as

$$X(z)=\left|z^d S(z)G_{\mathrm{PIb}}(z)-Q(z)\right|<1. \qquad (14)$$

Draw the Nyquist curve for $X(z)$ (Fig. 12). Even if the curve track of $X(z)$ expands a little in the fault-tolerant condition, the whole curve is still within the unit circle and keeps a distance from the circle boundary, which validates that the whole system still has enough stability.

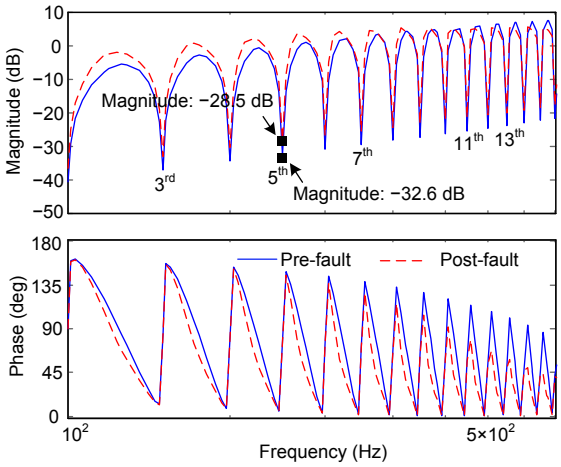

Fig. 11 Frequency characteristic of the steady-state error

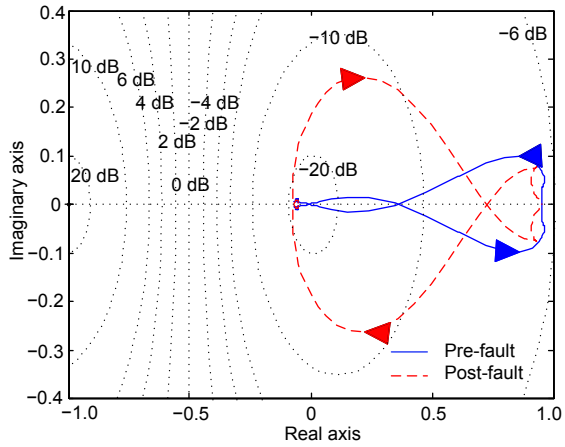

Fig. 12 Nyquist curve for $X(z)$

5 Experimental results and analysis

To verify the feasibility and efficiency of the proposed fault-tolerant strategy, an experimental prototype consisting of two modules was established. The parameters of the prototype are shown in Table 3. Fig. 13 shows the pictures of the prototype.

5.1 Steady-state compensation experiment with balanced loads

The schematic of the experimental setup is shown in Fig. 5. A nonlinear load (three-phase diode rectifier terminated to a resistive load with 1.5 Ω) is connected to the power grid and acts as the harmonic source. Considering that the current values are pretty high for the control system, two levels of measurement are adopted. The first level is the current

transducer (CT) whose transformation ratio is 400 A/5 A. The second level is the Hall sensor whose ratio is 5 A/25 mA. This kind of small current signal can be transferred into the control board. The corresponding experimental results are shown in Fig. 14.

Table 3 Configurations of the experimental prototype

Symbol	Description	Value
U_s	Phase voltage of the grid (V)	220
f_s	Grid frequency (Hz)	50
S_c	Rated capacity (kVA)	50
C_{dc}	DC-link capacitor (mF)	10
v_{dc}	DC-link voltage (V)	750
L_1	Inverter side inductor (μH)	180
L_2	Grid side inductor (μH)	60
C_f	Filter capacitor (μF)	30
R_d	Damping resistance (Ω)	0.1
f_{sw}	Switching frequency (kHz)	10

The effective value of i_{La} obtained from the oscilloscope is 277.3 A. Thus, the effective value of i_{Lha} can be calculated as $277.31/\sqrt{1+(1/\mathrm{THD}_a)^2}$ =72.7 A (THD means total harmonic distortion). The harmonic components before and after compensation are compared in Table 4. It can be seen that all the main harmonic components achieve an obvious reduction, especially the low-order harmonics. According to Figs. 14e and 14f, the 5th, 7th, and 11th harmonics decrease from the original values 22.36%, 10.51%, and 8.08% to 0.48%, 1.02%, and 0.93%, respectively, which indicates that both the detecting and tracking accuracies are very high and the cooperation among modules is also excellent. After compensation, the effective value of the grid harmonic current can be calculated as $271.4/\sqrt{1+(1/\mathrm{THD}_a)^2}$ =9.6 A, which shows a sharp reduction.

It can be observed from Fig. 14c that the load draws nonlinear currents, i_{La}, i_{Lb}, and i_{Lc}. Based on the series-wound detection for load currents and unified control strategy, each module's output currents are almost coincident. The three-phase output currents of

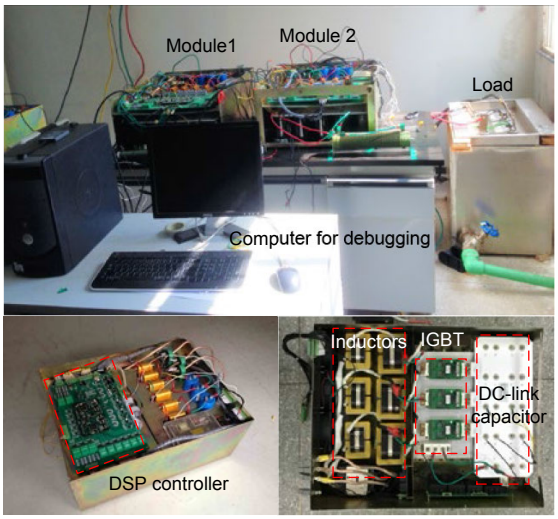

Fig. 13 Pictures of the prototype

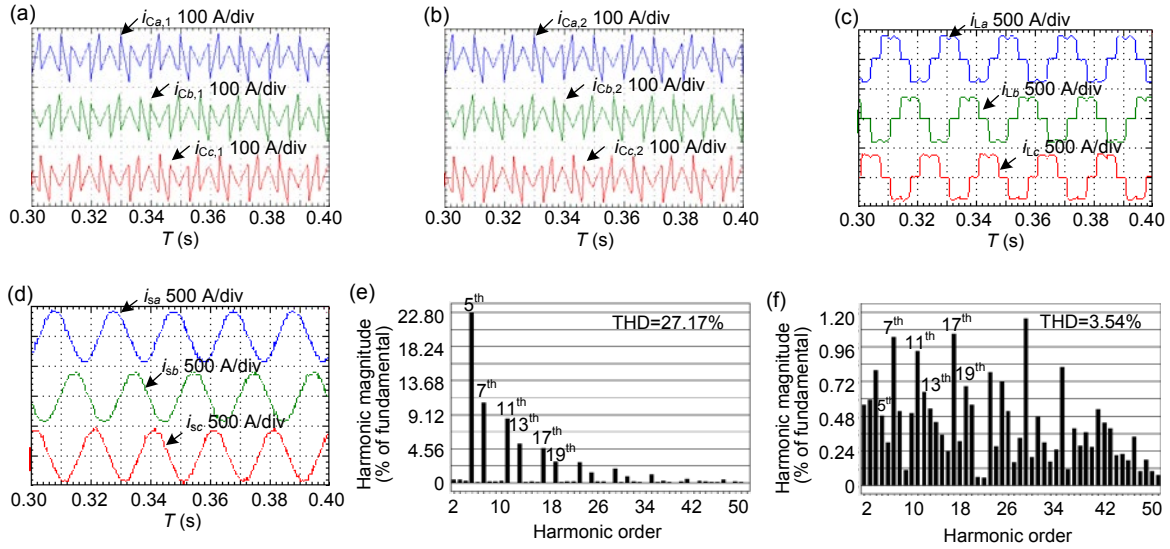

Fig. 14 Compensation waveforms with balanced loads: (a) module 1 output currents $i_{Ca,1}$, $i_{Cb,1}$, and $i_{Cc,1}$; (b) module 2 output currents $i_{Ca,2}$, $i_{Cb,2}$, and $i_{Cc,2}$; (c) load currents i_{La}, i_{Lb}, and i_{Lc}; (d) grid currents i_{sa}, i_{sb}, and i_{sc} after compensation; (e) frequency spectrum of load current i_{La}; (f) frequency spectrum of grid current i_{sa}

two modules are shown in Figs. 14a and 14b. Their resultant currents can track the load harmonic currents well, resulting in the harmonic components of the grid currents i_{sa}, i_{sb}, i_{sc} being close to zero (Fig. 14d).

Table 4 Harmonic component comparison

Harmonic order	i_{Lh} (% of the fundamental component)	
	Before compensation	After compensation
5th	22.36	0.48
7th	10.51	1.02
11th	8.08	0.93
13th	5.06	0.53
17th	4.24	1.05
19th	2.60	0.68

5.2 Steady-state compensation experiment with unbalanced loads

The experimental study was further extended to investigate the performance when compensating for unbalanced nonlinear loads. Three types of asymmetric loads are set up: (1) a parallel 20-Ω resistor between phases *a* and *b*; (2) an open circuit of phase *c*; (3) an open circuit of phase *c* and a 4-Ω resistor installed in series in phase *a*. The schematic is shown in Fig. 5.

Fig. 15a shows that when paralleling a 20-Ω resistor between phases *a* and *b*, the equivalent impedance of phases *a* and *b* becomes diminished, resulting in a current increase. According to the split-phase control, the detected and produced reference signals of phases *a* and *b* will be larger than that of phase *c*. Thus, the compensation currents of phases *a* and *b* should be greater than that of phase *c*. Fig. 15b shows that due to the open circuit of phase *c*, its compensation current is nearly zero and it does not affect the performance of the other two phases. Fig. 15c shows that when a 4-Ω resistor is in series in phase *a*, its equivalent impedance is increased, resulting in a current decrease. Similarly, the compensation current of phase *a* will be smaller than that of phase *b*. Table 5 lists the THD of grid currents under unbalanced conditions.

By observing the three-phase grid currents in Fig. 15, the waveforms of the grid currents are all purely sinusoidal and the corresponding THD decreases obviously after compensation, which validates that although the three-phase load configurations are asymmetrical and even lacking one phase, the SAPF system can still compensate for the load harmonics effectively based on split-phase control.

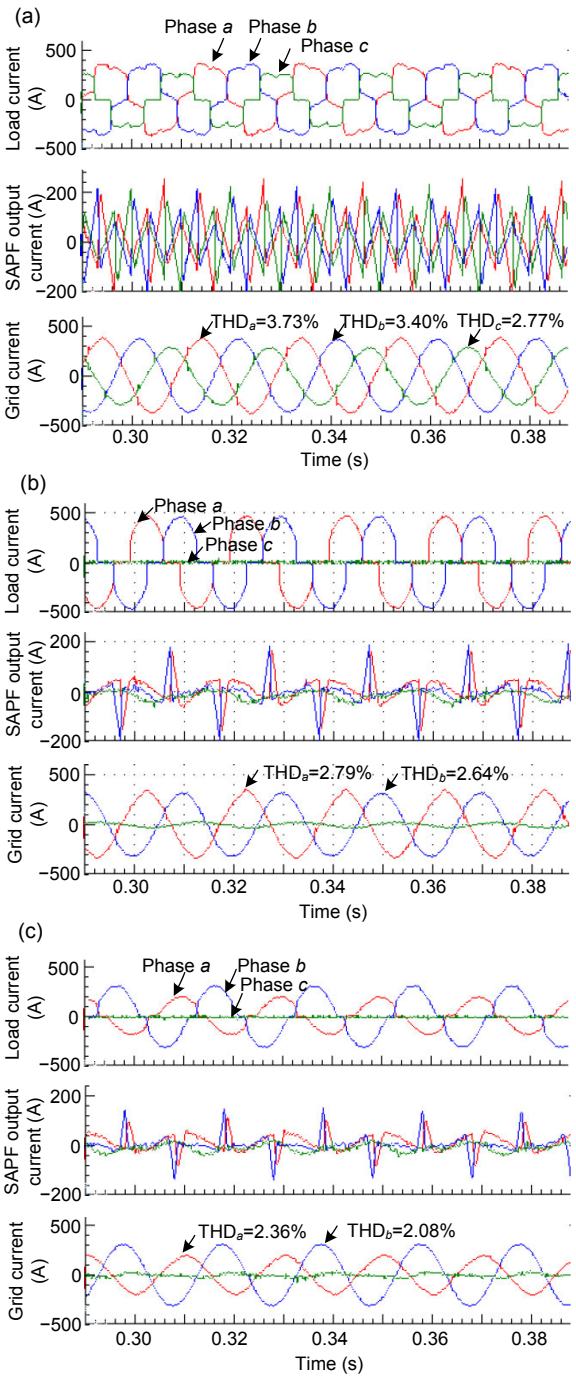

Fig. 15 Compensation waveforms with unbalanced loads: (a) a 20-Ω resistor between phases *a* and *b*; (b) an open circuit of phase *c*; (c) an open circuit of phase *c* and a 4-Ω resistor in series in phase *a*

5.3 Dynamic experiment with sudden load change

To validate the dynamic response of the multi-modular SAPF system, a load changing experiment was carried out. The most serious situation in which a load capacity changes sharply from zero to 100% is set up. Fig. 16 shows that when the load is turned on suddenly, these two modules respond almost at the same time and then compensate for half of the total load harmonics separately, which demonstrates that the synchronization between the modules is excellent. Meanwhile, the grid current is compensated for to an ideal sinusoid in almost one fundamental period, which indicates that the compound control strategy achieves good dynamic performance.

Table 5 Compensation performance under unbalanced conditions

Condition	Phase	THD (%)	
		Before compensation	After compensation
1	*a*	22.51	3.73
	b	22.32	3.40
	c	28.50	2.77
2	*a*	23.96	2.79
	b	23.76	2.64
	c	–	–
3	*a*	16.42	2.36
	b	10.55	2.08
	c	–	–

5.4 Dynamic experiment with a phase fault based on a conventional fault-tolerant control strategy

Fig. 17 shows the experimental results for the output currents and grid currents of a two-modular SAPF system during the occurrence of a fault in module 1 phase *a*. The fault occurs at t_0. It shows the effect of the conventional fault-tolerant control strategy, which can be regarded as a comparison for the proposed fault-tolerant approach.

According to the conventional remedial strategy, once a phase fault occurs, the whole module will be out of service (Fig. 17a). After the monitor detects the malfunction in module 1, module 2 will receive the double distribution coefficient and control its three phases to output the double compensation currents (Fig. 17b). After the activation of the upper strategy, the three-phase grid currents return to the same quality as that before the fault occurrence (Fig. 17c). Yet, during the activation process, the grid power quality becomes deteriorated and the three-phase THDs decrease to 9.27%, 11.30%, and 8.96%, respectively (Fig. 17d). This is due to the bus communication delay, coefficient updating calculation, and the dynamic response delay of the tracking unit. Note that a single-phase fault will affect the entire multi-modular system performance and also waste the remaining usable power devices when adopting the conventional strategy.

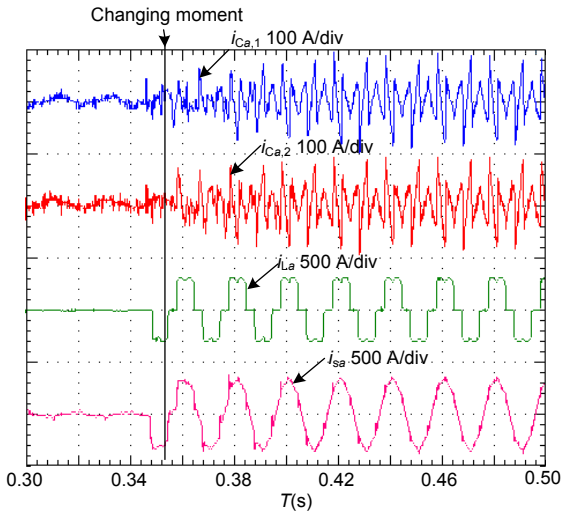

Fig. 16 Dynamic waveforms of a changing load

5.5 Dynamic experiment with a phase fault based on the proposed fault-tolerant control strategy

Fig. 18 shows the experimental results based on the proposed fault-tolerant control strategy. The fault mode is introduced at t_1. After the fault occurs, phase *a* is isolated separately. The controller blocks the PWM signals from phase *a* but keeps generating the other two phases' PWM signals and driving the remaining power semiconductors, resulting in a continuous operation of phases *b* and *c* (Fig. 18a). Attributed to the real-time bus communication and centralized control, the distribution coefficient $k_{a,2}$ will be renewed to double. Thus, phase *a* will output the double currents, which means that phase *a* in module 2 will undertake the compensation capacity of phase *a* in module 1. Due to the independent phase coefficient updating and split-phase control, the normal phases' reference signals will not change and their outputs will be the same as before (Fig. 18b). Thus, for the

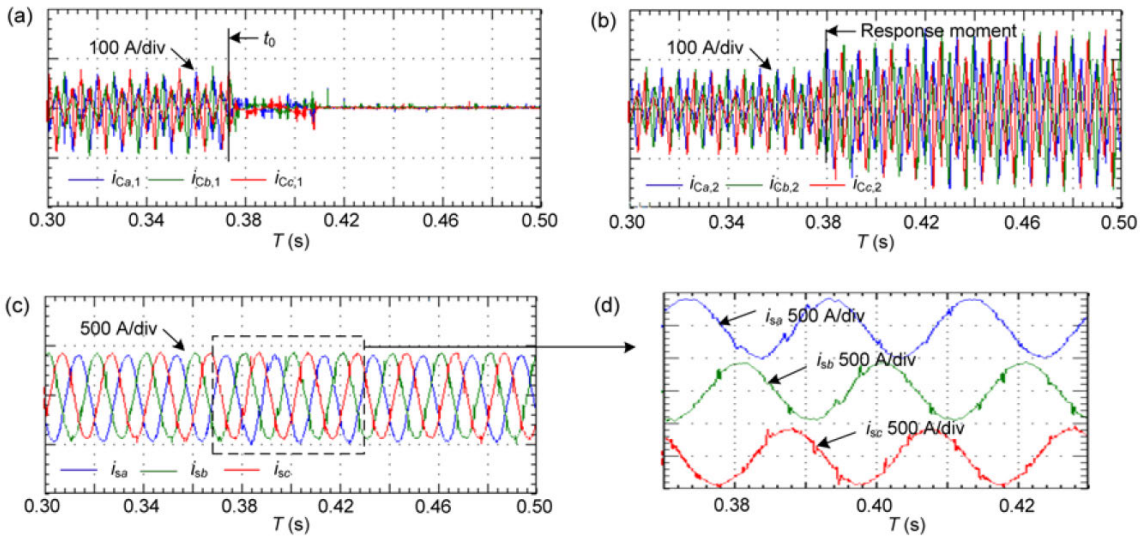

Fig. 17 Waveforms based on the conventional fault-tolerant strategy: (a) module 1 output currents $i_{Ca,1}$, $i_{Cb,1}$, and $i_{Cc,1}$; (b) module 2 output currents $i_{Ca,2}$, $i_{Cb,2}$, and $i_{Cc,2}$; (c) grid currents i_{sa}, i_{sb}, and i_{sc}; (d) zoomed grid currents during the strategy activation (References to color refer to the online version of this figure)

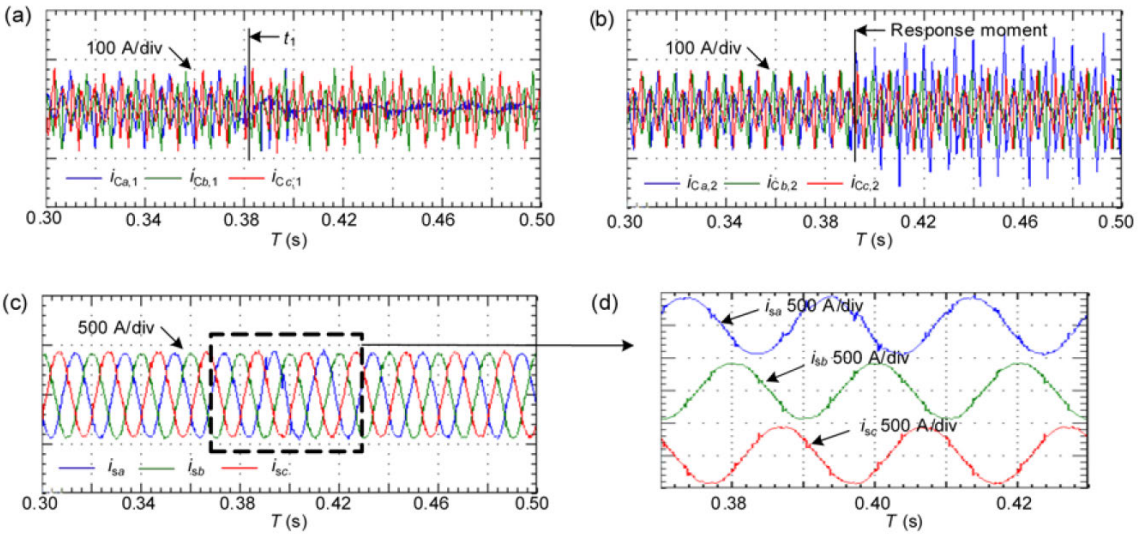

Fig. 18 Waveforms based on the proposed fault-tolerant strategy (one phase malfunction): (a) module 1 output currents $i_{Ca,1}$, $i_{Cb,1}$, and $i_{Cc,1}$; (b) module 2 output currents $i_{Ca,2}$, $i_{Cb,2}$, and $i_{Cc,2}$; (c) grid currents i_{sa}, i_{sb}, and i_{sc}; (d) zoomed grid currents during the strategy activation (References to color refer to the online version of this figure)

entire multi-modular SAPF system, only phase *a* will experience a capacity adjustment process. This avoids a fluctuation in the other two grid currents and guarantees the whole system compensation quality as much as possible (Figs. 18c and 18d). Compared with the conventional strategy, the proposed fault-tolerant strategy has a better disbursement of power loss and a higher reliability.

The experiment was further extended to validate the performance when faults appear in two phases simultaneously. Assume that phases *a* and *b* break down at t_2. Fig. 19a shows that phase *c* of module 1 is under a sustained operation because of the separate isolation and blocking of the faulted phases *a* and *b*. Similarly, with the effect of bus communication and split-phase control, phases *a* and *b* of module 2 respond and adjust the outputs while phase *c* maintains stability (Fig. 19b). Thus, the three-phase grid currents are still symmetrical and well compensated (Fig. 19c). Based on the proposed fault-tolerant

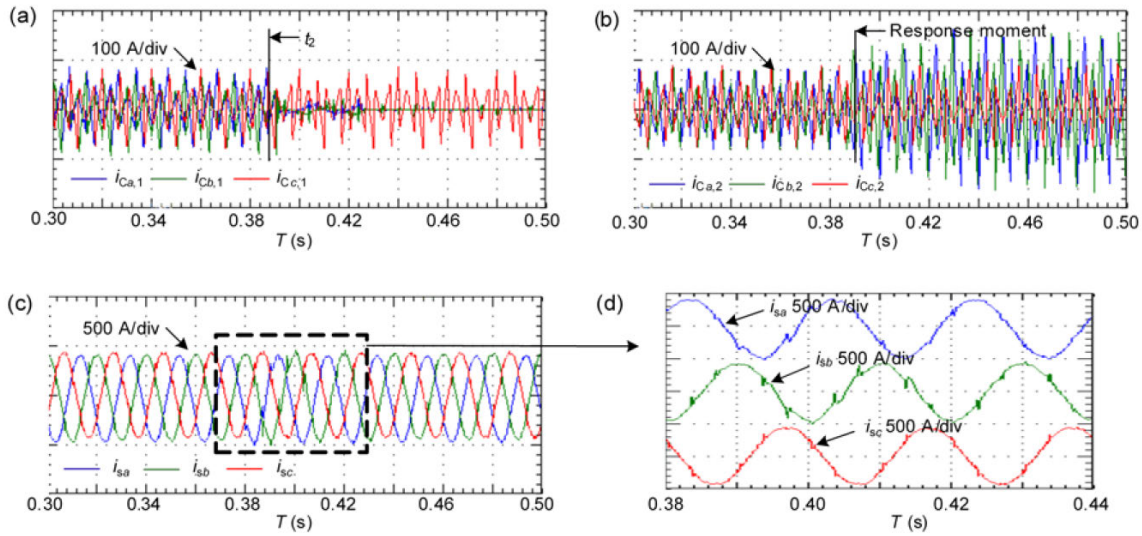

Fig. 19 Waveforms based on the proposed fault-tolerant strategy (malfunction of two phases): (a) module 1 output currents $i_{Ca,1}$, $i_{Cb,1}$, and $i_{Cc,1}$; (b) module 2 output currents $i_{Ca,2}$, $i_{Cb,2}$, and $i_{Cc,2}$; (c) grid currents i_{sa}, i_{sb}, and i_{sc}; (d) zoomed grid currents during the strategy activation (References to color refer to the online version of this figure)

control strategy, the performance deterioration for the three phases can be reduced to just two phases (Fig. 19d). In other words, if the two faults do not appear in the same phase, the two-modular SAPF system can always operate normally and the three-phase compensation performance will still be perfectly ensured. This is the biggest benefit of split-phase control and it can be verified as effective when extended to a multi-modular system.

6 Conclusions

In this study, a multi-modular SAPF system has been introduced and a novel fault-tolerant control strategy has been proposed. The advantages of structural consistency and functional compatibility have been shown to improve the coordination control among the modules. Each module's reference signal was obtained by multiplying the total reference signal by the respective distribution coefficient. Due to the three-phase four-wire configuration, the control system was decoupled into three independent phases in the *a*-*b*-*c* frame and split-phase control was implemented. When a fault occurs, unlike a conventional fault-tolerant method, the proposed approach just isolates the faulted phase and transfers the compensation capacity to the same phases of the other normal modules through real-time bus communication, resulting in the continuous operation of the faulted module and optimization of the remaining usable power devices. We also validated that as long as a set of integrated three-phase circuits exist, the whole system can still operate normally, and the compensation performance can be guaranteed. The post-fault circuit analysis and system stability dissection also demonstrate that even if the controller performance deteriorates a bit due to the circuit reconfiguration, the tracking accuracy and the system reliability are still high enough within the 2.5-kHz frequency band. Finally, various kinds of experimental results have verified the feasibility and validity of the proposed system and its fault-tolerant control strategy.

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