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Review:

Energy-efficient power amplifiers and linearization techniques for massive MIMO transmitters: a review*

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Abstract: Highly efficient power amplifiers (PAs) and associated linearization techniques have been developed to accommodate the explosive growth in the data transmission rate and application of massive multiple input multiple output (mMIMO) systems. In this paper, energy-efficient integrated Doherty PA monolithic microwave integrated circuits (MMICs) and linearization techniques are reviewed for both the sub-6 GHz and millimeter-wave (mm-Wave) fifth-generation (5G) mMIMO systems; different semiconductor processes and architectures are compared and analyzed. Since the 5G protocols have not yet been finalized and PA specifications for mMIMO are still under consideration, it is worth investigating novel design methods to further improve their efficiency and linearity performance. Digital predistortion techniques need to evolve to be adapted in mMIMO systems, and some creative linearity enhancement techniques are needed to simultaneously improve the compensation accuracy and reduce the power consumption.

Key words: Energy-efficient; Linearization; Massive multiple input multiple output (mMIMO); Monolithic microwave integrated circuit (MMIC); Power amplifier

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1 Introduction

To support a drastically increasing number of subscribers, multiple input multiple output (MIMO) systems have been widely used in modern wireless communication systems. In fact, MIMO techniques can increase data transmission rates, coverage of service areas, and communication reliability without additional radio frequencies (RFs). Massive MIMO (mMIMO) is a critical technology in fifth-generation (5G) systems, significantly increasing the network capacity and spectral efficiency, as well as reducing the wireless network interference. In recent proposals for 5G systems, the number of RF chains in mMIMO RF front ends can go up to 256, with bandwidths up to 800 MHz per chain (Larsson et al., 2014; Gao X et al., 2015; Harris et al., 2017). Broader bandwidth is expected in the upcoming 5G system to accommodate the growing user demand for much higher data transmission rates. The spectrum allocation is quite crowded already, and operators are seeking a new radio spectrum resource. Owing to their lower path loss, low-frequency bands remain crucial for maintaining the extensive coverage of 5G networks. Therefore, the 3.3–5.0 GHz band is receiving significant attention as a frequency range for 5G that can provide significant bandwidth. Initial studies conducted and prototyping efforts made at millimeter-wave (mm-Wave) frequencies have demonstrated that mm-Wave bands would also be promising for fulfilling the requirements of 5G. Therefore, multiple

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mm-Wave bands, including the spectra around 26, 28, 37, and 39 GHz, have been opened for 5G development.

For better spectrum efficiency, beamforming (BF) architectures have attracted intensive investigation in mMIMO systems. A fully digital BF can yield optimal performance, and has been widely adopted in the sub-6 GHz band. Multipath effects are quite abundant in the sub-6 GHz band, and a fully digital BF architecture can achieve high capacity and flexibility. However, due to the severe path loss at the mm-Wave range, the advantage of using a fully digital BF architecture is not straightforward; alternatively, a hybrid BF architecture stands out as a good trade-off between performance and system complexity. Moreover, the antenna element dimension in mm-Wave mMIMO is smaller; thus, more RF chains can be integrated into a single chipset.

The substantial increase in RF chains drastically complicates the mMIMO transmitter. System- and circuit-level designers must propose sound and implementable techniques and workarounds to maintain acceptable performance for the mMIMO transmitters from the energy efficiency and signal linearization perspectives. Unlike conventional power amplifier (PA) modules in a base station, monolithic microwave integrated circuits (MMICs) or hybrid integrated PA chips are highly desirable in transmitters, in order to reduce the dimensions of the mMIMO systems. Due to the increasing number of PA modules, the output power of each PA unit is reduced; thus, GaN-, GaAs-, and Si-based processes are all possible options for PA design. Efficiency is critical in reducing the system consumption, and a PA architecture with high back-off efficiency should be adopted. The signal bandwidth increases significantly in 5G; thus, broadband PAs are needed, and the video bandwidth has to be improved to eliminate the memory effects. Digital predistortion (DPD) is commonly used for linearization in 4G and will also be employed in 5G mMIMO systems. In mm-Wave bands, the signal bandwidth is up to 800 MHz and hybrid BF architectures are used; the cost and performance of present DPDs will be unacceptable. New DPD architectures and low-power DPD are required to reduce the digital consumption. Furthermore, the PA should be linearized from the circuit level to relieve the performance requirements for DPD, and analog predistortion (APD) is an attractive solution to satisfy the spectrum mask and distortion requirements.

This paper is organized as follows. First, transmitter architectures for mMIMO are analyzed, and the required PA architectures and specifications are given. Then, recent research progress in the fields of sub-6 GHz bands and mm-Wave Doherty PA (DPA) design is introduced in detail. Finally, linearization methods of PAs in mMIMO scenarios, including DPD and APD, are provided.

2 Transmitter architectures for mMIMO

As one of the key devices in RF transmitters, PAs are characterized as the most power-hungry components, and their performances directly affect the efficiency of RF transmitters. The semiconductor technology and the architectures have to be carefully selected when designing 5G PAs to meet the output power, efficiency, and linearity requirements, in particular for mMIMO transmitters. Therefore, in this section, we start by discussing the mMIMO structures in sub-6 GHz and mm-Wave bands, and then discuss the corresponding requirements for PAs.

2.1 mMIMO for the sub-6 GHz band

Measurements carried out in recent years on the sub-6 GHz mMIMO channels revealed some fundamental differences from what is currently being used in small-scale MIMO systems. These measurements indicate that the user equipment (UE) signals received from the different antenna elements of the transmitter tend to become space-orthogonal with increase in the number of antenna elements, and hence these MIMO state channels offer a favorable propagation scenario (Marzetta et al., 2016). In addition, the multitudes of scattering clusters at sub-6 GHz bands lead to multipath propagation, which is beneficial in supporting multiple subscribers. Generally, one mMIMO base station at the sub-6 GHz band can cover more than 10 users simultaneously (Bai and Heath, 2014). Ideally, the number of simultaneously served subscribers increases with the expansion of the array scale. However, considering the transmitter volume and form factor in the base station, the array size has to be maintained within reasonable dimensions. For example, a 64-element antenna array, distributed as an 8×8 uniform rectangular array (URA) with half-

wavelength element spacing at 3.5 GHz, occupies at least a 35 cm×35 cm space. As the array dimensions are moderate in sub-6 GHz mMIMO, a fully digital BF architecture is appropriate to make full use of the rich multipath channels (Bai and Heath, 2014; Hu HJ et al., 2017). Since mm-Wave transmission is not suitable for long-range outdoor communications, sub-6 GHz frequencies are expected to serve both outdoor and indoor coverage, and support high-mobility UE. This will require high output power from the transmitters to serve long-range, large cells. Taking into account hardware cost and power consumption, 64 channels associated with digital BF (Fig. 1a) are the optimum array size for a sub-6 GHz mMIMO transmitting system, as is already used in mMIMO measurements and prototypes.

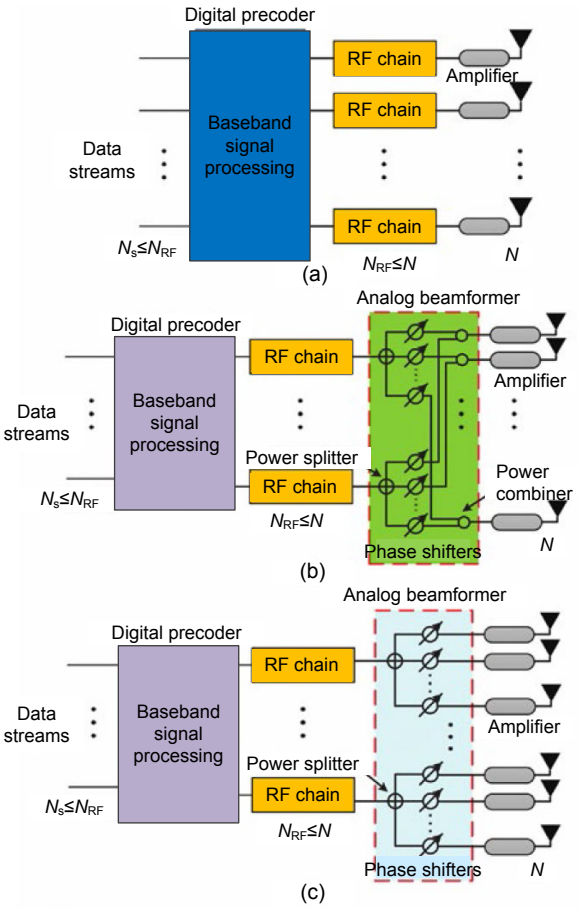

Fig. 1 Massive MIMO transmitter architectures: (a) digital beamforming; (b) fully connected hybrid beamforming; (c) sub-connected hybrid beamforming

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2.2 mMIMO for the mm-Wave band

The development of the mm-Wave frequency band, which can provide GHz bandwidth and tens of gigabit data transmission rate, is important to relieve the global spectrum scarcity and bandwidth shortage (Pi and Khan, 2011), to significantly expand the transmission scale, and to enhance service quality. However, the propagation condition is unfavorable for mm-Wave communication due to its considerable propagation loss. The legitimate concerns regarding the propagation characteristics at mm-Wave frequencies, such as higher rain attenuation, atmospheric absorption, and significant loss through foliage, are the main obstacles for mm-Wave carriers in long-range communications (Rappaport et al., 2015). However, when one considers the small-sized cells in the urban environment (on the order of 200 m), one realizes that rain attenuation and atmospheric absorption will not create significant path loss for the mm-Wave frequency, especially for 28 and 38 GHz frequency bands (Rappaport et al., 2013). Thus, the use of small-cell and high-density base stations can mitigate the attenuation issue. However, this approach may cause other interference to neighboring UEs due to the small coverage of the base station. To avoid such situations, a highly directional beam should be synthesized by the large-scale antenna array with high array gain to mitigate this interference and, simultaneously, compensate for the path loss and extend the range of communications (Niu et al., 2015).

According to the aforementioned mm-Wave propagation characteristics, the mm-Wave mMIMO scale should be much larger than that in the sub-6 GHz band (i.e., 256 antennas compared to 64 antennas) to achieve high array gain, which will pose severe challenges for its realization in practice. One challenging problem is that in a sub-6 GHz mMIMO system with a digital BF structure, each antenna requires one dedicated RF chain, including digital-to-analog converters (DACs), mixers, PAs, and passive components (Heath et al., 2016). This will result in unaffordable hardware costs and power consumption in mm-Wave mMIMO systems, due to the significant number of antennas and the high power consumption of the RF chain (e.g., 250 mW at mm-Wave frequencies compared with 30 mW at microwave frequencies). On the other hand, analog BF requires only one RF chain, resulting in relatively low hardware cost

and power consumption; however, it supports only single digital stream and is therefore not applicable in multiuser scenarios. Therefore, the hybrid BF, as shown in Figs. 1b and 1c, which combines the merits of digital and analog BF to support multiuser and multistream transmission, while requiring moderate hardware cost and power consumption, is considered to be the most appropriate architecture for mm-Wave mMIMO (Han et al., 2015).

Although mm-Wave hybrid BF can support multiple users, the number of simultaneously served users is smaller than that of sub-6 GHz digital BF (10 or more users in sub-6 GHz, compared to 1–4 users in the mm-Wave band) as the result of hardware limitations and mm-Wave channel conditions (Rappaport et al., 2013; Roh et al., 2014). However, as long as the number of RF chains is more significant than the rank of the channel matrix, the small-scale digital precoder is still able to obtain near-optimal performance compared to a fully digital BF, which also indicates the feasibility of hybrid BF for mm-Wave mMIMO (Gao XY et al., 2016).

2.3 PA architecture and specification

A large-scale array involving hundreds of antenna elements leads to different requirements for PAs, namely, higher integration and lower output power capability. Fig. 2 presents the output power of a single PA in the mm-Wave and sub-6 GHz array, which varies with the array size, and the resulting process selection. For simple analysis, the antennas in the array are anticipated to have roughly 6 dB gain for each single antenna and to be spaced half a wavelength for each adjacent element (Shakib et al., 2016). It is intuitive to see in Fig. 2 that the array gain increases significantly with the expansion of the array size. When the array size reaches 500 antennas or more (this is also expected to be the most common mm-Wave large array size), the antenna array can provide a gain of more than 30 dB, which reduces the output power requirement for each PA in the array. Unlike the high output power (>30 dBm) in the sub-6 GHz band, the required output power of a single PA in a mm-Wave mMIMO is only 10–20 dBm, where high-output materials, such as gallium nitride (GaN) and gallium arsenide (GaAs), are not needed. Most importantly, the highly integrated low power requirement suggests that complementary metal oxide semiconductor (CMOS) or silicon germanium (SiGe) materials would be more appropriate to fabricate the PAs.

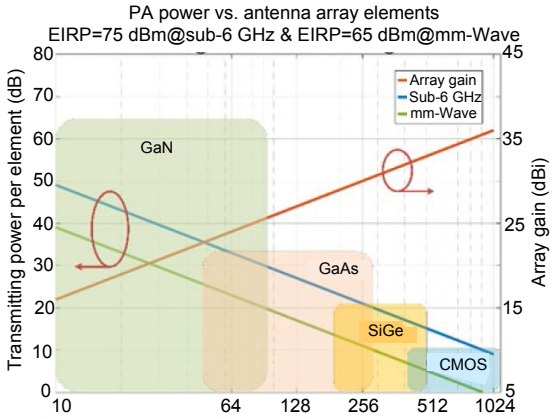

Fig. 2 Power amplifier specification analysis in sub-6 GHz and mm-Wave bands

Since PA is the most power-hungry component in the transmitter, its efficiency plays a key role in the overall system's efficiency performance. Due to the complex modulation scheme, modern communication signal usually exhibits a high peak-to-average power ratio (PAPR). To achieve high average efficiency under modulation of the excitation signal, PA should have a high back-off efficiency. Many class-AB PAs with state-of-the-art performance have been reported, including GaN MMIC PAs in the sub-6 GHz band (Quaglia et al., 2014b; Giofre et al., 2016; Liu B et al., 2018) and Si-based or GaAs PAs in the mm-Wave band (Nguyen and Pham, 2016; Sarkar et al., 2017; Ali et al., 2017, 2018; Li TW and Wang, 2018; Lv et al., 2018b). In spite of their high saturation efficiency, the back-off efficiency is relatively low: lower than 30% for sub-6 GHz GaN MMIC PAs and lower than 20% for mm-Wave PAs. Therefore, a high-efficiency PA architecture must be used to further improve the back-off efficiency. Among the efficiency enhancement techniques, Doherty and envelope tracking (ET) architectures have been successfully adopted in 4G transmitting systems. The ET architecture is a good solution for multiband and multimode energy-efficient transmitters, a solution that has been widely used in mobile terminals; however, it suffers from the bandwidth limitation of envelope amplifiers. For 5G systems, the signal bandwidth requirement exceeds 200 MHz in the sub-6 GHz or mm-Wave bands;

therefore, it is impractical to use ET in mMIMO transmitters. In contrast, the DPA architecture is a promising technique for moderate- to high-efficiency enhancement with high PAPR signals. The DPA architecture almost dominates the PA market in base stations due to its promising efficiency and relatively low circuit complexity. In the upcoming 5G system, the Doherty architecture offers a true, demonstrated, and energy-efficient advantage for 5G PAs.

The array's gain increases along with the expansion of the array scale. However, in practice, the array scale is also limited by technological factors, such as equipment volume, power consumption, and efficiency. A possible PA specification analysis is illustrated in Fig. 2 and outlined in Table 1 (Shakib et al., 2016). In the sub-6 GHz band, the target effective isotropic radiated power (EIRP) is above 75 dBm. Based on the literature, 64-channel mMIMO architectures have been used in demo prototypes, which means that the average power of each PA should be around 33–38 dBm and should support more than 200 MHz signal bandwidth. For 5G systems, the average efficiency of each PA is expected to be better than 40%, for the overall efficiency of the whole base station to be acceptable. Shakib et al. (2016) investigated the optimum carrier frequency and output power of mm-Wave mMIMO transmitters and UEs, considering the array scale, path loss, and other factors. Fig. 2 shows the total power consumption for the analog beamformer and the array's gain as a function of the number of antenna elements at 28 GHz, under the assumption of 200 m non-line-of-sight (NLOS) transmission for 65 dBm EIRP and 800 MHz bandwidth. The expected output power per PA can be calculated as follows:

$$P_{\mathrm{PerPA}}(\mathrm{dBm}) = \mathrm{EIRP}\ (\mathrm{dBm}) - \mathrm{ArrayGain}\ (\mathrm{dB}) - 3\log_2 N, \tag{1}$$

where N denotes the number of antenna elements.

The biggest challenge for 5G mMIMO is from the linearity specification to transmit high-order modulation schemes, such as 64 quadrature amplitude modulation (QAM) or 256QAM. In the sub-6 GHz digital BF architecture, at first glance, it is expected to perform DPD for each single channel; however, in such cases, the power consumption of the signal processing procedure in field-programmable gate array (FPGA) and high-speed ADC/DAC is almost comparable to PA devices' energy consumption; thus, a less power-hungry linearization technique is needed to improve the overall efficiency. In the mm-Wave band, it is not possible to implement DPD for each PA in a hybrid BF architecture, so some novel linearity enhancement techniques are needed for the upcoming mm-Wave mMIMO transmitters. Fortunately, owing to the large array gain and BF, the transmit power can be made significantly lower and concentrated within primary beams. For example, the transmit power from a large uniform linear array, which has 300 antennas spaced by half a wavelength, is predicted to be roughly 25, 19, and 13 dB lower compared to legacy single input single output (SISO) systems when serving 1, 4, and 15 subscribers in line of sight, respectively (Mollen et al., 2018).

Table 1 Power amplifier specifications for 5G

Parameter	Value or description	
	Sub-6 GHz	mm-Wave
Frequency	3.4–3.8 GHz/ 4.8–5.0 GHz	24.75–27.5 GHz/ 37–42.5 GHz
Bandwidth	>200 MHz	>800 MHz
P_{out}@sat	>43 dBm	>25 dBm (III-V)/ 17 dBm (Si)
Average efficiency	>40%	>20%
ACPR	<–45 dBc	<–27.5 dBc
EVM	<5% (64QAM)/ <3% (256QAM)	<5% (64QAM)/ <3% (256QAM)

ACPR: adjacent channel power ratio; EVM: error vector magnitude

3 Design of sub-6 GHz DPA

The sub-6 GHz bands can achieve wider coverage if the total transmit power is large enough since the path loss is relatively small at low-frequency bands. As a result, the saturation output power of each PA may reach 20 W, so GaN devices have been recognized as a good candidate technology due to their high power density and excellent efficiency. The DPAs implemented using a printed circuit board (PCB), available in the literature, generally show high performance. However, these designs are complicated for deployment in an mMIMO system due to their large size (Chen XF et al., 2016; Probst et al., 2017; Huang et al., 2018). Fortunately, DPA GaN MMICs for microwave backhaul applications and small-cell base stations are available (Camarchia et al., 2013a,

2013b; Gustafsson et al., 2013, 2014, 2016; Kim et al., 2014; Lee J et al., 2014; Piazzon et al., 2014; Giofre et al., 2015; Jee et al., 2015; Lee S et al., 2015; Park Y et al., 2015; Ayad et al., 2017; Giofre and Colantonio, 2017); such DPAs are excellent references for the design of DPAs in 5G transmitters. DPA GaN MMICs for 5G application have also been reported in recent years (Maroldt and Ercoli, 2017; Ishikawa et al., 2018; Li SH et al., 2018; Lv et al., 2019b), but further research is still required.

To enable a compact communication system, fully integrated GaN MMICs using only one material are the best solutions, as no off-chip matching components are required and the chip can be easily packaged. However, the fully integrated DPAs end up costly in most cases due to their large footprint on the GaN wafer, the fabrication of which is still considered to be an expensive process. An alternative solution is hybrid integration, which means that only active devices and power bars are fabricated using the GaN process, and all matching and biasing circuits are realized in other less expensive integrated passive device (IPD) processes. Then, different dies can be connected with bonding wires and integrated into one package. Partial integration is also investigated to reduce the die size, where transistors and partial matching circuits are implemented using the GaN process, while some passive devices are placed outside the chip. The performances of the typical works referenced in this section are summarized in Table 2.

3.1 DPA MMIC with full integration

A fully integrated C-band GaN DPA MMIC for 5G mMIMO application is presented elsewhere (Lv et al., 2019b) using a 0.25-μm GaN high electron-mobility transistor (HEMT) technology (WIN Semiconductors Corp.). A low-Q output network is used to broaden the bandwidth, and on-chip transmission lines (TLs) are used as drain bias inductors for a low insert loss. Reversed uneven power splitting and back-off input matching are proposed for gain enhancement. Fig. 3 shows the chip photo and measurement results. The fabricated DPA occupies a size of 2.2 mm×2.1 mm, requiring no off-chip components. A saturated output power of 40.4–41.2 dBm and a 6-dB back-off drain efficiency (DE) of 47%–50% are achieved across a wide bandwidth ranging from 4.5 to 5.2 GHz. Using a 40-MHz Long-Term Evolution (LTE) signal, the measured adjacent channel power ratio (ACPR) is –29 dBc at the output power of 33 dBm, which is improved to –46 dBc after applying DPD.

Since there is only one stage, the power gain of the DPA (Lv et al., 2019b) is relatively low. To improve the power gain, two stages are adopted (Lv et al., 2019d). Single- and dual-driver topologies are compared, and it is demonstrated that the former can significantly degrade the back-off power added efficiency (PAE) when the gain of the power stage is not high enough. Thus, to minimize the impact of the driver stage on the PAE, a dual-driver topology is used, wherein the driver stage is used in both the main and the auxiliary branches. Impedance transformers in the output network are realized by lumped high-pass π-type networks to reduce the occupied area. Fig. 4a shows the proposed output network. The shunt inductors at the same node can be merged into a much smaller inductor, and there are only three inductors in the final output network. Because of the limited direct current (DC) capacity and the low Q-factor of on-chip inductors, two drain bias inductors are realized by on-chip TLs, as shown in Fig. 4b. The fabricated DPA exhibits a power gain of 17 dB, a saturated output power of 41.3 dBm, a saturated PAE of 61%, and a 6-dB back-off PAE of 47% at 4.7 GHz, with a compact size of 3 mm×2.5 mm. Moreover, the 6-dB back-off PAE is better than 40% across a large bandwidth ranging from 4.4 to 5.1 GHz. Fig. 5 presents the chip photo and measurement results.

A dual-band DPA with hybrid operating modes for 5G mobile communication and vehicle network has been demonstrated (Lv et al., 2019c). Thus, 5G communication is a very big network composed of many different networks, such as the mobile communication network, Internet of Things, and Internet of Vehicles, rather than just mobile communication. The performance requirements of PAs for different networks are usually not consistent. For example, a 5.8-GHz dedicated short-range communication (DSRC) system for the vehicle network adopts a simple modulation scheme and requires high saturation efficiency, while mobile communication uses complex modulation and high back-off efficiency is required because of the large PAPR. The dual-band PA proposed by Lv et al. (2019) operates at Doherty mode in the 3.5-GHz band for a high back-off efficiency, and it is operated at harmonically tuned class-AB mode at 5.8 GHz for

Table 2 Sub-6 GHz Doherty power amplifier monolithic microwave integrated circuit performance

Reference	Frequency (GHz)	BW (GHz)	P_{sat} (dBm)	Back-off PAE	Gain (dB)	Integration	Process	GaN die size (mm^2)
Gustafsson et al., 2013	6.8–8.5	1.7	35	24%–37%@9 dB	9	Full	GaN	3.2
Camarchia et al., 2013b	7.0	0.35	37	47%@7 dB[a]	10	Full	GaN	21.6
Piazzon et al., 2014	7.0	1.0	38	36%@7 dB	10.5	Full	GaN	25
Gustafsson et al., 2014	5.8–8.8	3.0	36	31%–39%@9 dB	9	Full	GaN	8.4
Giofre and Colantonio, 2017	7.0	0.6	38	41%@6 dB	16	Full	GaN	9.0
Gustafsson et al., 2016	6.5	NA	42	21%@9 dB	18	Hybrid	GaN+GaAs	4.1
Ayad et al., 2017	5.5–6.5	1.0	43.5 44[b]	23%@9 dB 35%@9 dB[b]	11 12.5[b]	Hybrid	GaN+GaAs	2.6
Kim et al., 2014	2.14	NA	40.5	52.2%@7.3 dB[a]	15.7	Partial	GaN+PCB	8.6
Jee et al., 2015	2.1–2.7	0.6	41	55%@8 dB[a]	14	Partial	GaN+PCB	5.0
Lee et al., 2017a	2.6	NA	44	54.2%@6 dB[a]	13.7	Full	GaN	4.7
Lee et al., 2017b	2.6	NA	40.5	52.2%@6.5 dB[a]	13.8	Full	GaN	3.1
Maroldt and Ercoli, 2017	3.3–3.6	0.3	44.3	44%@6 dB	28	Hybrid	GaN+GaAs	NA
Ishikawa et al., 2018	4.0–4.5	0.5	36	44%@6 dB	17	Full	GaN	3.5
Li SH et al., 2018	5.1–5.9	0.8	38.7	49.5%@6 dB	14.4	Full	GaN	1.9
Lv et al., 2019d	4.4–5.1	0.7	42	47%@6 dB	17	Full	GaN	7.5
Lv et al., 2019b	4.5–5.2	0.7	41.2	45%@6 dB	11.6	Full	GaN	2.9
Lv et al., 2019c	3.3–3.8	0.5	42.6	51%@6 dB[a]	12	Full	GaN	5.8

[a] Drain efficiency. [b] Dual input. BW: bandwidth; PAE: power added efficiency. P_{sat}: saturated output power. NA: not available

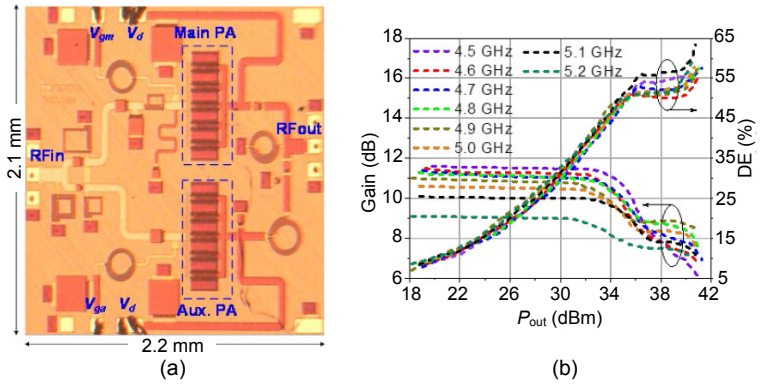

Fig. 3 Fully integrated GaN Doherty power amplifier monolithic microwave integrated circuit: (a) chip photo; (b) measurement results

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a high saturation efficiency. At Doherty mode, the main PA is biased at class AB, and the auxiliary PA is biased at class C. A 6-dB back-off efficiency of 51% is realized at 3.5 GHz (Fig. 6a). At class-AB mode, both main PA and auxiliary PA are biased at class AB, and second harmonic tuning is applied in the output matching network of the auxiliary PA. A saturation efficiency of 55% is achieved at 5.8 GHz (Fig. 6b).

Note that one of the main points of differentiation between PCB technology and MMIC technology is that, for the latter, we need to strictly comply with the design rules of the process, which requires access to and the use of process design kits (PDK). In addition, the MMIC process offers a limited DC-current density through metal layers. As a result of high drain bias voltage, the optimal load impedance is often

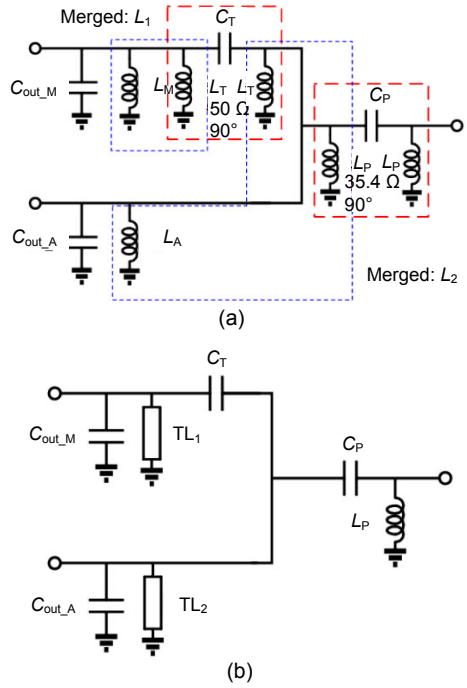

Fig. 4 Compact output network: (a) schematic before simplification; (b) final schematic with high-Q transmission lines

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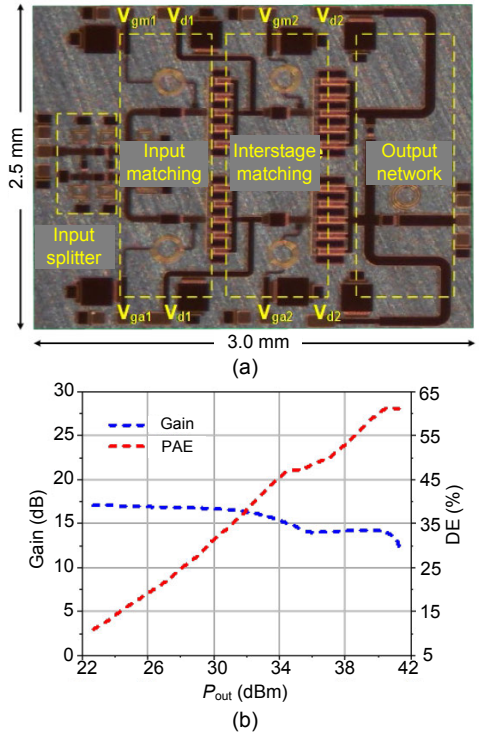

Fig. 5 Two-stage Doherty power amplifier: (a) chip photo; (b) measurement results at 4.7 GHz

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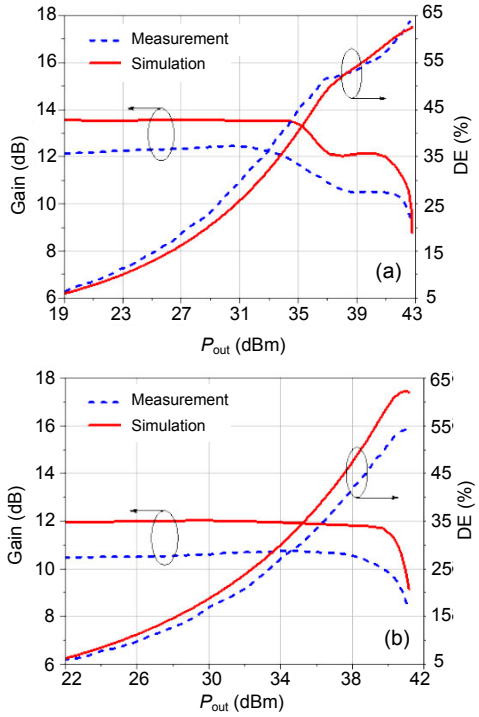

Fig. 6 Performance of the dual-band Doherty power amplifier with hybrid modes: (a) 3.5 GHz Doherty mode; (b) 5.8 GHz class-AB mode

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larger than 100 Ω, if the required output power is only in the range of several watts. The impedance inverting network (IIN) of a DPA with such a high characteristic impedance requires impractically narrow TLs. To overcome this limitation, a compact tee-network of TLs with feasible line widths is used (Li SH et al., 2018). Shunt inductors are required to neutralize the extra output capacitance of the main PA transistor and the auxiliary PA transistor. Then, the π-type inductor network is converted to a T-type network. The implemented DPA, as shown in Fig. 7, demonstrates a state-of-the-art performance with a 6-dB back-off PAE up to 49.5%. In addition, the measured X-parameters are used to investigate the DPA's nonlinear characteristics and verify the accuracy of conventionally used PA characterization/measurement methods for system-level design and testing applications.

3.2 DPA MMIC with hybrid integration

To reduce the cost of commercial chips and maintain the benefits of GaN technology, a 6.5 GHz hybrid DPA for microwave links has been designed

(Gustafsson et al., 2016). The GaN active devices are fabricated using a 0.25 μm GaN HEMT technology (United Monolithic Semiconductors), while all passive circuits are fabricated using the integrated GaAs process with high dielectric constant and low loss. The main and auxiliary PAs are both composed of two stages, and all dies are mounted on a single 9 mm× 9 mm quad-flat no-leads (QFN) package. The output network is designed together with bonding wires and the device's parasitics to realize an equivalent $\lambda/4$ TL behind the main PA and an equivalent $\lambda/2$ TL behind the auxiliary PA. However, the measurements exhibit a frequency offset and a reduction of bandwidth compared to the simulations, caused mainly by the model inaccuracy of bonding wires. An output power of 42 dBm and a PAE of 21% at 9 dB power back-off (PBO) are achieved at 6. 5 GHz, and the GaN die area is only 4.1 mm^2.

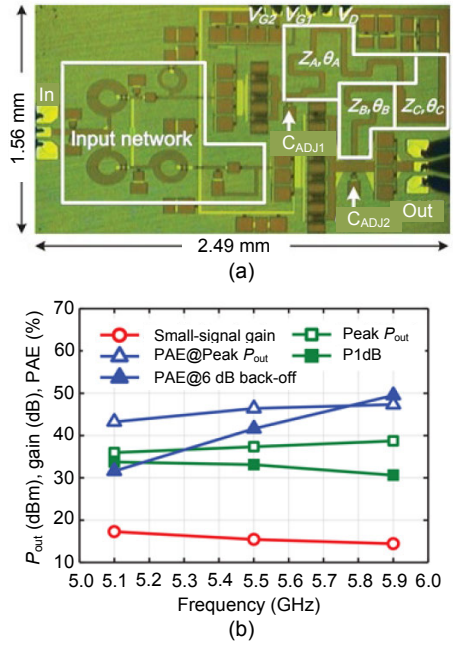

Fig. 7 GaN Doherty power amplifier monolithic microwave integrated circuit based on a tee-network: (a) layout; (b) experimental results

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A quasi-MMIC DPA operating in the range of 1.8–3.2 GHz is also presented (Quaglia et al., 2019). The power cells are based on Qorvo's AlGaN/GaN HEMT 0.25-μm high-voltage technology on SiC substrate, whereas the passive matching networks are realized using the Qorvo IPC3 passive component process on GaAs substrate. To increase the bandwidth, a two-stage high-pass filter is used to connect the main and auxiliary outputs with an impedance inverter of equivalent behavior, whereas an additional output matching is adopted to improve the matching of the auxiliary output at saturation. The design is based on a dual-input Doherty architecture. The lumped components values are adjusted to absorb the devices' capacitance and the bond wire effects, whereas the splitting ratio between the main and the auxiliary inputs is considered an additional degree of freedom during the design. The output power is higher than 42 dBm and the 6-dB back-off efficiency is higher than 38% over the 1.8–3.2 GHz frequency band.

Two 3.5-GHz MMIC DPAs for 5G mMIMO base station applications have been developed (Maroldt and Ercoli, 2017). High-gain two-stage GaN PA MMICs are designed as the cores of the DPAs. Area-consuming passive networks, such as input splitters and output combiners, are implemented on IPDs in the same QFN package. Fig. 8 presents the block diagram. To maximize the efficiency, the output combiner uses a parallel circuit class-E-like matching topology to properly terminate the output harmonics. A symmetrical version and an asymmetrical version of a DPA are both designed. The symmetrical DPA is fully integrated and yields a saturation output power of 44.3 dBm with 52% maximum PAE, and 44% PAE at 6 dB PBO. The asymmetrical DPA maintains an excellent efficiency of 40%–44% at a high PBO of 8.5–9 dB, in the range of 3.4–3.6 GHz.

3.3 DPA MMIC with partial integration

A compact 2.14 GHz DPA has been developed for small-cell base stations (Kim et al., 2014). The circuit is designed using lumped passives for size reduction. Note that lumped passives on MMICs, such as spiral inductors, usually degrade the efficiency due to their ohmic and substrate losses. Therefore, the major part of the PA is integrated on the MMIC die to achieve a small footprint, while low-loss surface-mounted off-chip inductors are used to enhance the efficiency. Fig. 9 shows the circuit diagram. High-Q chip inductors (obtained from Coilcraft) are mounted on a low-loss Taconic TLY PCB. The chip size is 3.3 mm×2.6 mm, and the total PA has a footprint of 1.1 cm×1.4 cm including all the off-chip

components. At 7.3 dB PBO, a DE of 52.2% and a power gain of 15.7 dB are achieved.

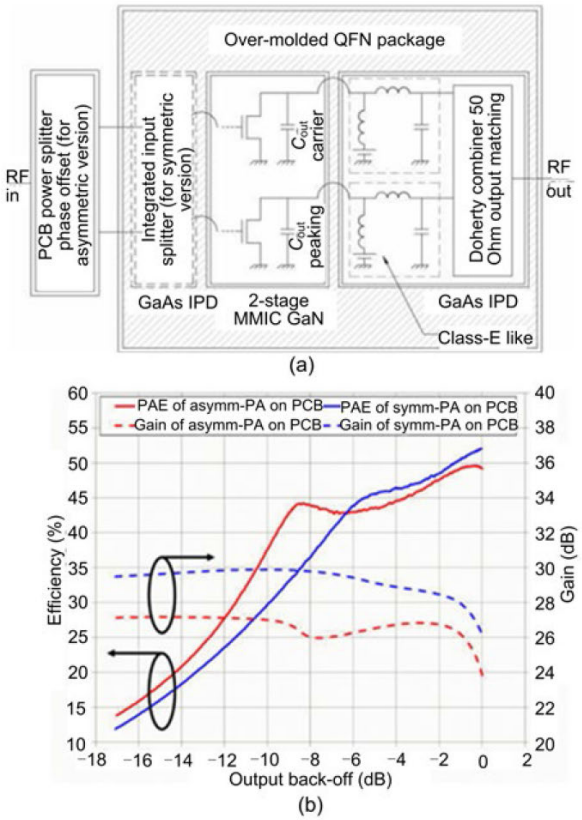

Fig. 8 A 3.5 GHz Doherty power amplifier with hybrid integration: (a) block diagram; (b) measurement results
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A 2.14 GHz two-stage DPA GaN MMIC has been presented in Lee J et al. (2014). The quadrature coupler based on a lumped-element magnetic coupler with capacitors is matched directly to the driver PA's optimum impedance, rather than matched to 50 Ω first and then to the optimum impedance. Thus, the size of the interstage matching network is reduced. The input matching network, interstage matching network, and all power cells are integrated in a GaN die, while the output combiner and biasing networks are implemented on the PCB. Fig. 10 presents the chip layout. Since the PCB-based output network exhibits lower loss, higher efficiency can be achieved. In addition, the size of the GaN die can be reduced, resulting in a lower cost. The fabricated DPA shows a saturated power of 41.2 dBm, a peak PAE of 56.2%, and a gain of 19.7 dB. For a downlink wideband code-division multiple access (WCDMA) signal, a PAE of 39.6% is achieved at an output power of 35.3 dBm. The area of the GaN Die is only 2.5 mm×2.7 mm.

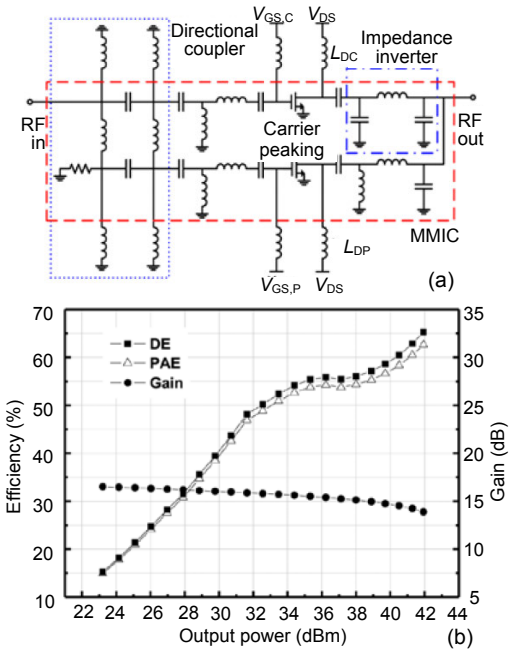

Fig. 9 A 2.14 GHz GaN Doherty power amplifier monolithic microwave integrated circuit with off-chip components: (a) circuit diagram; (b) measurement results
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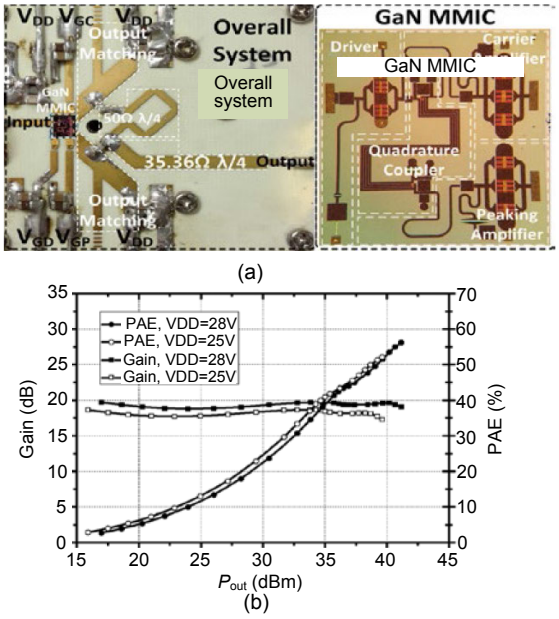

Fig. 10 Two-stage GaN Doherty power amplifier monolithic microwave integrated circuit with the PCB-based output network: (a) layout; (b) measurement results
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4 Design of mm-Wave DPA

The power requirement of the unit PA in mm-Wave MIMO phased-array transmitters is much lower than that in sub-6 GHz mMIMO transmitters, and this is mainly due to the large number of antenna elements in mm-Wave MIMO transmitters. In fact, the reported output power values of a single PA in such MIMO mm-Wave systems range from 10 to 30 dBm. Therefore, GaAs-, SiGe-, and CMOS-based processes can comfortably deliver such power, and hence they would be valuable process candidates for the design and manufacture of mm-Wave PA units. The design method of a PA in a compound semiconductor is very different from that in Si-based technology, so the research progress of mm-Wave DPAs is described in two subsections; the state-of-the-art mm-Wave DPAs are summarized in Table 3.

4.1 mm-Wave DPA based on III-V semiconductors

A Ka-band DPA implemented using a 0.15-μm E-mode GaAs process has been reported (Nguyen et al., 2017). Based on the low-*K* dielectric crossovers of the process, the authors proposed a meander broadside coupler with minimal size. As a result, an ultra-compact DPA with the size of 2.2 mm×1.3 mm is

Table 3 mm-Wave Doherty power amplifier performance

Reference	Frequency (GHz)	BW (GHz)	P_{sat} (dBm)	Peak PAE	Back-off PAE	Gain (dB)	Process	Area (mm^2)
Curtis et al., 2013	26.4	NA	25.1	38.0%	27%@6 dB	10.3	D-mode 0.15 μm GaAs	25
Quaglia et al., 2014a	24	2.4	30.9	38.0%	20%@6 dB	12.5	D-mode 0.15 μm GaAs	4.29
Nguyen DP et al., 2017	28	NA	26	40.0%	29%@6 dB	12	E-mode 0.15 μm GaAs	2.86
Nguyen DP et al., 2018a	29.5	1.0	27	38.0%	32%@6 dB	10.5	E-mode 0.15 μm GaAs	4.59
Nguyen DP et al., 2018b	28	1.25	28.7	37.0%	27%@6 dB	14.4	E-mode 0.15 μm GaAs	4.93
Lv et al., 2018b	31.1	2.8	26.3	35.0%	28%@7 dB	14	E-mode 0.15 μm GaAs	3.57
Lv et al., 2019a	29	2	25.4	33.0%	22%@6 dB	16	D-mode 0.1 μm GaAs	3.08
	46	2	25.2	25.0%	17%@6 dB	10.5		
Guo et al., 2018	26	NA	32	21.7%	20%@6 dB	13.6	0.15 μm GaN on SiC	5
Nakatani et al., 2018	28.5	2	35.6	25.5%	22.7%@6 dB	15.8	0.15 μm GaN on SiC	4.32
Giofre et al., 2019	28	1	32	30.0%	30%@6 dB	13	0.1 μm GaN on Si	6
Agah et al., 2012	42	NA	18	23.0%	17%@6 dB	7	45 nm CMOS SOI	0.64
Kaymaksut et al., 2015	72	19	21	13.6%	7%@6 dB	18.5	40 nm CMOS	0.96
Hu S et al., 2017	28	NA	16.8	20.3%	13.9%@5.9 dB	18.2	0.13 μm SiGe	1.76
	37	NA	17.1	22.6%	16.6%@6 dB	17.1		
	39	NA	17	21.4%	12.6%@6.7 dB	16.6		
Chen SC et al., 2017	60	7	13.2	22.0%[a]	10.6%@6 dB[a]	NA	65 nm CMOS	0.43
Özen et al., 2017	30	1	21	17.0%	24.3%@6 dB	6.7	0.13 μm SiGe	1.87
Indirayanti and Reynaert, 2017	32	5	19.8	21.0%	12.8%@OP1dB	22	28 nm CMOS	1.79
Chen D et al., 2018	60	8	14.9	16.8%	8.7%@6 dB	18	65 nm CMOS	0.195
Nguyen HT et al., 2018	65	6	19.4	27.5%	20.1%@6 dB	12.5	45 nm CMOS SOI	3.23
Rostomyan et al., 2018	28	6	22.4	40.0%	28%@6 dB	10	45 nm CMOS SOI	0.63

[a] Drain efficiency. BW: bandwidth; PAE: power added efficiency. P_{sat}: saturated output power. NA: not available

realized. At 28 GHz, the measured saturated power is 26 dBm, and the 6-dB back-off PAE goes up to 29%. To further improve the back-off efficiency, an asymmetrical DPA using a novel load-pull-based design technique has also been demonstrated (Nguyen DP et al., 2018a). A new load modulation scheme is proposed to optimize the efficiency at a desired back-off level. The asymmetrical ratio is determined based on the empirical load-pull data, instead of the current profile in the conventional design approach. A recorded PAE of 32% at 6 dB PBO and 28.5% at 8 dB PBO are achieved at 29.5 GHz. A similar load-pull-based design method has also been shown by Lv et al. (2018b), but the offset line behind the main PA is removed by choosing an appropriate output matching network, which results in a compact size of 2.1 mm× 1.7 mm and a large bandwidth of 2.8 GHz. The 7-dB back-off PAE is better than 21% in the frequency of 29–31.8 GHz, and a maximum value of 28% is observed at 31.1 GHz (Fig. 11).

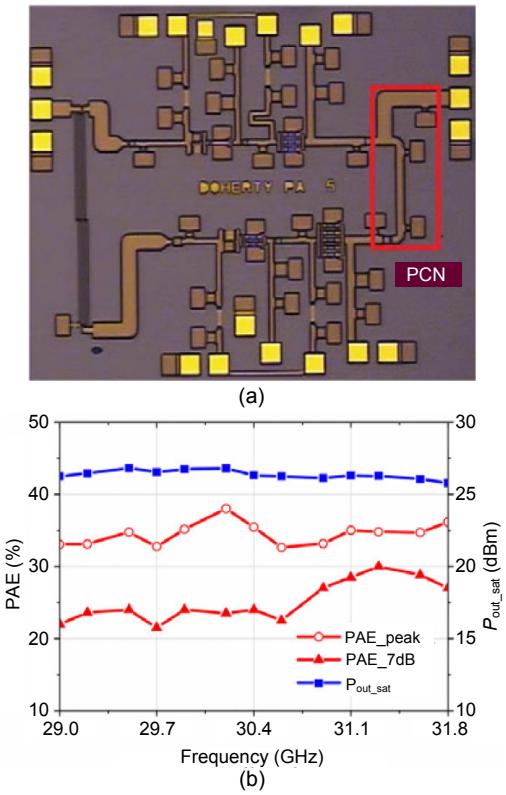

Fig. 11 Broadband Ka-band GaAs Doherty power amplifier monolithic microwave integrated circuit: (a) chip photo; (b) measurement results

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A Ka/Q dual-band DPA has been implemented using a 0.1-μm GaAs process (Lv et al., 2019a). Dual-band TLs used in the sub-6 GHz dual-band DPA are not suitable to be used as the offset lines in mm-Wave dual-band DPAs due to their large sizes and insertion losses. An in-depth analysis reveals that the phase requirement of the offset lines can be relaxed, and that the DPA exhibits a reasonable performance in a certain phase shift range. A novel design method is proposed to realize offset lines using simple TLs, which can satisfy the phase shift ranges in dual bands by choosing a proper electrical length. To enhance the gain of the DPA, a reversed uneven power splitter is adopted to deliver more power to the main PA. The fabricated DPA achieves an output power of 25.4/25.2 dBm, a peak PAE of 33%/25%, and a 6-dB back-off PAE of 22%/17% at 29/46 GHz, with a compact size of 2.2 mm×1.4 mm. Note that this work is the first demonstration of mm-Wave dual-band DPAs that do not require any additional switching or reconfiguration. Chip photo and measurement results are shown in Fig. 12.

GaN technology is attractive for 5G applications in view of its high power capability and high efficiency; nevertheless, reports on mm-Wave GaN DPAs are scarce (Campbell et al., 2012; Guo et al., 2018; Nakatani et al., 2018; Valenta et al., 2018; Giofre et al., 2019). A K-band GaN DPA has been presented previously (Campbell et al., 2012). At 23 GHz, the PAE at 8 dB input PBO from the 1 dB gain compression point is 25%, while the saturated power is over 5 W. A 26-GHz GaN MMIC DPA (Guo et al., 2018) exhibits a 6 dB back-off PAE of 20%, but the saturated output power is only 32 dBm. The Ka-band DPA in Nakatani et al. (2018) demonstrates a saturation output power of 35.6 dBm and a 6-dB back-off PAE of 22.7% at 28.5 GHz. These designs are all based on the 0.15-μm GaN-on-SiC process. In Giofre et al. (2019), a 28 GHz DPA based on a 0.1-μm GaN-on-Si process is demonstrated. The GaN-on-Si process allows to exploit the key features of most common GaN-SiC technologies, while ensuring significant benefits especially in terms of production cost, owing to the use of larger wafers. At 28 GHz, the measured gain and the output power are close to 13 dB and 32 dBm, respectively, whereas the PAE remains higher than 30% in 6-dB output PBO.

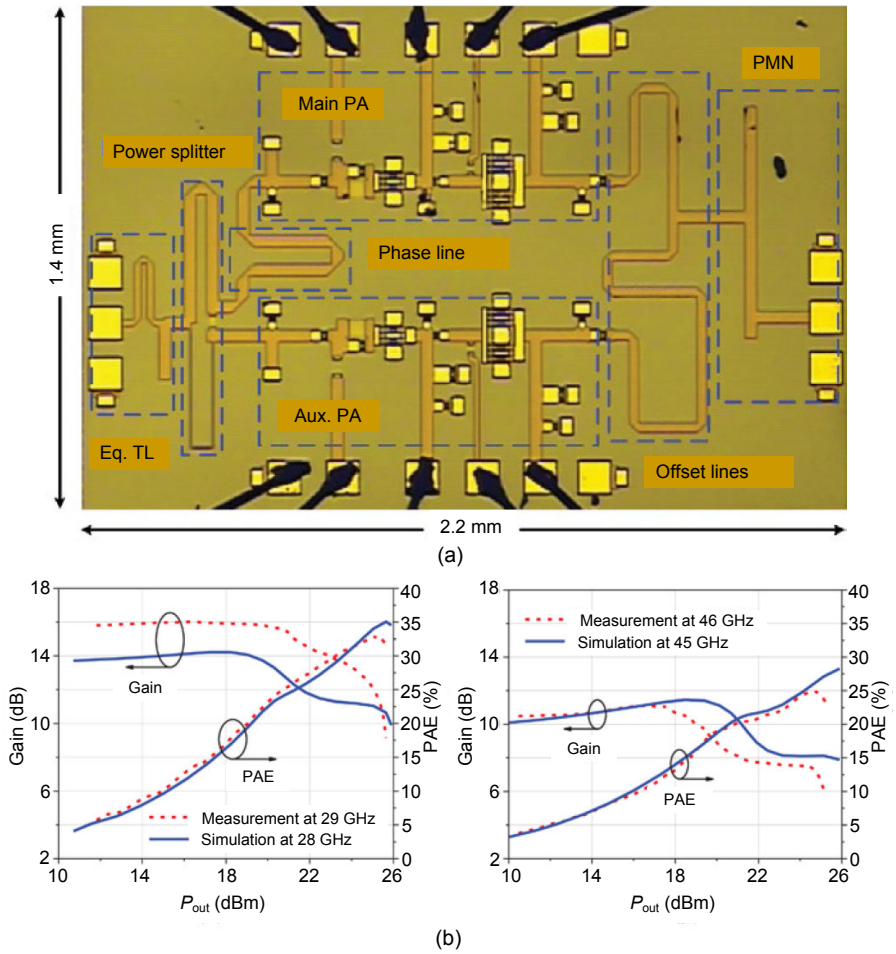

Fig. 12 Ka/Q dual-band GaAs Doherty power amplifier monolithic microwave integrated circuit: (a) chip photo; (b) measurement results

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4.2 mm-Wave DPA based on the Si-based process

A 45-GHz DPA implemented in 45 nm CMOS silicon on insulator (SOI) has been reported (Agah et al., 2012). Two-stack field-effect transistor (FET) amplifiers are used as main and auxiliary amplifiers to enhance the output power. The use of slow-wave coplanar waveguides (CPW) improves the PAE and gain remarkably, and the die area is also reduced by 20%. The DPA exhibits more than 18 dBm saturated output power, with a peak gain of 7 dB. The peak PAE and 6 dB PBO PAE are 23% and 17%, respectively. The quarter wavelength TL at the input of the auxiliary amplifier is replaced by an amplifier in Agah et al. (2013), to increase the gain of DPA and reduce the occupied area. The gain and PAE at 6 dB PBO are 8 dB and 20%, respectively, showing remarkable improvement compared to Agah et al. (2012).

In the Si-based technology process, it is convenient to implement a transformer architecture using the strong coupling between different metal layers; thus, the size of the DPA can be reduced by replacing the distributed TL-based divider and combiner with input and output transformers. An E-band DPA using transformers rather than TLs to achieve load modulation is demonstrated in a 40 nm CMOS-based process (Kaymaksut et al., 2015). An asymmetrical DPA structure with an asymmetrical transformer combiner is used to improve the back-off efficiency. A high output impedance of the auxiliary PA is achieved by inserting an additional LC tuning network. The implementation with cascode PA units demonstrates 21-dBm output power, with a peak PAE of 13.6% and a 6 dB PBO PAE of 7% at 72 GHz.

A 28-GHz DPA based on a 45-nm CMOS-based SOI process has been presented by Rostomyan et al. (2018). A state-of-the-art performance is achieved due to the use of a low-loss combiner synthesis technique. Impedance inversion and parasitic compensation are integrated in one compact network, leading to a loss reduction of 1 dB. The fabricated DPA exhibits a peak PAE of 40%, and a 6 dB PBO PAE of 28% (Fig. 13). A high output power of 22.4 dBm is achieved using two stacked power devices. Moreover, the PAE at 6 dB PBO is higher than 19% in the frequency range of 25–31 GHz.

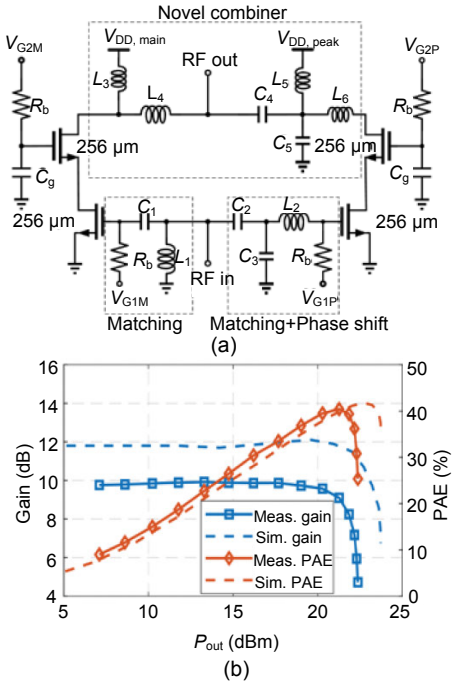

Fig. 13 A 28-GHz Doherty power amplifier in CMOS SOI: (a) schematic representation; (b) experimental results
Reprinted from Rostomyan et al. (2018), Copyright 2018, with permission from IEEE

Multiple mm-Wave frequency bands have been opened for 5G development. Multiband operations will greatly facilitate future cross-network/international roaming and enable ultracompact mMIMO 5G systems. In this context, a fully integrated 28/37/39 GHz multiband DPA is demonstrated using 0.13-μm SiGe BiCMOS (Hu S et al., 2017). It achieves +16.8/+17.1/+17 dBm peak output power, 18.2/17.1/16.6 dB peak power gain, 29.4%/27.6%/28.2% peak collector efficiency (CE), and CE of 25.4%@5.9 dB/26%@6 dB/20.6%@6.7 dB PBO at 28/37/39 GHz, respectively. A transformer-based output network with reduced impedance transformation ratios in PBO is used to broaden the bandwidth of the DPA. The relative phase of the main path relative to the auxiliary path is adjusted using nine-section varactor-loaded TLs. In consequence, the bandwidth is extended significantly using different varactor settings for 28/37/39 GHz. Fig. 14 presents the chip photo for clarification.

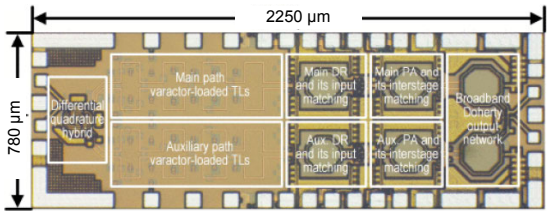

Fig. 14 Chip photo of the 28/37/39 GHz multiband Doherty power amplifier
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5 DPD for the mMIMO system

DPD, recognized as one of the most common amplifier linearization techniques, is ubiquitous in transmitters such that the system can operate at high efficiency while maintaining high quality of the signal (Ghannouchi and Hammi, 2009). In 5G mMIMO systems, due to the expansion of signal bandwidth and cross-antenna interactions, the linearity requirement is inherently stringent such that implementing the linearization techniques is still needed in an mMIMO system. In the sub-6 GHz band, fully digital BF architectures are preferred for the sake of high spectrum efficiency; the DPD method performs PA linearization. In the mm-Wave band, it is almost impractical to transplant conventional DPD in 4G transmitters mainly due to the hybrid BF architecture. Thus, with the introduction of an active antenna system and hybrid transmitter architecture, the DPD implementation faces new challenges in the mMIMO system, as in the following.

1. Nowadays, the higher data transmission rate requirements and crowded spectrum resources encourage the development of spatial multiplexing, such that deploying multiple antennas in most communication systems including the transmitters and

end users will become a tendency. Due to the mutual coupling and crosstalk among multiple channels, conventional SISO DPD problems extend to MIMO DPD problems. In previous work, various MIMO DPD methods, such as the crossover memory polynomial model (CO-MPM) and augmented crossover memory polynomial model (ACO-MPM), are implemented to linearize 2×2 MIMO transmitters and compensate for the linear crosstalk between the antenna elements and within the feed network (Bassam et al., 2009; Abdelhafiz et al., 2016); however, when it comes to the mMIMO scenario, most of the present MIMO DPD models become extremely complex and impractical to use in an actual system. Therefore, low-complexity DPD algorithms suitable for mMIMO systems are urged to be developed for the sake of low power consumption and hardware cost.

2. In some scenarios, hybrid BF architectures are adopted to strike a trade-off between computational complexity and the data transmission rate, especially in the mm-Wave band transmitters with hundreds of antennas. The conventional DPD schemes, which require a dedicated predistorter and feedback loop per PA, face implementation difficulties in hybrid mMIMO transmitters, since the number of digital streams is much smaller than that of RF chains and the PD signal that drives multiple phased transmitting branches is anticipated to linearize multiple amplifiers simultaneously. Fig. 15 presents the block diagram of DPD implementation in a fully digital MIMO architecture and a hybrid architecture. Moreover, the nonlinear behavior of each PA might be different and each PA might be driven with a different power level, depending on the BF array's conditions. It is practically infeasible to identify a predistorter to linearize multiple PAs at the same time for each BF array setting. Novel DPD techniques and architectures are needed in such cases.

3. The hardware configurations of the feedback loop, including the coupler, down-converter, and ADC, are bulky in 5G mMIMO transmitters. The conventional DPD schemes require a dedicate feedback loop per PA to observe its nonlinear behavior. However, due to the expansion of the array scale and the integration of antennas and PAs per RF chain, it is almost practically non-feasible to fulfill conventional DPD feedbacks in future 5G systems. Furthermore, simplified feedback methods and real-time operating DPD blocks that can be updated and trained online are urged to be solved.

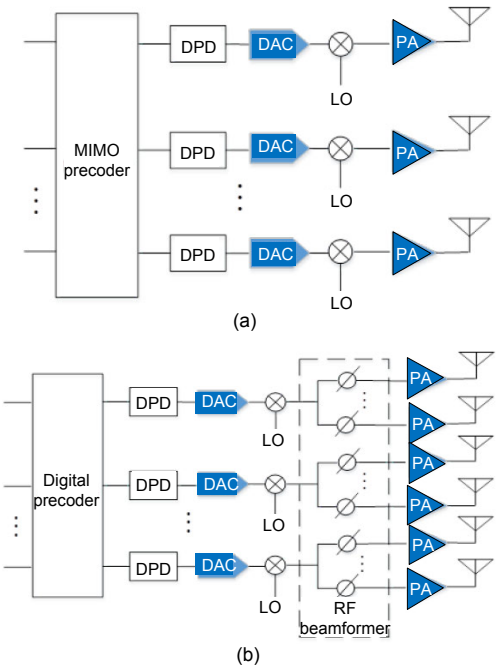

Fig. 15 Block diagram of digital predistortion implementation in a fully digital MIMO architecture (a) and a hybrid beamforming architecture (b)

As the signal bandwidth drastically increases in the 5G system, particularly for the mm-Wave band scenarios, where the bandwidth is up to 800 MHz, the requirements for extremely high sampling rates of DAC and ADC, the demands for broadband components in RF chains, and the cost of baseband computation resources become increasingly stringent and limit the application of DPD techniques. Thus, the study on high-performance and low-cost DPD schemes suitable for 5G mMIMO systems has been an active research area recently, and several promising apparatuses are proposed and prototyping efforts made. In this review, the present mMIMO DPD techniques have been investigated and summarized according to their suitable transmitter architectures, i.e., the fully digital BF architecture and hybrid or analog BF architectures.

5.1 DPD in a fully digital MIMO architecture

In the 5G sub-6 GHz band, the fully digital MIMO architectures are still preferable for the sake of spectrum efficiency. In a typical MIMO system, the

transmitter serves multiple users simultaneously so that the transmitted signal in each branch may not be correlated. Due to cross-channel coupling or the leakage through the common local oscillator (LO), the nonlinear behavior of each PA might be affected by the adjacent channels' behavior and the SISO DPDs are no longer capable of linearizing the multi-antenna system with strong crosstalk. According to where the crosstalk occurs, the crosstalk can be divided into two categories: (1) nonlinear crosstalk occurs before PA; (2) linear crosstalk occurs after PA, between the antenna element and within the feed network (Bassam et al., 2009). The crosstalk cancellation for MIMO transmitters has been investigated for a while, and several of MIMO DPD apparatuses and models have been proposed to linearize small multiple antenna systems. Bassam et al. (2009) have proposed a CO-MPM to compensate for the linear crosstalk; the model output is the sum of memory polynomial series formed by other branches' signal. Thus, the performance of the CO-MPM degrades when strong nonlinear crosstalk occurs. The ACO-MPM proposed by Abdelhafiz et al. (2016) modifies and simplifies the CO-MPM to realize better linearization performance while keeping the same number of coefficients. Amin et al. (2014) introduced a 2×2 parallel Hammerstein (PH) model to linearize 2×2 MIMO transmitters with both linear and nonlinear crosstalk. The 2×2 PH model is formed by the sum of dual-input memory polynomial functions and can scale to *M*-channel scenarios. A few more methods have been presented for compensation of crosstalk and PA nonlinearities in MIMO transmitters (Suryasarman and Springer, 2015; Vaezi et al., 2017).

Theoretically, linear and nonlinear crosstalk can be simultaneously compensated for by a full *M*-input *M*-output DPD model; however, the number of coefficients increases as the transmitter array scale expands. These techniques usually use the *M*-input nonlinear function to reflect the interaction of all branches, leading to an explosive growth in complexity with increasing *M*. It seems that reducing the nonlinear and crosstalk order in the model is a reasonable method for simplification, but it compromises the linearization performance and therefore is suitable only for weakly nonlinear crosstalk systems.

To avoid the explosive growth of model coefficients in mMIMO systems, novel model architectures need to be investigated. Hausmair et al. (2017, 2018a) and Barradas et al. (2017) proposed a different approach to rethink the linearization of *M*-channel MIMO transmitters, which uses some dual-input models as alternatives for the conventional *M*-dimensional model. In the dual-input model, the first input branch contains only the input information, while the second one copes with the crosstalk and load mismatch due to the mutual coupling as a weighted linear sum of output signals from the remaining transmitting branches. Therefore, the multiport *S*-parameters of the antenna array can be incorporated into the second input of the dual-input model to describe the cross-antenna interaction. Since the antenna network is linear and passive, the complexity for modeling the crosstalk and load modulation grows linearly with *M* and therefore yields affordable model coefficients. Fig. 16 demonstrates the architecture of the dual-input DPD model proposed by Hausmair et al. (2018a). Luo et al. (2018b) proposed a similar DPD approach while using a canonical piecewise linear function based model instead of the commonly used generalized memory polynomial model.

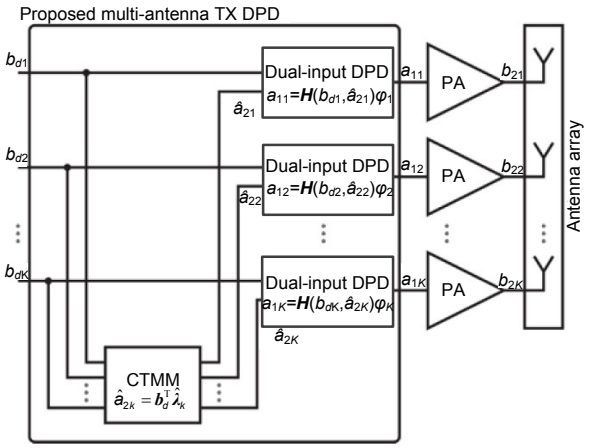

Fig. 16 Block diagram of the dual-input digital predistortion model for the multi-antenna transmitter
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In addition, there are a few more works on the DPD algorithm in fully digital mMIMO systems. Abdelaziz et al. (2017) proposed a DPD parameter estimation approach with a very simple decorrelation-based closed-loop processing and reduced-bandwidth observation for mMIMO transmitters. To reduce the

model order, Yao et al. (2018) suggested to adapt the channel and PA distortion iteratively by cascading adaptive zero-forcing precoding and the DPD module, while Yu et al. (2019) proposed simplification of the conventional DPD architecture using a two-stage DPD block, by compensating for the differences of PAs in different transmitter chains first and then linearizing the whole array with a common model.

5.2 DPD in hybrid and analog BF architectures

As aforementioned, hybrid BF architectures are widely adopted in mm-Wave mMIMO systems, and therefore the research of DPD in such cases has been a hot topic recently. In both hybrid and analog BF architectures, a digital stream drives multiple RF phased transmitting branches so that the DPD schemes in these two architectures are similar in some cases. Since the number of digital streams is much smaller than that of RF chains in hybrid mMIMO or phased-array transmitters, the use of conventional techniques using one DPD per PA is practically non-feasible in such systems. Therefore, a single DPD block that drives multiple phased transmitting branches that include one PA per branch is more appropriate and practically feasible for hybrid and phased-array mMIMO systems, provided that all the PAs in the array are identical. Unfortunately, due to mutual coupling, beam steering-associated load modulation, and other nonideal factors such as the fabrication error and aging, the PAs in an array usually have different nonlinear characteristics. Furthermore, some power control mechanisms that alter not only the phase but also the gain of each PA's input are adopted in some cases to better shape the beam pattern; hence, the PAs might be driven with different power levels, and thus it is practically infeasible to identify a predistorter to linearize multiple PAs simultaneously using the conventional DPD scheme.

Some early-stage articles simplify the implementation issue with some ideal assumptions. Liu L et al. (2016) proposed an apparatus using a "single DPD" block, which assumes that the PAs in the array are similar, and suggested a relatively simple approach to observe and linearize only one single PA and apply the model for the remaining PAs in the array. The "single DPD" methods are simple to implement; however, due to the presence of the fabrication error, heat variation, varying power control mechanisms, and other nonideal factors, the PAs in an array display different nonlinear behaviors such that the performance of the single DPD will be compromised. Similarly, Yan and Cabric (2017) assumed that all PAs in an array are identical and linearize the combined response of the PAs, while Lee S et al. (2015) introduced an iterative algorithm to identify the predistorter for each array.

Recently, many researchers have directed their efforts on the implementation of hybrid BF mMIMO DPD or the linearization of the phased array, and some instructive prototyping models and ideas have been proposed; among them, the idea of linearizing the main beam signal rather than the individual PAs to cope with the DPD implementation dilemma in hybrid mMIMO transmitters has promising prospects and has aroused wide research interest (Tervo et al., 2017; Abdelaziz et al., 2018; Liu X et al., 2018). Tervo et al. (2017) proposed to linearize the over-the-air (OTA) response of a phased array, which offers an instructive way of hybrid mMIMO array linearization over multiple PAs. Liu X et al. (2018) proposed the beam-oriented DPD (BO-DPD) scheme to construct and linearize a "virtual" main beam signal with the real-time BF conditions and thereafter validated the proposed DPD by both simulation and experimental measurements. Fig. 17 presents the block diagram of the proposed BO-DPD scheme. Measurement results show that the nonlinear distortion in the main beam direction, i.e., the end-user's direction, is significantly eliminated to meet the required signal quality, and the interference in other directions is also investigated. Similarly, Abdelaziz et al. (2018) presented an idea for linearizing the signal in the beam steering direction, while the main beam estimation methods are totally different.

Previous works have provided an alternative way to rethink the concept of linearizing hybrid mMIMO systems; however, the feedback loop or linearization performance must pay the price. For example, the BO-DPD technique necessitates the feedback loop of each PA to acquire the output information for the main beam signal estimation, which is bulky, expensive, and even infeasible in some of the 5G mMIMO transmitters (e.g., mm-Wave scenarios), wherein the PAs and antennas are usually integrated on a chip. To avoid the cumbersome feedback configurations, Li HM et al. (2018) used only one

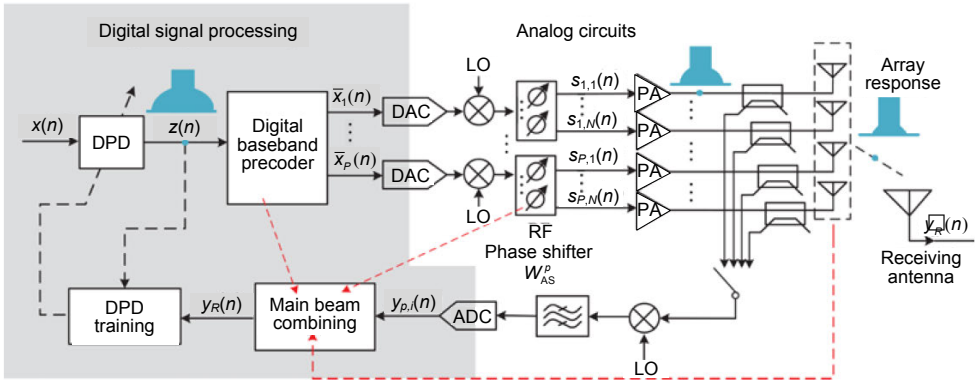

Fig. 17 Beam-oriented digital predistortion structure in a hybrid beamforming array
Reprinted from Liu X et al. (2018), Copyright 2018, with permission from IEEE

feedback of the selected PA to extract an all-PA-shared forward model and then synthesized the received signal with the estimated PAs' outputs, while Choi and Jeong (2012) and Park CW et al. (2016) combined the outputs from the PAs before they are sampled in an observation receiver.

Furthermore, the OTA setup may be a promising solution for the DPD feedback loop. Ng et al. (2018, 2019) and Luo et al. (2018a) used an external observation receiver in the far field to capture the array's response directly. Fig. 18 shows the experimental setups with OTA observation for DPD validation (Ng et al., 2019). Although identification of the predistorter is simplified using the far-field observation, this feedback setup is still difficult to implement because the receiver placed in the far field will lead to low signal-to-noise ratios (SNR) of the feedback signal such that the nonlinear components are submerged under the noise floor, and constructing the feedback loop from the far field to the transmitter is also infeasible. In contrast to the external feedback setups, Hausmair et al. (2018b) and Liu et al. (2019a, 2019b) used the observation antennas embedded in the transmitting array, which is practically more feasible in hybrid mMIMO systems.

6 Linearity enhancement through circuit design

To relieve the linearization burden of DPD, many researchers are seeking novel analog or low power consumption linearization schemes to enhance PA linearity. In mm-Wave hybrid mMIMO systems, the linearity requirements are lower than in the case of

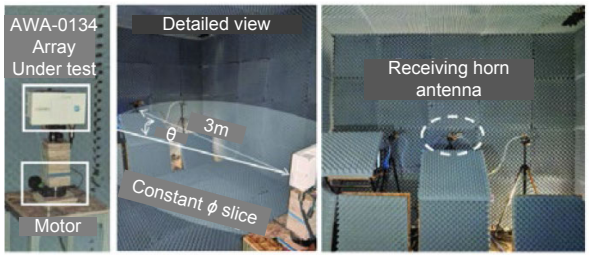

Fig. 18 A 2×64 element array experimental measurement setup, including the AWA-0134 antenna under test (left), a detailed view (center), and the view in front of the array (right)
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sub-6 GHz systems due to the lower power output of each PA, and the circuit-level linearization design will be useful. Even if DPDs are used mostly in the sub-6 GHz band to compensate for nonlinearity, linearity enhancement design methods are also found to be able to reduce DPD complexity and its associated power consumption. The analog linearization methods can be divided into two main categories of nonlinearity compensation and enhancement circuits.

6.1 Nonlinearity compensation

Analog nonlinearity compensation methods include mainly a linear gain/attenuation unit, a PD unit for amplitude-to-amplitude modulation (AM-AM) and amplitude-to-phase modulation (AM-PM). The early-stage APD method uses a linear bias offset to stabilize the DC operating point (Yamauchi et al., 1997; Yoshimasu et al., 1998). The conventional bias circuit is constructed by a resistance network. Due to the nonlinearity of the base-emitter diode of the input

amplification transistor, the DC operating point will decrease at large signals, resulting in a decrease in the transconductance and gain. An adaptive linearization bias can effectively compensate for the gain compression and phase distortion under large signal conditions by stabilizing the DC operating point, as shown in Fig. 19 (Wang DH et al., 2019).

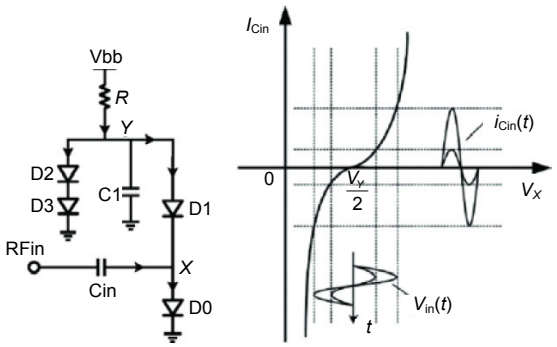

Fig. 19 The equivalent circuit of the linearization bias circuit and its input *I-V* characteristic curve
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Another alternative solution is to compensate for the PA nonlinearities with cascaded analog predistorters, as shown in Fig. 20a (Tsai et al., 2006). A common method for PD of AM-AM characteristics is to use cold-mode FET (Tsai et al., 2006, 2011; Kao et al., 2013). The equivalent circuit of the cold-mode FET can be expressed as a parallel combination of a capacitor series with a small resistor and a current source (Fig. 20b). When the input power increases, the slope of the DC *I-V* curve decreases, which results in increased R_{ds} (equivalent resistance of HEMT2), so that the cold-mode FET linearizer can achieve a positive gain and compensate for the gain of the PA.

Many studies also focus on using positive channel metal oxide semiconductor (PMOS) transistors to compensate for the AM-PM distortion caused by the nonlinear input capacitance of a negative channel metal oxide semiconductor (NMOS) transistor (Wang CZ et al., 2004; Kulkarni and Reynaert, 2014, 2016; Xi et al., 2017; Vigilante and Reynaert, 2018). A PMOS varactor is used to compensate for the nonlinearity of the input capacitance (Fig. 21); thus, the net AM-PM distortion is reduced. According to the experimental results, the analog AM-PM correction method is a promising solution for mm-Wave PA linearization, which is expected to satisfy the PA specifications in 5G mMIMO.

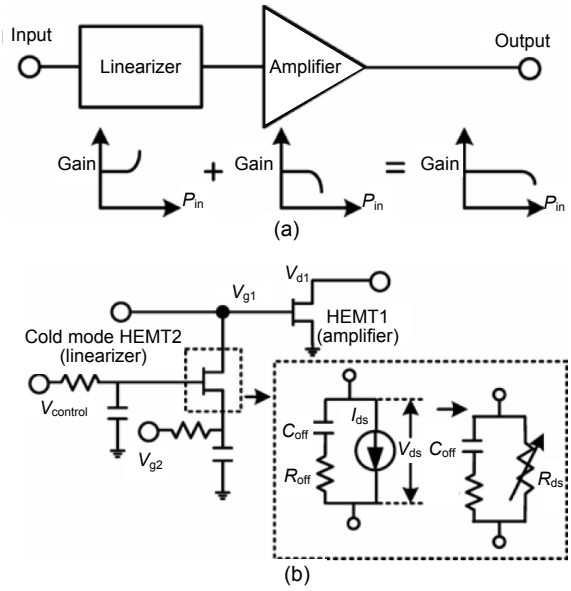

Fig. 20 Block diagram of analog predistortion: (a) principle of the analog predistorter; (b) equivalent circuit model of cold-mode FET
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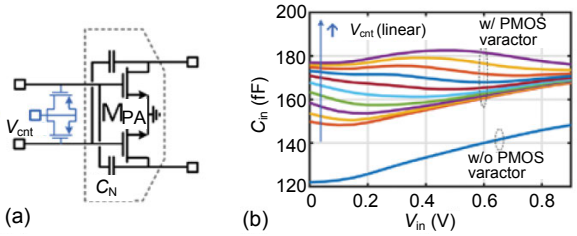

Fig. 21 Simplified schematic of neutralized common source power amplifiers with input PMOS varactors for linearization (a) and power amplifier input capacitance vs. input voltage with and without a PMOS varactor at the input, where V_{cnt} is swept linearly from 0 to 900 mV (b)
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6.2 Linearity enhancement circuits

The primary methods for using linearity enhancement circuits to improve the linearity of amplifiers include antiphase techniques, feedback, multigate transistors, third-order intercept cancellations, and harmonic short circuit. The antiphase technique is a method for cancellation of the third-order intermodulation distortions (IMD3s) between the driver and the power stages of the PA (Lu et al., 2007; Choi et al., 2010; Joo et al., 2013; Park B et al., 2016, Park J et al., 2017b). This is achieved by the opposite sign gm3 of each stage. The driver stage generates

positive-sign IMD3s, which can pass through the interstage matching network because they appear close to the signals to be transmitted. At this time, the positive-sign IMD3s are still quite small, but after amplification in the power stage with the signals, the positive-sign IMD3s reach a sufficient size to cancel the negative-sign IMD3s generated in the power stage. Thus, the linearity of PA can be improved significantly.

The control of the second harmonic impedances can be a practical solution to reduce nonlinearity, because the memory effect is caused mainly by the reflections of the envelope frequency and second harmonics at the device terminals (Kang et al., 2006; Jin et al., 2013; François and Reynaert, 2015; Park B et al., 2016). A highly linear PA with harmonic short circuit has been achieved by Park B et al. (2016) (Fig. 22). By achieving second harmonic short circuit at both the source and the drain, the PA achieves good linearity.

7 Conclusions

In this paper, energy-efficient integrated DPA MMICs and linearization techniques are reviewed for both sub-6 GHz and mm-Wave 5G mMIMO systems. Different semiconductor processes and architectures are compared and analyzed, and the enhancement levels are investigated. Since the PA specifications for mMIMO are still under consideration and not yet finalized, it is worth proposing novel design methods to further improve their efficiency and linearity performance. Specifically, for PA linearization, the DPD techniques need to evolve to be adapted in mMIMO systems, and some creative techniques are expected to simultaneously improve the compensation accuracy and reduce the power consumption.

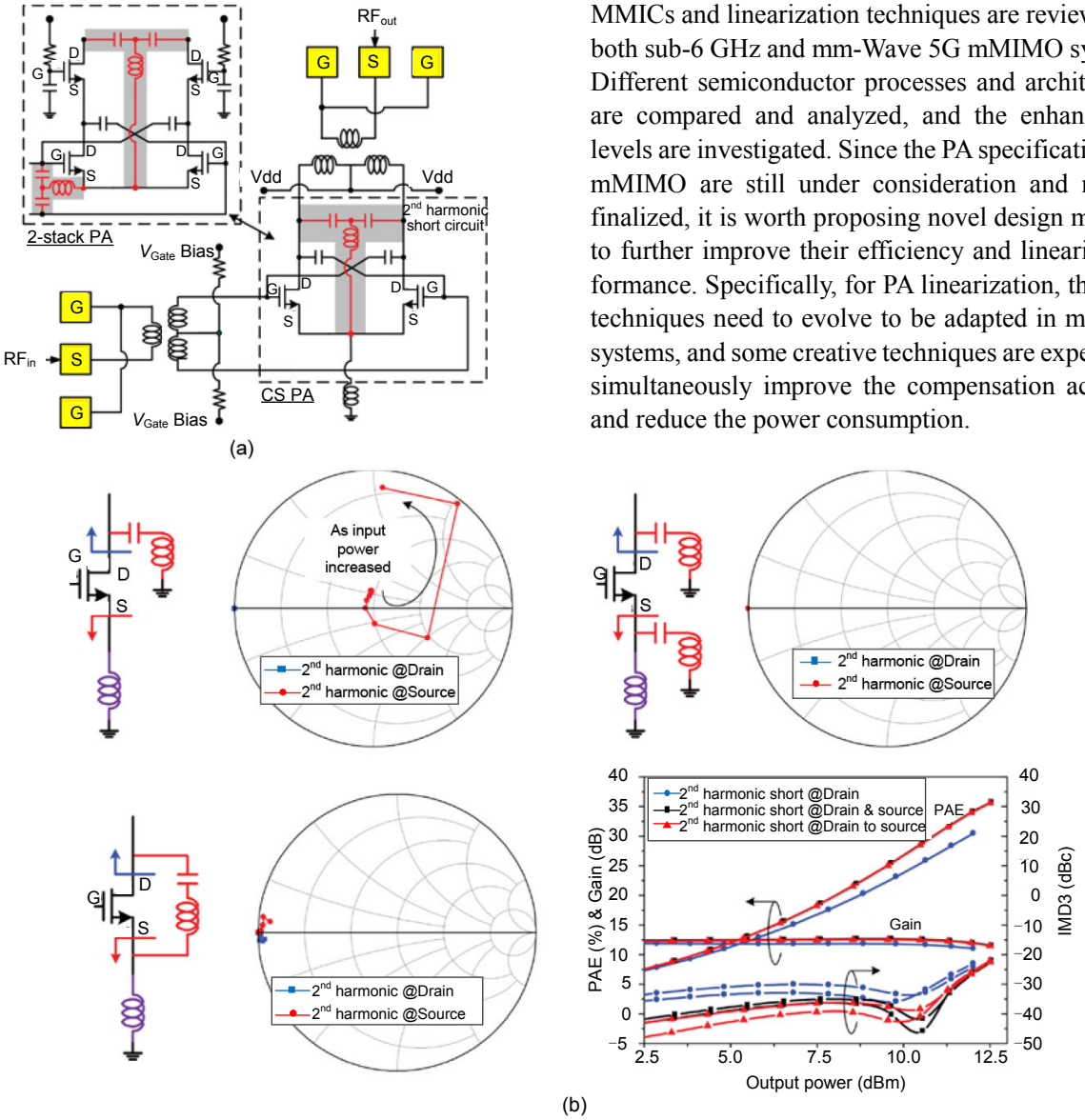

Fig. 22 Linearity enhancement by harmonic short circuit: (a) schematic representation of the designed power amplifier; (b) simulation results

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Contributors

Xin LIU, Guan-sheng LV, and De-han WANG wrote and edited the draft of the manuscript. Wen-hua CHEN and Fadhel M. GHANNOUCHI revised and edited the final version.

Compliance with ethics guidelines

Xin LIU, Guan-sheng LV, De-han WANG, Wen-hua CHEN, and Fadhel M. GHANNOUCHI declare that they have no conflict of interest.

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