Frontiers of Information Technology & Electronic Engineering
www.jzus.zju.edu.cn; engineering.cae.cn; www.springerlink.com
ISSN 2095-9184 (print); ISSN 2095-9230 (online)
E-mail: jzus@zju.edu.cn

Fractional-order memristive neural synaptic weighting achieved by pulse-based fracmemristor bridge circuit*

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Received Feb. 23, 2020; Revision accepted Aug. 23, 2020; Crosschecked May 8, 2021

Abstract: We propose a novel circuit for the fractional-order memristive neural synaptic weighting (FMNSW). The introduced circuit is different from the majority of the previous integer-order approaches and offers important advantages. Since the concept of memristor has been generalized from the classic integer-order memristor to the fractional-order memristor (fracmemristor), a challenging theoretical problem would be whether the fracmemristor can be employed to implement the fractional-order memristive synapses or not. In this research, characteristics of the FMNSW, realized by a pulse-based fracmemristor bridge circuit, are investigated. First, the circuit configuration of the FMNSW is explained using a pulse-based fracmemristor bridge circuit. Second, the mathematical proof of the fractional-order learning capability of the FMNSW is analyzed. Finally, experimental work and analyses of the electrical characteristics of the FMNSW are presented. Strong ability of the FMNSW in explaining the cellular mechanisms that underlie learning and memory, which is superior to the traditional integer-order memristive neural synaptic weighting, is considered a major advantage for the proposed circuit.

Key words: Fractional calculus; Fracmemristor; Fracmemristance; Fractional-order memristor; Fractional-order memristive synapses

https://doi.org/10.1631/FITEE.2000085 **CLC number:** TP183; TN6

1 Introduction

Neural synaptic weight refers to the influence strength of a connection between two neurons. The term is ususally used in neuroscience and artificial brain-inspired neural networks, as described in Iyer et al. (2013). In biological neuroscience, signal transmission is performed by interconnected networks of nerve cells or neurons, which resembles the transmission function in the computational case. The changes occurring in synaptic weight are well-known as synaptic plasticity, which is the ability of synapses to become stronger or weaker over time in response to fluctuations in their recent patterns of activity (Hughes, 1958). Hebbian theory is an original attempt to explain synaptic plasticity, which is the adaptation of brain neurons during the learning process (Hebb, 1949). One of several phenomena underlying synaptic plasticity is long-term potentiation (LTP), which is a long-lasting increase in synaptic weight, as explained in Bliss and Collingridge (1993) and Cooke and Bliss (2006). Long-term depression (LTD) is the opposing process to LTP, which was discussed in Massey and Bashir (2007). In artificial neural networks, the vector of inputs and that of outputs are interconnected with synaptic weights.

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* Project supported by the National Key Research and Development Program of China (No. 2018YFC0830300) and the National Natural Science Foundation of China (No. 61571312)

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Neurons that fire together wire together (Hebb, 1949). A number of efficient learning rules such as Hebb's rule (Hebb, 1949; Magee and Johnston, 1997), Oja's rule (Oja, 1982), radial basis functions (Powell, 1977), and the backpropagation algorithm (Battiti, 1992) can be used to change neural synaptic weights. As a number of theoretical and experimental problems became known, corresponding computational modified models have been suggested to learn the relationship between biological neurons. For instance, a supervised error-backpropagation algorithm was introduced for a network of spiking neurons that encoded information in the timing of individual spike times (Bohte et al., 2002). A number of stochastic computational elements used in artificial neural networks were examined in Brown and Card (2001a, 2001b). A content-addressable memory system was provided based on the aspects of neurobiology but readily adapted to integrated circuits in Hopfield (1982). In dual whole-cell voltage recordings from pyramidal neurons, the coincidence of postsynaptic action potentials and unitary excitatory postsynaptic potentials was explored in Markram et al. (1997). In addition, for dissociated rat hippocampal neurons, persistent potentiation and depression of glutamatergic synapses were induced by correlated spiking of presynaptic and postsynaptic neurons (Bi and Poo, 1998). Furthermore, a very-high-performance Viterbi decoder with a circularly connected two-dimensional analog cellular neural network cell array was disclosed in Kim et al. (2005). Weight limitation constraints were applied to the spike time error-backpropagation algorithm for temporally encoded networks of spiking neurons in Wu et al. (2006). Also, synapses in a spiking neural P system were endowed with integer weight denoting the number of synapses for each pair of connected neurons in Pan et al. (2012). However, due to the lack of a proper device to implement the synapses, research in this area has only had limited success practically.

To alleviate the explained problem, the great potential for exploiting the applications of the fourth missing circuit element, memristor (Chua, 1971, 1980a, 2003, 2011, 2012; Chua and Kang, 1976; Strukov et al., 2008; Borghetti et al., 2010), to neural networks has been investigated by many researchers (Snider, 2007; Jo et al., 2010; Adhikari et al., 2012, 2014, 2015; Kim et al., 2012; Sah et al., 2012; Li et al., 2013; Wang et al., 2015; Yang et al., 2018; Zhang CX et al., 2018). Memristor was originally envisioned (Chua, 1971) and then generalized to memristive systems (Chua and Kang, 1976), by circuit theorist Chua, as a missing nonlinear passive two-terminal electrical component (Chua, 1980a). This component has the non-volatility property as indicated in Chua (2003, 2011, 2012), Strukov et al. (2008), Borghetti et al. (2010), and Prodromakis et al. (2012). Symbol ⊓⊔⊓ denotes the memristor. The memristor is a new nonlinear circuit element that has the properties of memory and similar synapse. Zhang P et al. (2019) proposed a nanochannel-based interfacial memristor to emulate the analog weight modulation of synapses. Furthermore, Krishnaprasad et al. (2019) introduced an electronic synapse with basic synaptic behaviors, which was realized with MoS_2/graphene memristors. An artificial synapse with tunable synaptic behavior on the basis of a solution-processed memristor was explained in Zhou et al. (2019). Fu et al. (2020) proposed a type of diffusive memristor with the protein nanowires harvested from the bacterium to simulate nerve synapses with low power. Snider (2007) introduced a memristor-based self-organized network using dedicated connections for inhibitory weighting. Kim et al. (2012) proposed a memristor bridge circuit consisting of four identical memristors to perform zero, negative, and positive synaptic weightings. Adhikari et al. (2012) offered a novel analog hardware architecture of a memristor bridge synapse-based multilayer neural network and its learning scheme. Sah et al. (2012) proposed a simple and compact memristor-based bridge circuit that was able to carry out signed synaptic weighting in neuron cells. Li et al. (2013) presented a memcapacitor bridge circuit consisting of four identical memcapacitors. Adhikari et al. (2014) proposed a learning architecture for memristor-based multilayer neural networks. They also proposed a memristor-based circuit architecture for multilayer neural networks (Adhikari et al., 2015). Wang et al. (2015) introduced a spintronic memristor bridge synapse circuit. Yang et al. (2018) discussed the excitatory and inhibitory actions of a memristor bridge synapse. In the essence of mathematics, the aforementioned memristor bridge synapses were of integer-order memristive neural synaptic weightings.

At present, fractional calculus has become a key novel branch in mathematical analysis as

discussed in Oldham and Spanier (1974) and Podlubny (1998). However, the application of fractional calculus to neural networks, especially to spiking neural networks, is an emerging discipline of research. Fractional calculus has evolved to be a promising mathematical method for physical scientists and engineers. Some remarkable results and ideas have proved that fractional calculus can be a useful tool in many scientific fields such as diffusion processes (Özdemir and Karadeniz, 2008), viscoelasticity theory (Koeller, 1984), fractal dynamics (Rossikhin and Shitikova, 1997), fractional control (Podlubny et al., 2002), image processing (Pu et al., 2018b), fractor (Pu, 2016a, 2016b), fracmemristor (Fouda and Radwan, 2013, 2015; Yu and Wang, 2015; Yu et al., 2015; Pu and Yuan, 2016; Shi and Hu, 2017; Pu et al., 2018a), and neural networks (Pu, 2016c; Pu et al., 2017a, 2017b). The application of fractional calculus in neural networks is mainly due to its inherent advantages such as long-term memory, nonlocality, and weak singularity. Important properties of fractional calculus were discussed in Oldham and Spanier (1974) and Podlubny (1998). The basic feature of fractional calculus has extended the concepts of integer-order difference and Riemann sums. It is worth underlining that characteristics of fractional calculus are considerably different from those of classic integer-order calculus. For instance, fractional differential, except based on the Caputo definition, of a Heaviside function is nonzero, whereas its integer-order differential must be zero (Oldham and Spanier, 1974; Podlubny, 1998). From Chua's axiomatic circuit element system (Chua, 1971, 1980a, 2003, 2011, 2012; Chua and Kang, 1976) and according to constitutive relation, logical consistency, axiomatic completeness, and formal symmetry, it can be assumed that there should be a capacitive and an inductive fractional-order memristor corresponding to a capacitive and an inductive fractor, respectively (Pu, 2016a, 2016b). The concept of the memristor was generalized preliminarily from classic integer-order memristor to fractional-order memristor (Fouda and Radwan, 2013, 2015; Yu and Wang, 2015; Yu et al., 2015; Pu and Yuan, 2016; Shi and Hu, 2017; Pu et al., 2018a). There are two types of fractional-order memristor, i.e., the capacitive fractional-order memristor and the inductive fractional-order memristor (Pu and Yuan, 2016). The "fractional-order memristor" and the "fractional-order memristance" are abbreviated as "fracmemristor" and "fracmemristance," respectively (Pu and Yuan, 2016). Electrical properties of the capacitive fracmemristor fall in between those of the capacitor and those of the memristor, as explained in Pu and Yuan (2016) and Pu et al. (2018a). Similarly, electrical properties of the inductive fracmemristor fall in between those of the inductor and those of the memristor (Pu and Yuan, 2016; Pu et al., 2018a). Then, we combine the symbol of the capacitor and that of the memristor to denote the fracmemristor as symbol  . Furthermore, denote the positive incremental fracmemristor and negative one as  and  , respectively. In Pu and Yuan (2016) the generic fractional-order driving-point impedance functions of an arbitrary-order capacitive and inductive fracmemristor in their natural implementations were derived, respectively. Furthermore, Pu et al. (2018a) discussed the proposal for the first preliminary attempt of a feasible hardware achievement for an arbitrary-order fracmemristor and the recognition of the fingerprint of the fracmemristor. Therefore, based on the aforementioned studies on the fracmemristor (Fouda and Radwan, 2013, 2015; Yu and Wang, 2015; Yu et al., 2015; Pu and Yuan, 2016; Shi and Hu, 2017; Pu et al., 2018a), a challenging theoretical problem would be whether the fracmemristor can be applied to achieve the fractional-order memristive synapses or not. In this research, the fractional-order memristive neural synaptic weighting (FMNSW) is introduced to be achieved by a pulse-based fracmemristor bridge circuit.

2 Backgrounds

This section presents a brief introduction to the necessary theoretical background for fractional calculus, memristor, and fracmemristor.

First, the commonly used fractional calculus definitions in Euclidean measure are Grünwald-Letnikov, Riemann-Liouville, and Caputo (Oldham and Spanier, 1974; Podlubny, 1998). In this study, we adopt mainly the Grünwald-Letnikov defined fractional calculus as follows. The Grünwald-Letnikov definition of fractional calculus for causal signal $f(x)$ is given as

$$ {}^{\mathrm{G-L}}_{a}D^{v}_{x}f(x) = $$

$$\lim_{N\to\infty}\left\{\frac{(x-a)^{-v}}{\Gamma(-v)N^{-v}}\sum_{k=0}^{N-1}\frac{\Gamma(k-v)}{\Gamma(k+1)}f\left(x-k\frac{x-a}{N}\right)\right\}, \tag{1}$$

where $f(x)$ is a differintegrable function (Oldham and Spanier, 1974; Podlubny, 1998), $[a,x]$ is duration of $f(x)$, N is the number of partitions of the duration, v is an arbitrary real number, $\Gamma(\alpha)=\int_0^\infty \mathrm{e}^{-x}x^{\alpha-1}\mathrm{d}x$ is the Gamma function, and ${}^{\mathrm{G-L}}_{a}D^{v}_{x}$ denotes the Grünwald-Letnikov defined fractional differential operator. The Grünwald-Letnikov defined fractional calculus is readily calculated, which is related only to the discrete sampling value $f\left(x-k(x-a)/N\right)$ of $f(x)$ and not to the derivative or integral value of $f(x)$. If $f(x)$ is a causal signal and its fractional primitives are zero, the Fourier transform of the v-order fractional differential operator (Oldham and Spanier, 1974; Podlubny, 1998) is described as $\mathrm{F}\left[{}^{\mathrm{G-L}}_{0}D^{v}_{x}f(x)\right]=(\mathrm{j}\omega)^{v}\mathrm{F}\left[f(x)\right]$, where $\mathrm{F}(\cdot)$ denotes the Fourier transform, j presents the imaginary unit, and ω denotes an angular frequency. In this study, equivalent notations $D^{v}_{x}={}^{\mathrm{G-L}}_{0}D^{v}_{x}$ are used in an interchangeable manner.

Second, the memristor, M, completes the set of relations with (Chua, 1971)

$$\phi\left[q(t)\right]=M\left[q(t)\right]q(t), \tag{2}$$

where ϕ, q, and t denote the magnetic flux, quantity of electric charge, and time variable, respectively. The slope of this function is called the memristance, $r(q)$, which is similar to variable resistance (Chua, 1971), expressed as

$$\begin{aligned}v_{\mathrm{in}}(t)&=\frac{\mathrm{d}\phi(q)}{\mathrm{d}q}i_{\mathrm{in}}(t)\\&=\left[M(q)+q\frac{\mathrm{d}M(q)}{\mathrm{d}q}\right]i_{\mathrm{in}}(t)\\&=r(q)i_{\mathrm{in}}(t)=h(q)*i_{\mathrm{in}}(t),\end{aligned} \tag{3}$$

where $v_{\mathrm{in}}(t)$ and $i_{\mathrm{in}}(t)$ denote instantaneous values of the input voltage and input current of a memristor, respectively. The symbol "$*$" denotes convolution, $r(q)=[M(q)+q\mathrm{d}M(q)/\mathrm{d}q]$ and $h(q)$ denote memristance and transmission function of a memristor, respectively, where $q(t)=I_t^{-1}i_{\mathrm{in}}(t)=\int_0^t i_{\mathrm{in}}(t)\mathrm{d}t$. Then, we will have $r(q)=(h(q)*i_{\mathrm{in}}(t))/i_{\mathrm{in}}(t)$. Furthermore, the small-signal behavior method is an efficient approach for studying a resistive nonlinear network, as discussed in Chua (1978a, 1978b, 1980b). Eq. (3) indicates that in the case of small-signal behavior, the Laplace transform of $v_{\mathrm{in}}(t)=r(q)i_{\mathrm{in}}(t)$ is $V_{\mathrm{in}}(s)=\dfrac{1}{2\pi}\cdot\mathrm{L}\{r\left[q(t)\right]\}*I_{\mathrm{in}}(s)$, where $\mathrm{L}\{\ \}$ represents the Laplace transform and s denotes a complex variable of the Laplace transform. Thus, in Eq. (3), the Laplace transform of $v_{\mathrm{in}}(t)=h(q)*i_{\mathrm{in}}(t)$, $V_{\mathrm{in}}(s)=H(s)I_{\mathrm{in}}(s)$, achieves a multiplication in the Laplace transform domain, where $H(s)=\mathrm{L}\{h\left[q(t)\right]\}$ is reactance of the memristor (Pu et al., 2018a). For an arbitrary-order capacitive or inductive fracmemristor in their natural implementations, the generic fractional-order driving-point impedance function was derived (Pu and Yuan, 2016; Pu et al., 2018a), given as

$$\begin{aligned}\mathrm{FM}^{c}_{-v}&=\mathrm{FM}^{c}_{-(\eta+p)}\\&=\frac{V_{\mathrm{in}}(s)}{I_{\mathrm{in}}(s)}=c^{-v}\left[H(s)\right]^{1-p}s^{-v},\end{aligned} \tag{4}$$

$$\begin{aligned}\mathrm{FM}^{l}_{v}&=\mathrm{FM}^{l}_{\eta+p}\\&=\frac{V_{\mathrm{in}}(s)}{I_{\mathrm{in}}(s)}=l^{v}\left[H(s)\right]^{1-p}s^{v},\end{aligned} \tag{5}$$

where FM^{c}_{-v} and FM^{l}_{v} represent the fractional-order driving-point impedance function of a purely ideal v-order capacitive fracmemristor and that of an inductive fracmemristor, respectively, and c and l are capacitance and inductance, respectively. $r^{c}_{-v}(q)=c^{v}\mathrm{L}^{-1}\{[H(s)]^{1-p}\}$ and $r^{l}_{v}(q)=l^{v}\mathrm{L}^{-1}\{[H(s)]^{1-p}\}$ are respectively capacitive fracmemristance and inductive fracmemristance, where $\mathrm{L}^{-1}\{\ \}$ is the inverse Laplace transform. $v=\eta+p$ is a non-negative real number, η is a non-negative integer, and $0\le p\le 1$. Note that, if $v=0$, then $\eta=0$ and $p=0$. Eqs. (4) and (5) identically degenerate to the driving-point impedance function of the resistor. Furthermore, if v is a positive integer, then $\eta=v-1$ and $p=1$. Eqs. (4) and (5) degenerate to the driving-point impedance function of the capacitor and that of the inductor, respectively. In addition, if $0<v<1$, then $\eta=0$ and $0<p<1$. Eqs. (4) and (5) represent the v-order ($0<v<1$) driving-point impedance function of the capacitive fracmemristor and that of the inductive fracmemristor, respectively. In addition, if $v>1$ is a positive fraction, then $\eta=[v]$ and $0<p<1$, where $[\,]$ is the rounding operation. Eqs. (4) and (5) represent the corresponding v-order ($v>1$) driving-point impedance function of the capacitive fracmemristor and that of the inductive fracmemristor, respectively.

3 Fractional-order memristive neural synaptic weighting

In this section, the FMNSW achieved by a pulse-based fracmemristor bridge circuit is implemented.

To implement the FMNSW and to start with, the corresponding pulse-based fracmemristor bridge circuit should be achieved. The pulse-based fracmemristor bridge circuit can be obtained by two v-order oppositely incremental capacitive fracmemristors (FM_1^1 and FM_2^1) with the same circuit parameters (Fig. 1).

In Fig. 1, the input voltage $v_{\mathrm{in}}^1(t)$ is a positive or negative pulse signal that inputs at the input port of a pulse-based fracmemristor bridge circuit. Two integrated operational amplifiers A_1^1 and A_2^1 construct two identical voltage-to-current converters in phase input mode. FM_1^1 is a negative incremental fracmemristor, while FM_2^1 is a positive one. Hence, whether the polarity of $v_{\mathrm{in}}^1(t)$ is positive or negative is not important, and the fracmemristance variation tendency of FM_2^1 is in the opposite direction of FM_1^1. Therefore, according to Kirchhoff's current law (KCL) and Kirchhoff's voltage law (KVL), from Fig. 1 the following relationships are derived:

$$i_{\mathrm{in}}^1(t) = i_{\mathrm{in}}^2(t) = \frac{v_{\mathrm{in}}^1(t)}{r_{\mathrm{s}}}, \tag{6}$$

$$I_{\mathrm{in}}^1(s) = \mathrm{L}\{i_{\mathrm{in}}^1(t)\} = I_{\mathrm{in}}^2(s) = \mathrm{L}\{i_{\mathrm{in}}^2(t)\}, \tag{7}$$

$$v_{\mathrm{FM}_1^1}(t) = v_0 - \mathrm{L}^{-1}\{c^{-v}\left[H(s)\right]^{1-p} s^{-v} I_{\mathrm{in}}^1(s)\}, \tag{8}$$

$$v_{\mathrm{FM}_2^1}(t) = v_0 + \mathrm{L}^{-1}\{c^{-v}\left[H(s)\right]^{1-p} s^{-v} I_{\mathrm{in}}^1(s)\}, \tag{9}$$

$$v_A^1(t) = v_{\mathrm{FM}_1^1}(t) + v_{\mathrm{in}}^1(t), \tag{10}$$

$$v_B^1(t) = v_{\mathrm{FM}_2^1}(t) + v_{\mathrm{in}}^1(t), \tag{11}$$

where v_0 is an initial voltage drop across FM_1^1 or FM_2^1. Thus, from Eqs. (6)–(11), the output voltage $v_{\mathrm{out}}^1(t)$ of a pulse-based fracmemristor bridge circuit is equal to the potential difference between point B and point A, given as

$$\begin{aligned} v_{\mathrm{out}}^1(t) &= v_B^1(t) - v_A^1(t) \\ &= 2\mathrm{L}^{-1}\{c^{-v}\left[H(s)\right]^{1-p} s^{-v} I_{\mathrm{in}}^1(s)\}. \end{aligned} \tag{12}$$

Eq. (12) implies that since $H(s) = \mathrm{L}\{h\left[q(t)\right]\}$ is reactance of the memristor constituting an incremental capacitive fracmemristor, the synaptic weight of a pulse-based fracmemristor bridge circuit is a nonlinear function with long-term memory. In artificial neural networks, the synaptic weight of a pulse-based fracmemristor bridge circuit obtains fractional-order memristive nonvolatile weight storage. The fracmemristor bridge synapse is composed of two incremental capacitive fracmemristors with opposite operations. By applying a programmed pulse signal $v_{\mathrm{in}}^1(t)$, the output voltage $v_{\mathrm{out}}^1(t)$ of a pulse-based fracmemristor bridge circuit can be set to a desired value, which can be expressed as

$$v_{\mathrm{out}}^1(t) \begin{cases} > 0, \ \mathrm{L}^{-1}\{c^{-v}\left[H(s)\right]^{1-p} s^{-v} I_{\mathrm{in}}^1(s)\} > 0, \\ = 0, \ \mathrm{L}^{-1}\{c^{-v}\left[H(s)\right]^{1-p} s^{-v} I_{\mathrm{in}}^1(s)\} = 0, \\ < 0, \ \mathrm{L}^{-1}\{c^{-v}\left[H(s)\right]^{1-p} s^{-v} I_{\mathrm{in}}^1(s)\} < 0. \end{cases} \tag{13}$$

In the first step, to provide a transparent discussion, in Fig. 1, the pulse-based fracmemristor bridge circuit is implemented using two v-order oppositely incremental capacitive fracmemristors with identical circuit parameters. However, in an actual circuit, the circuit parameters (r_{p} and r_{s}) of these two v-order incremental capacitive fracmemristors can be different. Hence, in this case, $i_{\mathrm{in}}^1(t) = v_{\mathrm{in}}^1(t)/r_{\mathrm{s}_1}$ and $i_{\mathrm{in}}^2(t) = v_{\mathrm{in}}^1(t)/r_{\mathrm{s}_2}$ are derived, where r_{s_1} and r_{s_2} are the bias resistances of FM_1^1 and FM_2^1, respectively. Then, we have $v_{\mathrm{FM}_1^1}(t) = v_0 - \mathrm{L}^{-1}\{c^{-v}\left[H(s)\right]^{1-p} s^{-v} I_{\mathrm{in}}^1(s)\}$ and $v_{\mathrm{FM}_2^1}(t) = v_0 + \mathrm{L}^{-1}\{c^{-v}\left[H(s)\right]^{1-p} s^{-v} I_{\mathrm{in}}^2(s)\}$. In a similar way for deriving Eq. (12), we obtain $v_{\mathrm{out}}^1(t) = \mathrm{L}^{-1}\{c^{-v}\left[H(s)\right]^{1-p} s^{-v} I_{\mathrm{in}}^2(s)\} + \mathrm{L}^{-1}\{c^{-v}\left[H(s)\right]^{1-p} s^{-v} I_{\mathrm{in}}^1(s)\}$.

In the second step, weighted signals of a biological synapse are summed in each unit. In a similar way for biological synapses, by applying a pulse-based fracmemristor bridge circuit, the fracmemristor bridge synaptic circuit can be achieved (Fig. 2).

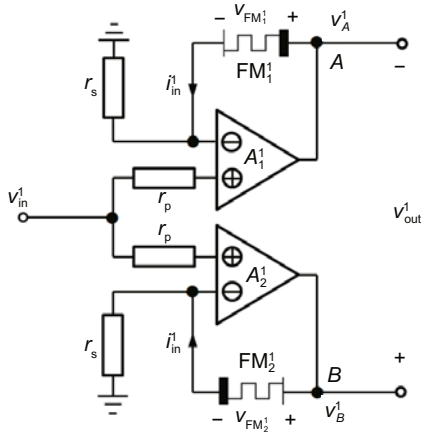

Fig. 1 Pulse-based fracmemristor bridge circuit

In Fig. 2, A_1^1, A_2^1, A_3^1, and A_4^1 are four integrated operational amplifiers, of which A_3^1 constructs a subtractor and A_4^1 gives a voltage-to-current converter in reversed-phase input mode. r_{L} is a load resistor, and i_{L}^1 is load current that flows through r_{L}. Thus, from Fig. 2, under individual effect of v_A^1 and v_B^1, we obtain

$$v_3^1(t)=\frac{r_{\mathrm{f}}}{r_{\mathrm{t}}}\left[v_B^1(t)-v_A^1(t)\right]. \tag{14}$$

As for A_4^1, from Eqs. (12) and (14), it can be written as

$$\begin{aligned} i_{\mathrm{L}}^1(t)&=i_1^1(t)=\frac{v_3^1(t)}{r_1^1}\\ &=\frac{1}{r_1^1}\frac{r_{\mathrm{f}}}{r_{\mathrm{t}}}\left[v_B^1(t)-v_A^1(t)\right]=\frac{r_{\mathrm{f}}}{r_1^1 r_{\mathrm{t}}}v_{\mathrm{out}}^1(t). \end{aligned} \tag{15}$$

From Eq. (15), load current $i_{\mathrm{L}}^1(t)$ depends merely on $v_B^1(t)-v_A^1(t)$, and has nothing to do with the load resistor r_{L}. Therefore, the fracmemristor bridge synaptic circuit implements a differential current source in practice.

In the third step, a biological neuron consists of multiple synapses and one activation unit. Similar to biological neurons, by applying the fracmemristor bridge synaptic circuit, the fracmemristor bridge neuron circuit can be implemented (Fig. 3).

In Fig. 3, FM_1^1, FM_2^1, A_1^1, A_2^1, A_3^1, and A_4^1 construct the first fracmemristor bridge synaptic circuit. FM_1^n, FM_2^n, A_1^n, A_2^n, A_3^n, and A_4^n construct the n^{th} fracmemristor bridge synaptic circuit, and the integrated operational amplifier A^{n+1} achieves a cell bias circuit. $v_{\mathrm{b}}(t)$ is a cell bias voltage (voltage source biasing pulse), and $i_{\mathrm{L}}(t)$ is the load current that flows through r_{L}. Thus, from Fig. 3 and Eq. (15), according to KCL, it can be written as

$$\begin{aligned} i_{\mathrm{L}}^i(t)&=i_1^i(t)=\frac{v_3^i(t)}{r_1^i}\\ &=\frac{1}{r_1^i}\frac{r_{\mathrm{f}}}{r_{\mathrm{t}}}\left[v_B^i(t)-v_A^i(t)\right]=\frac{r_{\mathrm{f}}}{r_1^i r_{\mathrm{t}}}v_{\mathrm{out}}^i(t), \end{aligned} \tag{16}$$

$$\begin{aligned} i_{\mathrm{L}}^n(t)&=i_1^n(t)=\frac{v_3^n(t)}{r_1^n}\\ &=\frac{1}{r_1^n}\frac{r_{\mathrm{f}}}{r_{\mathrm{t}}}\left[v_B^n(t)-v_A^n(t)\right]=\frac{r_{\mathrm{f}}}{r_1^n r_{\mathrm{t}}}v_{\mathrm{out}}^n(t), \end{aligned} \tag{17}$$

$$i_{\mathrm{L}}^{n+1}=i_1^{n+1}=\frac{v_{\mathrm{b}}(t)}{r_1^{n+1}}, \tag{18}$$

where $i\in[1,n]$ is a positive integer. From Fig. 3 and Eqs. (15)–(18), it can be observed that the output currents, weighted separately by each fracmemristor bridge synapse, are gathered to flow through the load resistor r_{L}. Therefore, it follows as

$$i_{\mathrm{L}}(t)=\sum_{i=1}^{n}i_{\mathrm{L}}^i(t)+i_{\mathrm{L}}^{n+1}(t), \tag{19}$$

$$v_{\mathrm{out}}(t)=r_{\mathrm{L}}i_{\mathrm{L}}(t)=r_{\mathrm{L}}\left(\sum_{i=1}^{n}i_{\mathrm{L}}^i(t)+i_{\mathrm{L}}^{n+1}(t)\right). \tag{20}$$

In the fourth step, a common architecture of biological neural networks is simply the repeated connections of each neuron. Similar to biological neural

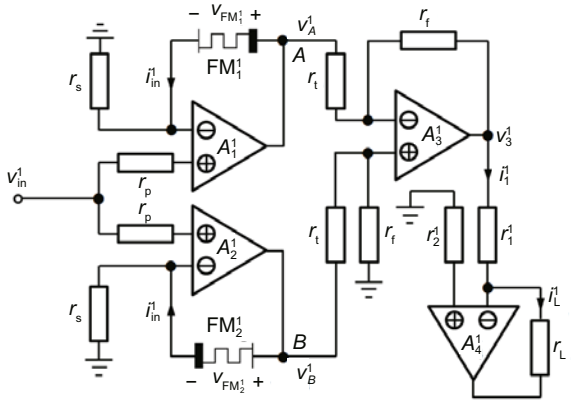

Fig. 2 Fracmemristor bridge synaptic circuit

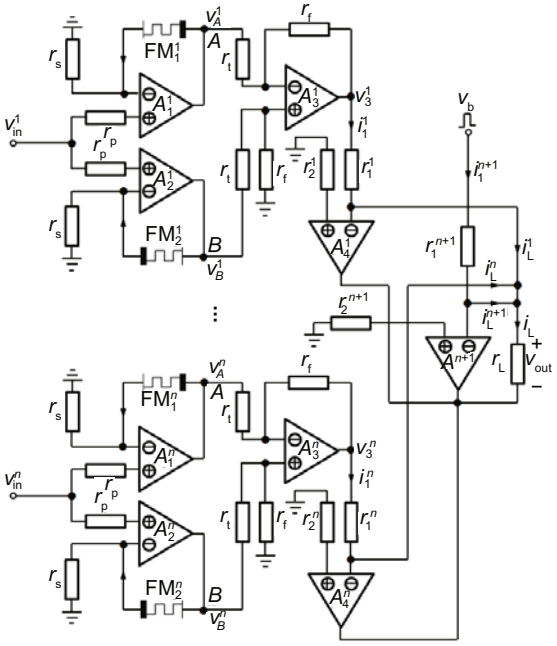

Fig. 3 Fracmemristor bridge neuron circuit

networks, by applying the fracmemristor bridge neuron circuit, the architecture of the fractional-order memristive neural networks circuit can be achieved (Fig. 4).

Fig. 4 illustrates that for the fractional-order memristive neural networks circuit, the output of each neuron is connected to another fracmemristor bridge neuron circuit. It is worth underlining that in a fractional-order memristive neural network, all fracmemristor bridge synaptic circuits operate only during the pulse width period of $v_{\mathrm{b}}(t)$.

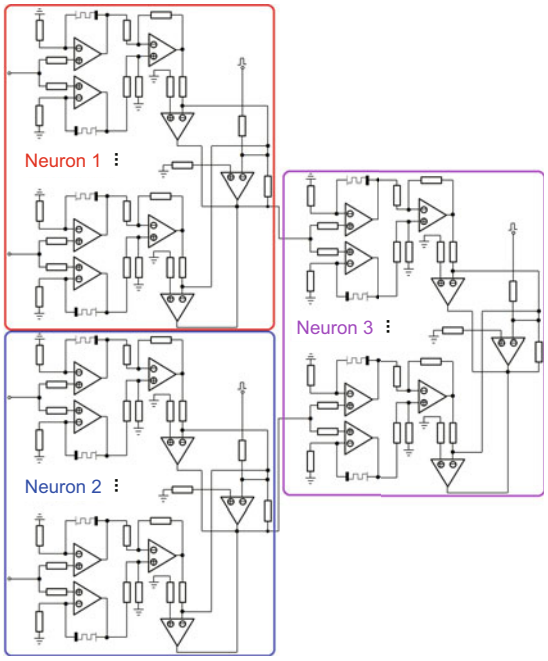

Fig. 4 Architecture of fractional-order memristive neural networks circuit

4 Experimental tasks and analyses

In this section, electrical characteristics of the pulse-based fracmemristor and memristor bridge circuit are compared. Then, different synaptic behaviors such as short- and long-term memory, LTP and LTD, and non-associative learning are better explained using the pulse-based fracmemristor bridge circuit.

4.1 Electrical characteristics of pulse-based fracmemristor bridge circuit

Electrical characteristics of a pulse-based fracmemristor bridge circuit are compared and analyzed below.

In Fig. 1, a current-controlled capacitive fracmemristor is taken as an example to analyze the electrical characteristics of a pulse-based fracmemristor bridge circuit. It is assumed that the input causal current across the memristor constituting an incremental capacitive fracmemristor, which is the same as the current across this incremental capacitive fracmemristor, is given over one period as follows:

$$i_{\mathrm{in}}^{1}(t)=\frac{v_{\mathrm{in}}^{1}(t)}{r_{\mathrm{s}}}=\begin{cases}A_0, & 0<t\le T_1,\\ 0, & T_1<t<T,\end{cases} \tag{21}$$

where A_0 is the amplitude of the pulse signal. This input current is periodic with fundamental period T, fundamental frequency $f_0=1/T$, and fundamental angular frequency $w_0=2\pi/T$. Therefore, in the case of small-signal behavior, from Eq. (21), the corresponding Fourier transform will be

$$\begin{aligned}I_{\mathrm{in}}^{1}(\mathrm{j}w)&=\mathrm{F}\{i_{\mathrm{in}}^{1}(t)\}\\&=\sum_{k=-\infty}^{+\infty}\frac{2A_0}{k}\sin\left(\frac{kw_0T_1}{2}\right)\mathrm{e}^{\frac{-\mathrm{j}wT_1}{2}}\delta(w-kw_0),\end{aligned} \tag{22}$$

where $\delta(\cdot)$ is the impulse function.

The quantity of electric charge across an incremental capacitive fracmemristor is equal to the one-order integral of the input current:

$$q(t)=I_t^{-1}i_{\mathrm{in}}^{1}(t). \tag{23}$$

Furthermore, from Eq. (21), the v-order fractional integral of $i_{\mathrm{in}}^{1}(t)$ can be derived as follows:

$$\begin{aligned}D_t^{-v}i_{\mathrm{in}}^{1}(t)&=\frac{A_0t^v}{\Gamma(1+v)}\\&+\sum_{k=1}^{N}\frac{A_0(-1)^k(t-kT/2)^v}{\Gamma(1+v)}u\left(t-\frac{kT}{2}\right),\end{aligned} \tag{24}$$

where $u(t)$ is the Heaviside function. In addition, it is assumed that the memristance of the positive incremental memristor used in a positive incremental capacitive fracmemristor is given as

$$r[q(t)]=K_1+K_2q(t), \tag{25}$$

where K_1 and K_2 are constants. Thus, from Eqs. (3) and (25), the instantaneous input voltage of this memristor can be derived as

$$v_{\mathrm{in}}(t)=r(q)i_{\mathrm{in}}^{1}(t)=h(q)*i_{\mathrm{in}}^{1}(t), \tag{26}$$

where v_{in} is input causal voltage across the memristor, and $r(q) = (h(q) * i^1_{\text{in}}(t))/i^1_{\text{in}}(t)$. It is assumed that the initial value of electric charge of this memristor is equal to zero. Then, the Fourier transform of Eq. (26) can be derived as follows:

$$V_{\text{in}}(\text{j}w) = H(\text{j}w)I^1_{\text{in}}(\text{j}w) \Leftrightarrow H(\text{j}w) = \frac{V_{\text{in}}(\text{j}w)}{I^1_{\text{in}}(\text{j}w)}, \quad (27)$$

where reactance of this memristor is equal to $H(\text{j}w) = \text{F}\{h(q)\}$. Substituting Eq. (27) into Eq. (4) with $s = \text{j}w$, the voltage-current relationship equation of a v-order incremental capacitive fracmemristor can be expressed as

$$V_{\text{FM}^1_i}(t) = c^{-v}\text{F}^{-1}\{[H(\text{j}w)]^{1-p}\} * [D_t^{-v} i^1_{\text{in}}(t)], \quad (28)$$

where F^{-1} is the inverse Fourier transform.

There is a possibility to make the input current be equal to Eq. (21) by choosing an appropriate voltage source and resistance. We set the fundamental frequency $f_0 = 5$ Hz, $A_0 = 10^{-5}$ A, $r_{\text{s}} = 1000\ \Omega$, $K_1 = 2000$, and $K_2 = 5 \times 10^7$. The voltage of a half-order positive incremental capacitive fracmemristor is presented in Fig. 5.

When $v = 0$, then $p = 0$, and the positive incremental capacitive fracmemristor becomes a special case, which is a positive incremental memristor. The voltage of a positive incremental memristor is presented in Fig. 6.

It is assumed that the memristance of the negative incremental memristor used in a negative incremental capacitive fracmemristor is as follows:

$$r\,[q(t)] = K_1 - K_2 q(t). \quad (29)$$

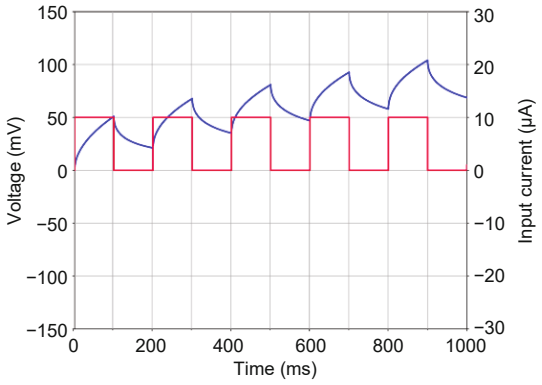

Fig. 5 Voltage of a positive incremental capacitive fracmemristor of half-order. Red corresponds to the right vertical axis and blue corresponds to the left vertical axis. References to color refer to the online version of this figure

The voltages of a negative incremental capacitive fracmemristor of half-order and the negative incremental memristor can be gained in a similar way, as shown in Figs. 7 and 8, respectively.

Therefore, the output voltage of a pulse-based fracmemristor bridge circuit can be obtained, which is demonstrated in Fig. 9.

Similarly, the output voltage of a pulse-based memristor bridge circuit can be obtained as shown in Fig. 10.

The pulse-based memristor bridge circuit realizes linear weighting on the input signal, whereas the pulse-based fracmemristor bridge circuit yields nonlinear weighting operation, which is more appropriate for explaining the neural synaptic weighting. In addition, circuit parameters can be adjusted to

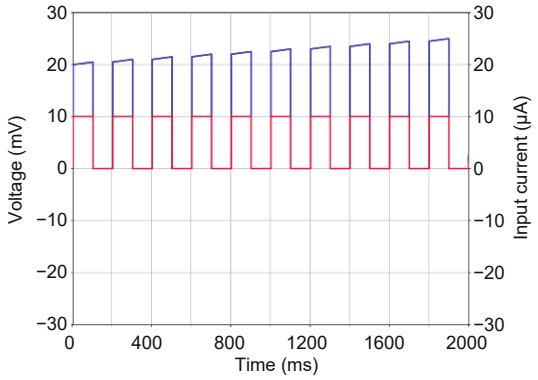

Fig. 6 Voltage of a positive incremental memristor of half-order. Red corresponds to the right vertical axis and blue corresponds to the left vertical axis. References to color refer to the online version of this figure

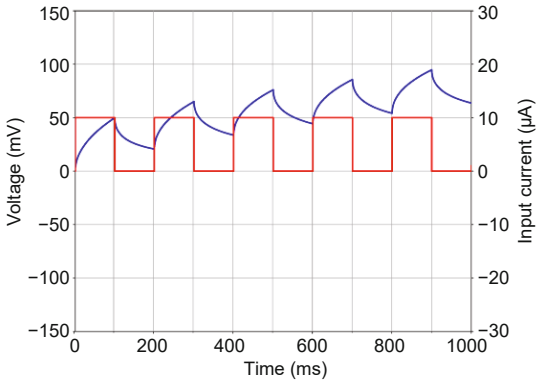

Fig. 7 Voltage of a negative incremental capacitive fracmemristor of half-order. Red corresponds to the right vertical axis and blue corresponds to the left vertical axis. References to color refer to the online version of this figure

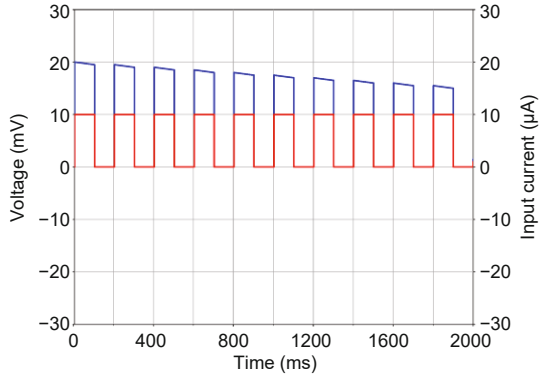

Fig. 8 Voltage of a negative incremental memristor of half-order. Red corresponds to the right vertical axis and blue corresponds to the left vertical axis. References to color refer to the online version of this figure

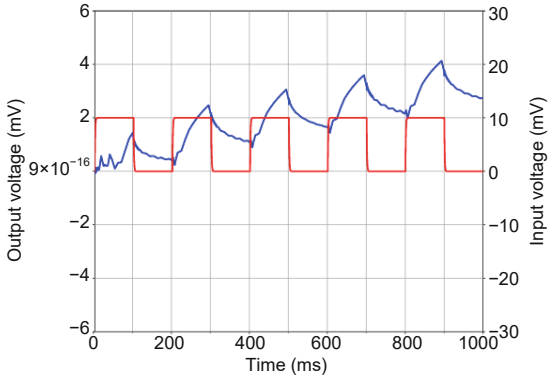

Fig. 9 Output voltage of a pulse-based fracmemristor bridge circuit with $v_{\mathrm{in}}^1(t) = 10$ mV, $r_{\mathrm{p}} = 1000\ \Omega$, and $r_{\mathrm{s}} = 1000\ \Omega$. Red corresponds to the right vertical axis and blue corresponds to the left vertical axis. References to color refer to the online version of this figure

change the outputs. For instance, when the resistance r_{s} is reduced to 100 Ω, the current flowing through the fracmemristor increases, and the overall output voltage of this pulse-based fracmemristor bridge circuit increases, as demonstrated in Fig. 11.

The output current of a fracmemristor bridge synaptic circuit is equal to $i_{\mathrm{L}}^1(t) = r_{\mathrm{f}} v_{\mathrm{out}}^1(t)/(r_1^1 r_{\mathrm{t}})$, and the output current wave is similar to the output voltage of the corresponding pulse-based fracmemristor bridge circuit.

4.2 Simulation of different synaptic behaviors

4.2.1 Short- and long-term memories

Different synaptic behaviors can be simulated by changing amplitude A, width W, and time

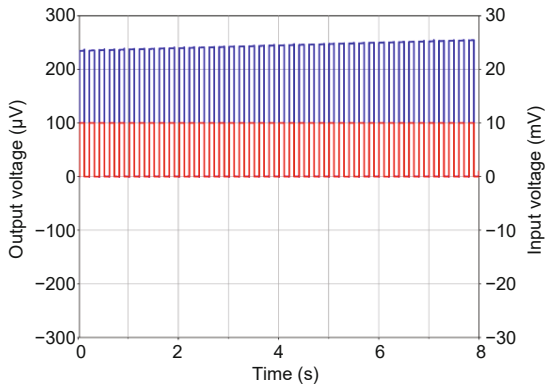

Fig. 10 Output voltage of a pulse-based memristor bridge circuit with $v_{\mathrm{in}}^1(t) = 10$ mV, $r_{\mathrm{p}} = 1000\ \Omega$, and $r_{\mathrm{s}} = 1000\ \Omega$. Red corresponds to the right vertical axis and blue corresponds to the left vertical axis. References to color refer to the online version of this figure

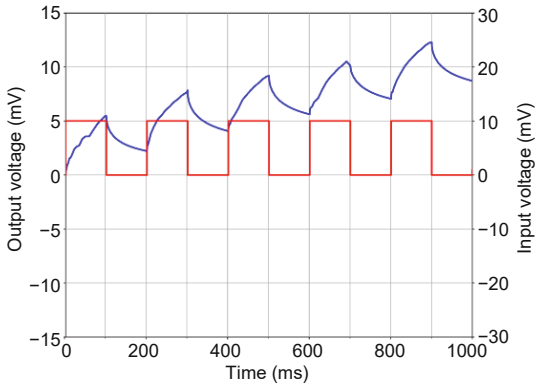

Fig. 11 Output voltage of a pulse-based fracmemristor bridge circuit with $v_{\mathrm{in}}^1(t) = 10$ mV, $r_{\mathrm{p}} = 1000\ \Omega$, and $r_{\mathrm{s}} = 100\ \Omega$. Red corresponds to the right vertical axis and blue corresponds to the left vertical axis. References to color refer to the online version of this figure

interval T of the input pulse (Fig. 12).

Figs. 12a–12c show examples of A=10 mV, W=2 ms, where time interval T is 198, 98, and 48 ms, respectively. After the first pulse input, the synaptic weight reaches a certain value rapidly. However, before the next pulse is input, the synaptic weight will spontaneously decay to a lower state exponentially. This phenomenon can be explained as the short-term plasticity behavior of synapses, similar to the short-term memory process of biological brains. For ordinary people, if something is learnt once only, that will be forgotten soon, but a little impression will be kept. With continuous input of pulses, the synaptic weight keeps increasing continually. Through continuous learning, we are more impressed with that

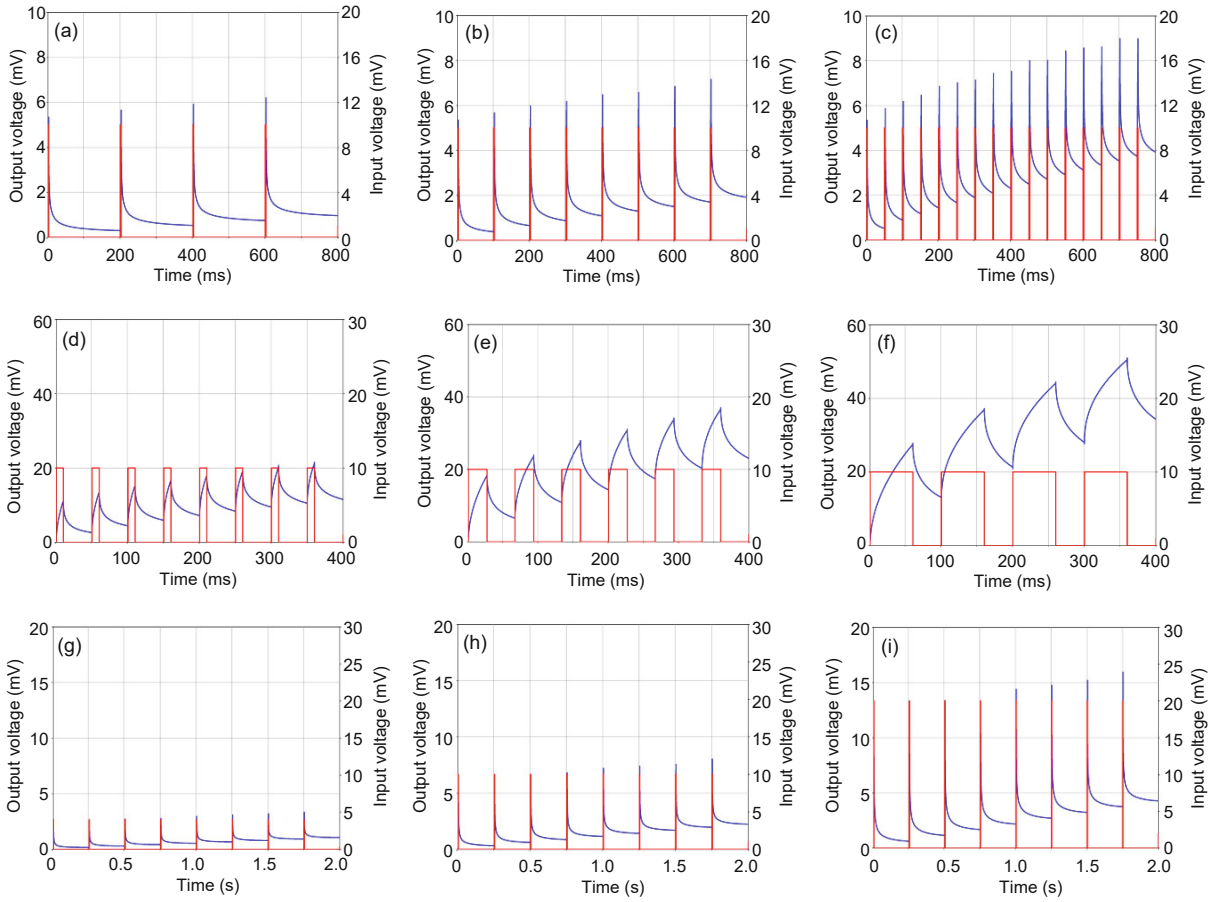

Fig. 12 Different synaptic behaviors with different amplitudes A, widths W, and time intervals T of the input voltage: (a) A =10 mV, W =2 ms, T =198 ms; (b) A =10 mV, W =2 ms, T =98 ms; (c) A =10 mV, W =2 ms, T =48 ms; (d) A =10 mV, W =10 ms, T =40 ms; (e) A =10 mV, W =36.67 ms, T =40 ms; (f) A =10 mV, W =60 ms, T =40 ms; (g) A =4 mV, W =2.5 ms, T =247.5 ms; (h) A =10 mV, W =2.5 ms, T =247.5 ms; (i) A =20 mV, W =2.5 ms, T =247.5 ms. Red corresponds to the right vertical axis and blue corresponds to the left vertical axis. References to color refer to the online version of this figure

knowledge point. By decreasing the input pulse interval, decay time of synaptic weight decreases. The higher the frequency of stimulation, the more the synaptic weight increases. After the last pulse inputs, the synaptic weight is almost constant after a certain period of decay. In the same period, if a knowledge point is reviewed multiple times, one will be more impressed with that knowledge point. Multiple reviews in the same period can lead to a transition from short-term memory to long-term memory.

Figs. 12d–12f show examples of A=10 mV, T=40 ms, for various widths as 10, 36.67, and 60 ms. Since the decay time is the same, the synaptic weight increases as the input pulse width increases. By increasing the input pulse width, the learning time becomes longer. In the same period, increasing the learning time can lead to a transition from short-term memory to long-term memory.

Figs. 12g–12i show examples of W=2.5 ms, T=247.5 ms, for various amplitudes as 4, 10, and 20 mV. With the increase of input pulse amplitude, the synaptic weight increases. With the same duration and frequency, the synaptic weight increases with the increase of amplitude. Increasing the amplitude of the input pulse resembles the enhancement of learning intensity. In the same period, enhancing the learning intensity can also lead to a transition from short-term memory to long-term memory.

4.2.2 LTP and LTD

In neuroscience, LTP of synaptic transmission was discovered by Bliss and Lømo (1973) in the

dentate area of a rabbit. LTP describes the long-lasting increase of the synaptic weight. LTD, as the opposite of LTP, produces a long-lasting decrease in the synaptic weight. As learning and memory are encoded by modification of the synaptic weight, LTP and LTD are widely considered as two major cellular mechanisms that underlie learning and memory.

At present, many LTP studies conduct an investigation to develop methods to enhance LTP to improve learning and memory. In addition, LTP is a subject of clinical research, for example, in the areas of Alzheimer's disease and addiction medicine. The results of this study prove that we can achieve the purpose of LTP or LTD by means of the pulse-based fracmemristor bridge circuit, as shown in Figs. 13 and 14.

Applying a positive voltage pulse strengthens the output voltage of a pulse-based fracmemristor bridge circuit gradually, which leads to the LTP of the synapse weight. On the other hand, a negative voltage pulse input weakens the output voltage of the pulse-based fracmemristor bridge circuit gradually, which leads to the LTD of the synapse weight. When the duty cycle of the input voltage pulse is equal to 50%, the output voltage almost returns to its starting value after a period (Fig. 13). When the duty cycle of the input voltage pulse is equal to 70%, the overall output voltage increases (Fig. 14).

4.2.3 Habituation and sensitization

The pulse-based fracmemristor bridge synaptic circuit can unfold the non-associative learning processes well. One of the non-associative learning processes is habituation. When a harmless stimulus is repeatedly applied to a person or an animal, the degree of response is progressively weakened, as depicted in Fig. 15.

Humans and animals can learn not to respond to many meaningless stimuli with the help of habituation. We may habituate to an environment with repeated noises when we learn that these have no consequences (Fennell, 2012). The Nobel laureate Eric R. Kandel had observed that repeated stimuli of the siphon of a sea slug Aplysia led to progressively less contraction of the gill-withdrawal muscles and that the response was steadily weakening (Kandel, 2007; Chua, 2013).

Another non-associative learning process is sensitization (Shettleworth, 2009). Sensitization often is featured by an enhancement of response to a weak stimulus after an intense harmful stimulus, as presented in Fig. 16. For example, humans usually feel nothing when touching the finger. However, after our finger is hit with a hammer or pinched with a plier, the response of touching the finger is amplified because we feel the pain and become more sensitive to touching the finger.

Sensitization helps humans and animals learn to avoid noxious stimuli. After weakening the response by repeatedly touching the siphon of a sea slug Aplysia, Eric R. Kandel and his colleagues employed noxious electrical stimuli to stimulate the siphon, which led the gill-withdrawal response to reappear.

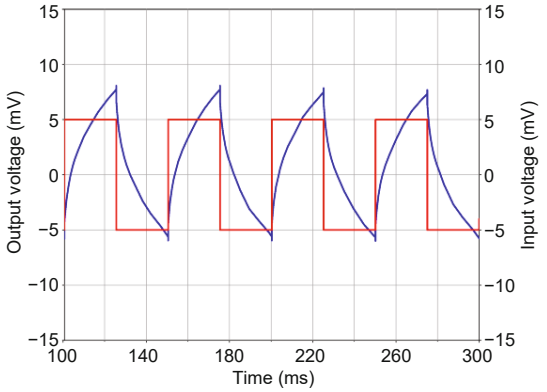

Fig. 13 Output voltage of a pulse-based fracmemristor bridge circuit with the duty cycle of the input voltage pulse equal to 50%. Red corresponds to the right vertical axis and blue corresponds to the left vertical axis. References to color refer to the online version of this figure

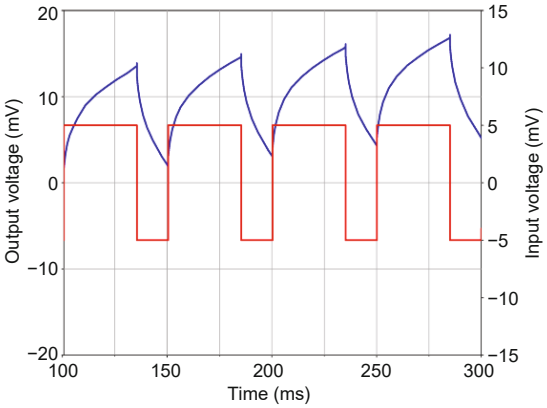

Fig. 14 Output voltage of a pulse-based fracmemristor bridge circuit with the duty cycle of the input voltage pulse equal to 70%. Red corresponds to the right vertical axis and blue corresponds to the left vertical axis. References to color refer to the online version of this figure

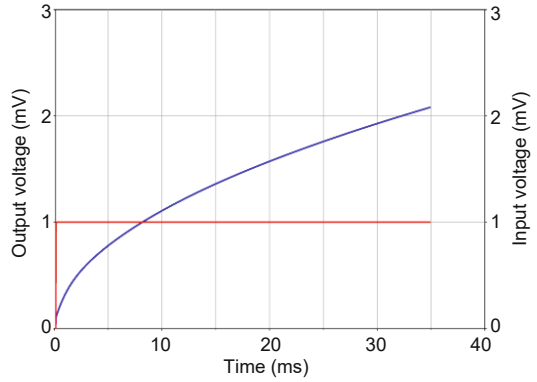

Fig. 15 Habituation explained by the pulse-based fracmemristor bridge circuit. Red corresponds to the right vertical axis and blue corresponds to the left vertical axis. References to color refer to the online version of this figure

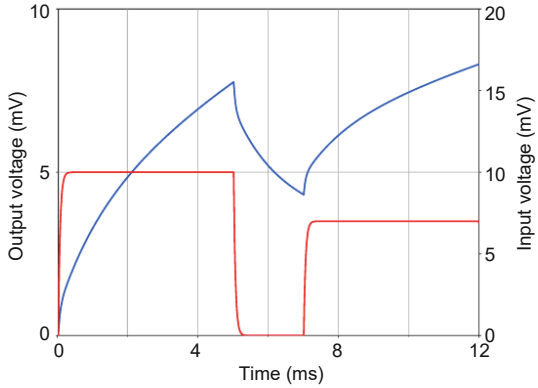

Fig. 16 Sensitization explained by the pulse-based fracmemristor bridge circuit. Red corresponds to the right vertical axis and blue corresponds to the left vertical axis. References to color refer to the online version of this figure

After this sensitization, a light touch to the siphon produced a strong gill-withdrawal response and this type of phenomenon lasted several days (Squire and Kandel, 2003).

4.2.4 Neural signals

For a pulse-based fracmemristor bridge circuit, the fundamental frequency of the input voltage can be altered to produce what is needed. For instance, when the fundamental frequency is $f_0 = 40$ Hz, in the positive voltage pulse interval, the output voltage of the pulse-based fracmemristor bridge circuit is demonstrated in Fig. 17, which can be applied to explain the action potential of a neuron.

According to Fig. 17, when the input voltage is equal to zero, namely, there is no input voltage, the

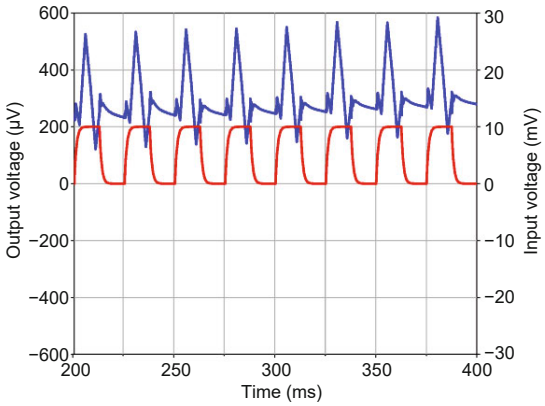

Fig. 17 Output voltage of a pulse-based fracmemristor bridge circuit with the fundamental frequency $f_0 = 40$ Hz. Red corresponds to the right vertical axis and blue corresponds to the left vertical axis. References to color refer to the online version of this figure

output voltage gradually decreases but cannot decay to zero. For a stable system, its response approaches a steady state eventually. Thus, it is reasonable for the output voltage of the pulse-based fracmemristor bridge circuit to reach a steady state without input voltage, which also proves that this circuit has memory.

5 Conclusions

In this study, the FMNSW using a pulse-based fracmemristor bridge circuit was investigated and discussed in detail. Electrical characteristics of a pulse-based fracmemristor bridge circuit can be used to explain the cellular mechanisms that underlie learning and memory such as LTP, LTD, habituation, and sensitization. This application is considered as a major advantage.

In addition, pulse-based fracmemristor bridge circuit could be employed to produce an appropriate signal for the brain-computer interface, which is superior to the traditional integer-order memristive neural synaptic weightings. It is difficult for patients with diseases such as paraplegia and myasthenia to move and communicate. Specific brain neural signals can be produced by the pulse-based fracmemristor bridge circuit to control the body of the patient to help move or communicate like a healthy person. As the signal produced by the pulse-based fracmemristor bridge circuit is very similar to the brain neural signal, this kind of control conforms very well to the natural physiology.

The study is a preliminary work on the application of fracmemristor in fractional-order memristive synapses. Solving other related problems will be the topic for future studies. For instance, this research discussed solely the half-order pulse-based fracmemristor bridge circuit. Therefore, arbitrary-order pulse-based fracmemristor bridge circuits and investigating ways to use arbitrary-order pulse-based fracmemristor bridge circuits to describe synaptic behaviors need to be analyzed in future work.

Contributors

Yifei PU designed the research. Bo YU and Qiuyan HE processed the data. Yifei PU and Qiuyan HE drafted the manuscript. Bo YU and Xiao YUAN helped organize the manuscript. Yifei PU, Bo YU, Qiuyan HE, and Xiao YUAN revised and finalized the paper.

Compliance with ethics guidelines

Yifei PU, Bo YU, Qiuyan HE, and Xiao YUAN declare that they have no conflict of interest.

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