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A large-current, highly integrated switched-capacitor divider with a dual-branch interleaved topology and light load efficiency improvement*

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Abstract: Because it is magnet-free and can achieve a high integration level, the switched-capacitor (SC) converter acting as a direct current transformer has many promising applications in modern electronics. However, designing an SC converter with large current capability and high power efficiency is still challenging. This paper proposes a dual-branch SC voltage divider and presents its integrated circuit (IC) implementation. The designed SC converter is capable of driving large current load, thus widening the use of SC converters to high-power applications. This SC converter has a constant conversion ratio of 1/2 and its dual-branch interleaved operation ensures a continuous input current. An effective on-chip gate-driving method using a capacitively coupled floating-voltage level shifter is proposed to drive the all-NMOS power train. Due to the self-powered structure, the flying capacitor itself is also a bootstrap capacitor for gate driving and thus reduces the number of needed components. A digital frequency modulation method is adopted and the switching frequency decreases automatically at light load to improve light load efficiency. The converter IC is implemented using a 180 nm triple-well BCD process. Experimental results verify the effectiveness of the dual-branch interleaved operation and the self-powered gate-driving method. The proposed SC divider can drive up to 4 A load current with 5–12 V input voltage and its power efficiency is as high as 96.5%. At light load, using the proposed optimization method, the power efficiency is improved by 30%.

Key words: Switched-capacitor converter; Dual branch; Integrated circuit; Bootstrap gate driver
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1 Introduction

Compared with switched-inductor converters like buck or boost converters, the magnet-free switched-capacitor (SC) converter is superior in size and power density, and is ideal for integrated implementation. The charge pump (CP) circuit (Palumbo and Pappalardo, 2010; Luo et al., 2017), a widely known kind of SC converter, has been vastly employed in nonvolatile memories, energy harvesters, liquid crystal display drivers, etc. The traditional use of an SC converter has been confined to low-power applications or even with pure capacitive loads. However, in recent years, much work (Sanders et al., 2013; Andersen et al., 2017) has been done to widen the use of SC converters to high-power applications (load current I_L>1 A). An SC converter has very high power efficiency when it realizes a conversion ratio based on its topology. In the direct current (DC) transformer model of an SC converter, as shown in Fig. 1, M is the ideal DC voltage

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conversion ratio without load and R_{out} represents the loss caused by charge transfer on capacitors and the resistive conduction loss on MOSFETs.

An SC converter has many promising applications in modern electronics (Fei et al., 2017; Jong, 2019). In Fig. 1a, it is an intermediate stage to supply the point-of-load (POL) regulators that will finally power system-on-chips (SoCs), microprocessors, field programmable gate arrays (FPGAs), etc. Because the SC converter has already halved the input voltage, the POL regulators can operate at a higher switching frequency and have a smaller solution size. MOSFET's voltage stress is reduced and the switching loss is lowered for the voltage regulator (VR), resulting in a higher efficiency. In a DC transformer, the output current is doubled when the output voltage is halved. As shown in Fig. 1b, with the help of the voltage divider or current doubler, the standard type-C^{TM} cable with the maximum current of 3 A can still be used for charging current up to 6 A in a smartphone direct charging application (DA9318, 2017).

Many methods have been proposed (Seeman and Sanders, 2008; Zhang et al., 2008; Schaef et al., 2018) for high-power applications, whereas implementing an SC converter needs more consideration. An SC converter has a larger number of power switches than an inductive converter. For a high-voltage converter (the highest node voltage is larger than the rated voltage of the MOSFET), it should be guaranteed that the voltage each transistor withstands is within its rated voltage. For a large-current converter, each phase should be driven independently and reasonable dead time must be ensured to avoid unbearable short-circuit current. An all-NMOS power train is preferred because the PMOS transistor has inferior mobility, and the bootstrap drive technique is then usually needed (Liu ZD et al., 2015; Yuan et al., 2020). All these issues make the gate driving of large-current SC converters quite intractable. Some researchers (Andersen et al., 2017) tended to use PMOS transistors when necessary with the penalty of inferior mobility. Xu et al. (2006) and Meyvaert et al. (2015) used an all-NMOS power train; however, the former needed a large number of bootstrap capacitors, and the latter required an additional auxiliary rail generator.

This paper proposes a dual-branch SC voltage divider to ensure a continuous input current, thereby greatly reducing the electromagnetic interference (EMI) noise. An efficient gate-driving method is also proposed for high-power SC converters. The uniqueness of this method is to adopt internal nodes of the power stage as the power supply for the driver and reuse the flying capacitor as the bootstrap capacitor, thus simplifying the driving circuit and reducing the cost. A digital frequency modulation method is adopted and the switching frequency decreases automatically to improve the light load efficiency. A chip implemented with a 180 nm triple-well BCD process is designed and tested to verify the effectiveness of the proposed dual-branch SC divider and its gate-driving method.

2 Power stage of the proposed SC divider and consideration of power efficiency

There are many SC topologies (Fardahar and Sabahi, 2020; Liu WL et al., 2020), such as ladder,

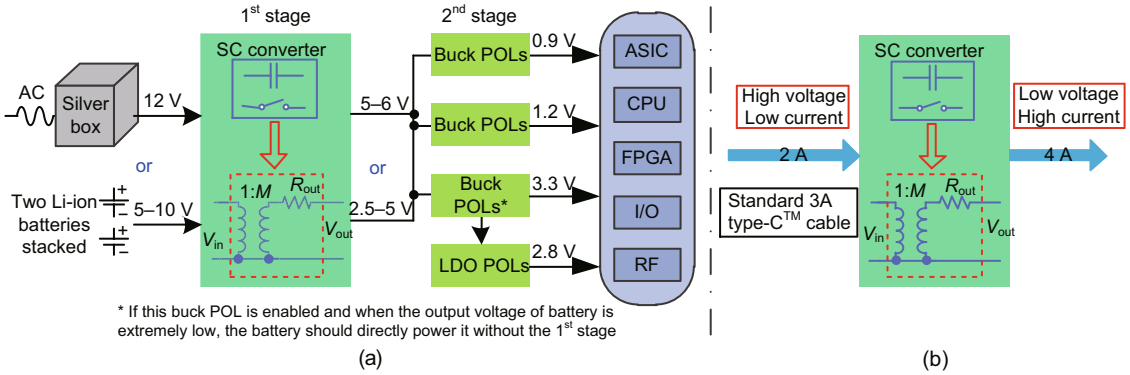

Fig. 1 Application scenarios of the SC converter used as a DC transformer: (a) SC converter used as a high efficiency first power stage in a distributed power architecture; (b) smartphone direct charging

series-parallel, Dickson, and Fibonacci. However, they can converge to a simple voltage divider when realizing a 2-to-1 voltage ratio. We use this simple voltage divider and further extend it to dual-branch interleaved operation.

2.1 Dual-branch interleaved SC divider and its operation process

The designed SC DC-DC converter has the function of halving the input voltage, and features large current capability and high power efficiency. The main topology of its power stage uses a dual-branch structure, as shown in Fig. 2.

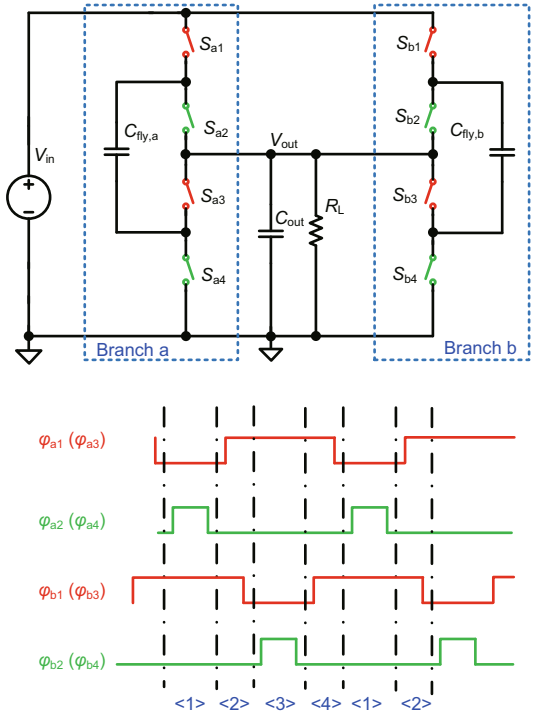

Fig. 2 Main topology of the proposed dual-branch interleaved SC divider and clock phases to drive the eight power switches

The main topology is divided into parallel left and right branches. Each branch includes four power switches and one flying capacitor. By reasonably arranging the clock phase which drives the power switches of branch a (or branch b), the flying capacitor and the output capacitor are in series and then in parallel within one clock cycle, thus achieving the function of halving the input voltage ($V_{out} = 1/2 \times V_{in}$).

Based on the halving function of each branch, the dual-branch interleaved operation ensures a continuous input current, and can effectively reduce the output voltage ripple and increase its driving capability of large current load.

The clock phases to drive the eight power switches of the dual-branch SC divider are also shown in Fig. 2. When the clock signal is high, the corresponding power switch turns on and vice versa. The driving clocks of branch a or b are two-phase non-overlapping clocks, thereby avoiding unbearable short-circuit current when the power switch changes its state. Meanwhile, the driving clocks of branches a and b are interleaved to make sure that during one entire clock period, at least one of the two power switches S_{a1} and S_{b1} is being turned on. Thus, this divider's power supply is always connected to the circuit, and the input current is continuous to reduce the EMI noise.

The operation phase transition diagram of the proposed SC divider is shown in Fig. 3. During one entire clock period, the power stage will go through eight operation states, of which <1>, <2>, <3>, and <4> are the main states and will last a relatively long time. The interval between one main state and the following one is the dead time of each branch's non-overlapping clock.

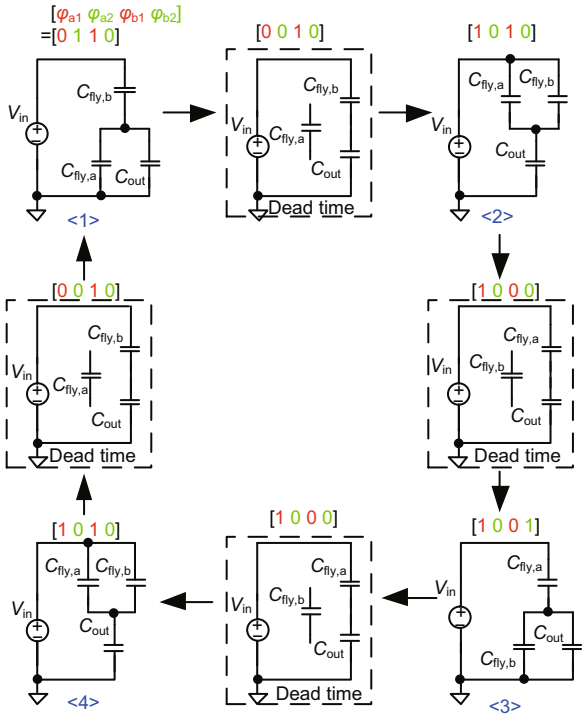

Fig. 3 Phase transition diagram of the divider

2.2 Consideration of power efficiency

In the DC transformer model of an SC converter as shown in Fig. 1, $R_{\rm out}$ represents the loss caused by charge transfer on capacitors and the resistive conduction loss on MOSFETs. Considering driving a resistive load $R_{\rm L}$, the power efficiency of this SC converter is

$$\eta=\frac{R_{\rm L}}{R_{\rm L}+R_{\rm out}}. \tag{1}$$

As Eq. (1) indicates, the smaller the $R_{\rm out}$ value is, the higher the power efficiency will be. Aiming at a high-efficiency SC converter, key design parameters related to output impedance must be found and chosen to achieve a small $R_{\rm out}$.

Using the analysis methods in Seeman and Sanders (2008) and Schaef et al. (2018), the output impedance $R_{\rm out}$ of an SC converter in the slow switching limit (SSL) case can be expressed as

$$R_{\rm SSL}=\sum_i \frac{\alpha_{{\rm c},i}^2}{C_i f_{\rm sw}}, \tag{2}$$

where C_i represents the $i^{\rm th}$ flying capacitor in each branch of the SC converter and $f_{\rm sw}$ is the switching frequency.

For each branch of the divider, there is only one flying capacitor and $i=1$. The parameter $\alpha_{{\rm c},i}$ equals 1/2. To achieve a high efficiency for high-power application ($I_{\rm L}$>1 A), $C_{\rm fly}$ must be very large, and here we choose $C_{\rm fly}=94$ μF (two 47 μF ceramic capacitors in parallel) with $f_{\rm sw}=500$ kHz.

In addition, the output impedance $R_{\rm out}$ of an SC converter in the fast switching limit (FSL) case can be expressed as

$$R_{\rm FSL}=2\sum_i R_i\alpha_{{\rm r},i}^2, \tag{3}$$

where R_i represents the on-resistance of the $i^{\rm th}$ power switch in each branch of the SC converter.

For each branch of the divider, there are four power switches and $i=4$. The parameter $\alpha_{{\rm r},i}$ equals 1/2. Suppose that all the power switches have the same on-resistance $R_{\rm on}$:

$$R_{\rm FSL}=2\times 4\times (0.5)^2\times R_{\rm on}=2R_{\rm on}. \tag{4}$$

In the design of a large-current SC converter, the power switch must be chosen especially large to achieve a small on-resistance (around 20 mΩ). In our design, the length of the power switch is 500 nm and the width of each cell is 50 μm. There are tens of thousands of basic cells in parallel, and as shown later in the micrograph of the chip, the power MOSFETs take up a large portion of the whole area.

3 On-chip self-powered bootstrap gate driver using capacitively coupled floating-voltage level shifter

The converter integrated circuit (IC) is implemented using 5 V devices and 12 V LDMOS devices with 5 V gate oxide. In each branch, for S_2, S_3, and S_4, $V_{\rm in}$ cannot be used to power their drivers, although it is possible for a low-voltage application ($V_{\rm in}$<5 V). Because S_1 is N-type, to switch on it completely, a voltage higher than $V_{\rm in}$ (e.g., 7.5 V with $V_{\rm in}$ being 5 V) is needed. For S_1 and S_3, because their source potentials ($V_{{\rm SW}_1}$ and $V_{{\rm SW}_2}$) change with phase, the corresponding driver must also be able to adapt to the change accordingly.

3.1 Self-powered bootstrap gate driver with the flying capacitor being reused

Fig. 4 shows the traditional bootstrap gate-driving method. It has been widely adopted (Liu ZD et al., 2015; Yuan et al., 2020) to drive the dual-NMOS power train for a buck converter. Xu et al. (2006) used the same structure to drive an SC voltage divider, and two bootstrap capacitors must be used because there is one more switching point in this voltage divider than in a buck converter.

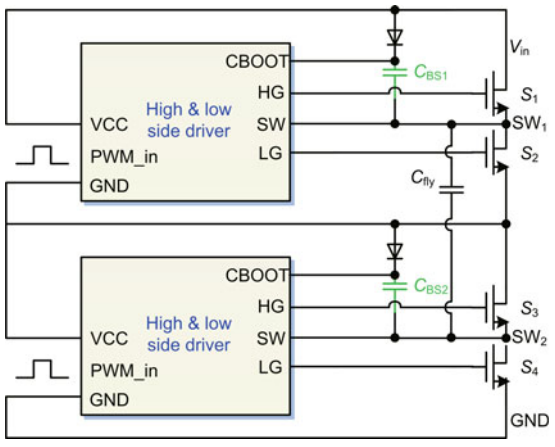

Fig. 4 A traditional gate-driving method using the bootstrap technique

Note that in the power stage of this SC voltage divider, nodes $V_{\rm in}$, $V_{\rm out}$, and GND (ground) are

DC potentials, whereas nodes SW_1 and SW_2 are two switching points. SW_1 alternates its potential between V_{in} and V_{out}, and SW_2 alternates its potential between V_{out} and GND. Flying capacitor C_{fly} is placed between SW_1 and SW_2 to shuttle charge from V_{in} to V_{out}, and its capacitance is quite large.

Fig. 5 shows the proposed C_{fly} reused gate-driving technique based on the above analysis. By carefully examining the terminal potentials of the flying capacitor, its stored charge may be used to power a suitable power MOSFET. Specifically, in each branch of this SC 2-to-1 converter, the stored charge of C_{fly} can be used to power S_3. Fig. 6 presents the operation of the proposed gate driver. Because C_{fly} now has two roles, during clk_phi2, it still has to shuttle charge to C_L when C_{BS} is charged. During clk_phi1, it is charged and also functions as the power supply for S_3.

For S_1, an auxiliary rail generator or an extra bootstrap capacitor must be needed, and here an external bootstrap capacitor C_{BS} is used. A power switch S_P is adopted to charge C_{BS}. The stimulating signal for S_P is also clk_phi2, but the inverter chain has an inverting gain.

As shown in Fig. 6, when S_2 and S_4 are turned on, S_P is also turned on, and C_{BS} is charged to the voltage of about $0.5 \times V_{in}$. When S_1 and S_3 are turned on, the voltage across C_{BS}, V_{CBS}, can be used to switch on S_1, and the node potential V_{BS} at the top plate of C_{BS} is now about $1.5 \times V_{in}$, which ensures that S_1 can be turned on completely.

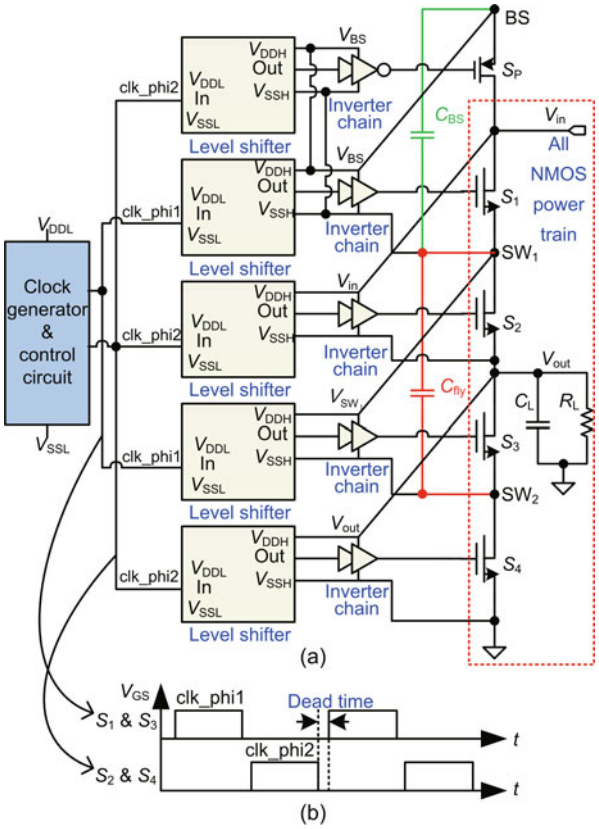

Fig. 5 Proposed C_{fly} reused bootstrap gate driver for branch a or b (a) and non-overlapping two-phase clock signals (b)

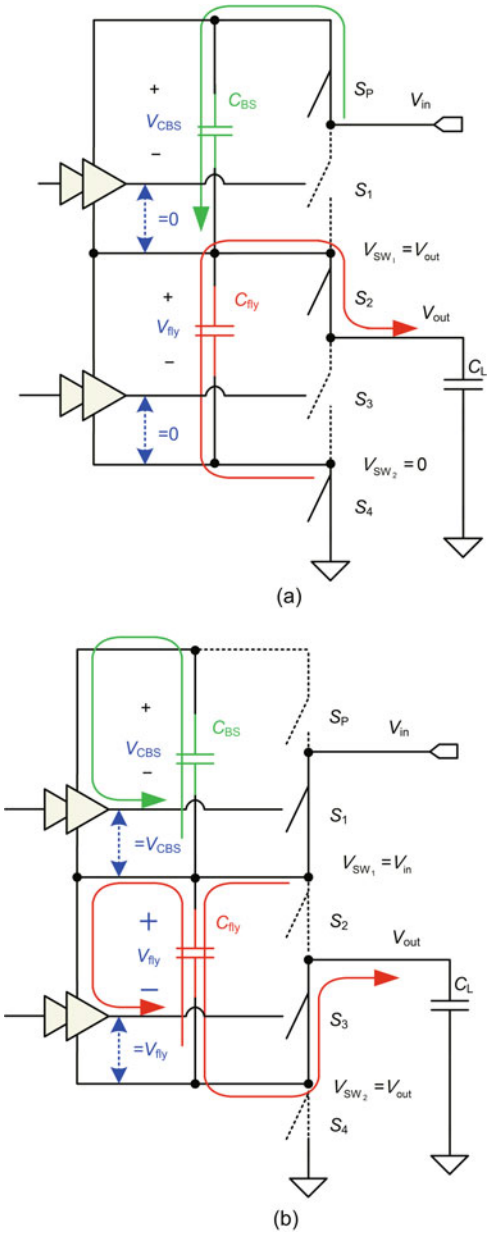

Fig. 6 Operation of the C_{fly} reused bootstrap gate driver: (a) during clk_phi2, C_{BS} is charged, whereas C_{fly} is discharged; (b) during clk_phi1, C_{BS} is the power supply for S_1, whereas C_{fly} is the power supply for S_3 and it is charged

The main difference in our method from the previous driving methods is the sufficient use of internal nodes of the power stage to power the gate driver. The features of this self-powered gate driver are as follows:

1. The traditional bootstrap gate-driving method uses only the nodes with DC potentials in the power stage to power the driver. In Fig. 5, SW_1 and SW_2 are also used to power the gate driver. As a result, the flying capacitor C_{fly} itself is also the bootstrap capacitor for S_3. Thus, only one extra bootstrap capacitor C_{BS} is needed to drive S_1.

2. A power switch S_P is adopted instead of a diode, and thus C_{BS} can be more fully charged. S_P is controlled to be synchronous with S_2 and S_4.

3. Instead of the full-swing level shifter, whose output voltage and input voltage have the same reference voltage, a floating-voltage level shifter that shifts input signal to output signal with a different reference voltage is designed.

3.2 Capacitively coupled high-speed floating-voltage level shifter

As shown in Fig. 5, a floating-voltage level shifter is essential for the gate driver using this self-powered structure and it must be carefully designed.

Fig. 7 shows the proposed level shifter used in this design. All the level shifters in Fig. 5 use this structure, although an LDMOS transistor is needed only for the driving circuitry related to S_1. MN_1 and MN_2 are used to pull down out+ or out− in the floating circuitry between V_{DDH} and V_{SSH}. MP_1 and MP_2, whose gates are connected to V_{SSH}, are used to clamp the lower voltage of out+ and out− to be V_{SSH}. In the floating circuitry, latch-based circuits finally generate the output digital signal using the internal positive feedback.

Based on the design in Moghe et al. (2011), a capacitive route from input signal to the output signal is added to increase the switching speed. C_1 and C_2 are two metal-oxide-metal (MOM) capacitors constructed with routing metals. Using two metal layers, each of these two capacitors takes up an area of about 24 μm×12 μm to generate an effective capacitance of around 100 fF.

Fig. 8 shows the transient voltage waveforms of several key nodes with a load capacitance of 100 fF. The effect of the added coupled capacitors is distinctively reflected in the waveform of node out+ as circled in red. Simulation results showed a delay time of around 1.3 ns with $V_{SSL} = 0$ V and $V_{DDL} = V_{DDH} - V_{SSH} = 4$ V. Table 1 shows the performance summary of the proposed level shifter and the comparison with other state-of-the-art floating-voltage level shifter designs under similar working conditions.

4 Frequency modulation to improve light load power efficiency

Previous consideration of power efficiency in Section 2 ensures high efficiency at a heavy load.

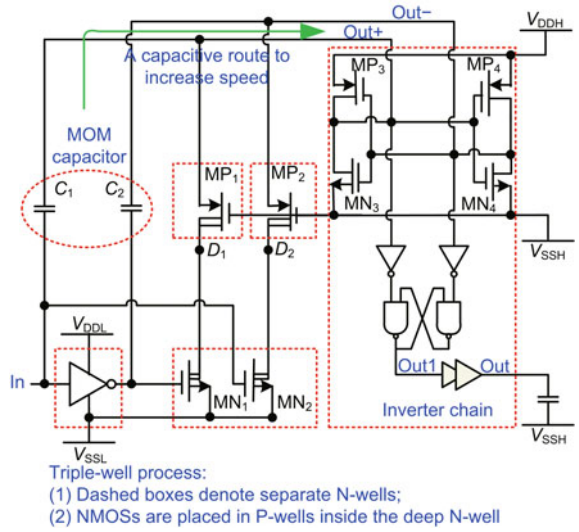

Fig. 7 Proposed capacitively coupled floating-voltage level shifter

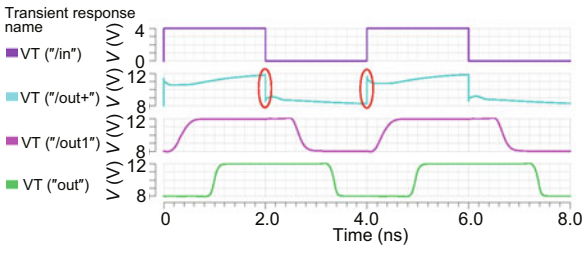

Fig. 8 Transient voltage waveforms of key nodes of the level shifter

Reference to color refer to the online version of this figure

Table 1 Performance comparison of the proposed floating-voltage level shift circuit with other methods

Method	V_{SSH} (V)	V_{DDH} (V)	Delay (ns)	Verification method
Moghe et al. (2011)'s	6.7	10.0	7.7	Measurement
Moghe et al. (2011)'s	6.7	10.0	2.2	Measurement
Lehmann (2014)'s	9.5	12.0	2.0	Simulation
Ours	8.0	12.0	1.3	Simulation

However, at light load, if the power converter continues to operate at a high frequency, the switching loss will become the primary cause of power loss. As a result, it is necessary to automatically decrease switching frequency at light load to improve the power efficiency.

Fig. 9 shows the proposed digital frequency modulation method to optimize the power efficiency. With a constant frequency of 500 kHz, the output voltage will continue to increase as the load decreases; at light load, the output voltage will be very close to half of the input voltage. Based on the above analysis, a window comparator including two comparators (Fig. 9a) is used to compare the sensed output voltage $V_{\mathrm{out,s}}$ ($0.5 \times V_{\mathrm{out}}$) with V_{in,S_1} ($0.242 \times V_{\mathrm{in}}$) and V_{in,S_2} ($0.236 \times V_{\mathrm{in}}$). The purpose is to maintain $V_{\mathrm{out,s}}$ between V_{in,S_1} and V_{in,S_2}.

As Fig. 9b indicates, if the output of the window comparator [SEL1, SEL2] = [1, 1], it means that the output voltage is too high and that the frequency selection module will decrease the switching frequency step by step. If [SEL1, SEL2] = [0, 1], it means that $V_{\mathrm{out,s}}$ is between V_{in,S_1} and V_{in,S_2}, and that the current operation frequency is appropriate. The power converter will operate with the current switching frequency. However, when [SEL1, SEL2] = [0, 0], the frequency selection module will decide that the output voltage is too low and that the switching frequency must go back to 500 kHz immediately. This aims to reduce the undershoot voltage, and the control logic makes sure that the goal of maintaining V_{out} near half of V_{in} has priority to the consideration of power efficiency.

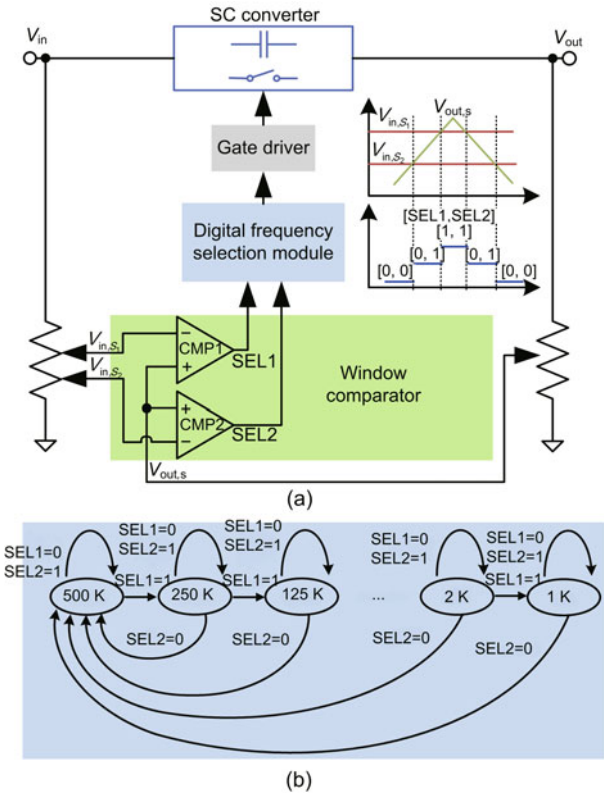

Fig. 9 Proposed digital frequency modulation method (a) and control logic of the digital frequency selection module (b)

The proposed frequency modulation method is digital, and thus is robust. Unlike Souvignet et al. (2015), Mostacciuolo et al. (2018), or Jawalikar et al. (2020), no complicated loop stability consideration or complicated modeling of the power stage is needed.

5 Experimental results

The designed chip and the printed circuit board (PCB) for testing are shown in Fig. 10. A 180 nm

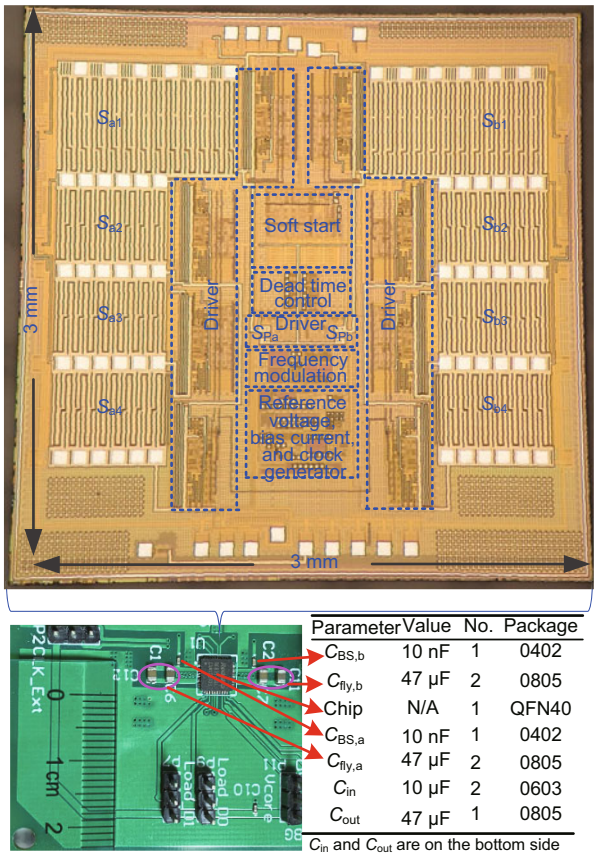

Fig. 10 Chip micrograph of the designed SC voltage divider with each function block being enclosed and the evaluation PCB

triple-well BCD process is used to design the converter IC. The gate driver and power switches are all integrated on the chip. For each branch, S_2, S_3, and S_4 are regular low-voltage devices, whereas S_1 is an LDMOS. Only in the soft-start process, does V_{DS} of S_1 need to withstand the full input voltage. External ceramic capacitors are needed for high-power applications and C_{fly} equals 94 μF (2 × 47 μF) for each branch. The chosen external bootstrap capacitor C_{BS} is 10 nF for each branch.

Fig. 11 shows the measured voltage waveforms of the switching nodes (SW_1 and SW_2) of branches a and b. For each branch, V_{SW_1} can change between V_{in} and V_{out} successfully, and V_{SW_2} can change between V_{out} and GND successfully. This verifies that all the eight power switches in the dual branch power stage can be turned on or off successfully and that each branch works normally. It is clear from Fig. 11 that these two branches do not work at the same time, and by carefully examining the waveforms, SW_1 of branch a will not change to V_{out} before SW_1 of branch b changes to V_{in}, and vice versa. This verifies that there is at least one of the two power switches, S_{a1} and S_{b1}, being turned on, and that the interleaved operation of the dual-branch SC divider is as described in Section 2.

Fig. 12 shows the measured voltage waveforms of nodes BS and SW_2 of branch a (the same for branch b). With only one extra bootstrap capacitor, the gate driver can successfully bootstrap V_{BS} to about $1.5\times V_{in}$. As a result, S_{a1} can be switched on effectively to achieve high power efficiency and verifies that the proposed on-chip self-powered bootstrap gate driver with the flying capacitor being reused and using capacitively coupled floating-voltage level shifter in Section 3 is feasible.

Fig. 13 shows the measured voltage waveforms of V_{out} and node SW_2 of branch a. Because the power converter now works at a heavy load, the switching frequency is 500 kHz. However, it is clear that the frequency of the ripple voltage of V_{out} is 1 MHz as a result of the interleaved operation of this dual-branch SC voltage divider.

Fig. 14 shows the modulation process of the operation frequency at light load. This is observed from a test pin which can reflect the clock signal generated by the digital frequency selection module in Section 4. When the load changes from heavy to light, the window comparator decides that the output voltage is too high and that the frequency selection module reduces the switching frequency step by step. This verifies the feasibility of the proposed digital frequency modulation method in Section 4.

Fig. 15 shows the measured operation frequency of this SC divider as load current varies. This is the modulation result of the switching frequency with a corresponding load current. As load current decreases, the frequency modulation circuit will produce a lower switching frequency as analyzed in

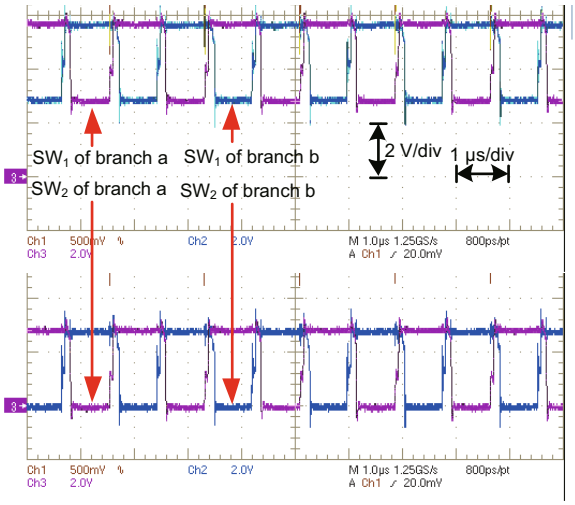

Fig. 11 Measured voltage waveforms of switching nodes (SW_1 and SW_2) of branches a and b with I_L = 1 A and V_{in} = 6 V

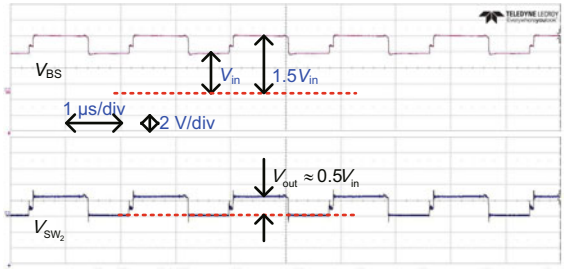

Fig. 12 Measured voltage waveforms of nodes BS and SW_2 of branch a

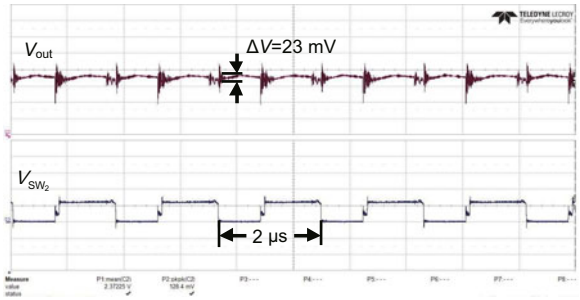

Fig. 13 Measured voltage waveforms of V_{out} and node SW_2 of branch a when I_L = 1 A

Section 4. This proves the effectiveness of the proposed frequency modulation method, and the converter can decrease the switching frequency automatically at the light load to improve the power efficiency.

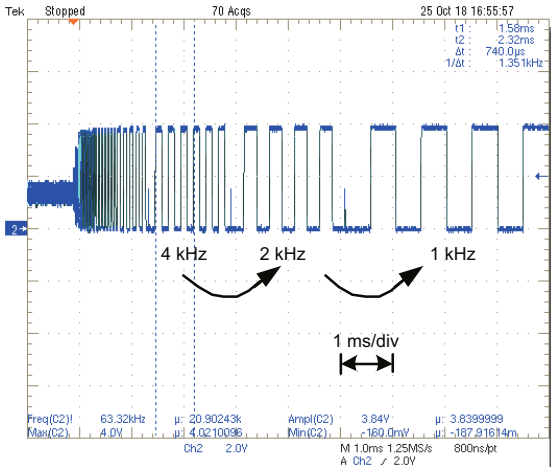

Fig. 14 Modulation process of the operation frequency at light load (observed from a test pin)

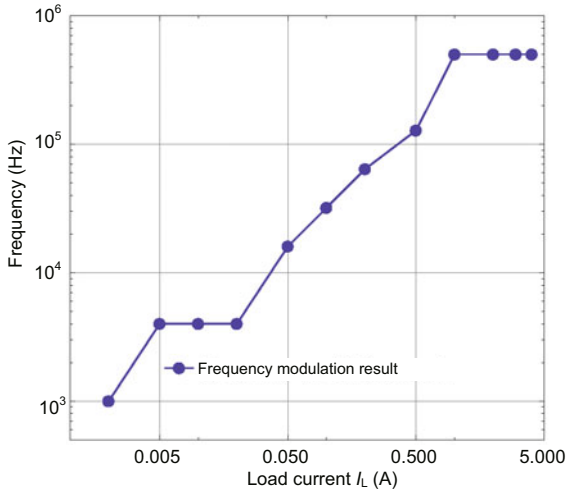

Fig. 15 Operation frequency variation with load current I_L

Fig. 16 shows the measured power efficiency of the SC voltage divider under different load conditions. The input voltage is set at 5.2 V, and the power efficiency can be as high as 96.5%. It should be noted that with the increase in input voltage, its power efficiency also increases a little. This is very different from VRs like the buck converter. The reason is that as the input voltage increases, unlike a buck converter whose output voltage should remain unchanged, the output voltage will also increase and the gate-source voltage V_{GS} of each power switch increases, resulting in smaller on-resistance and higher power efficiency.

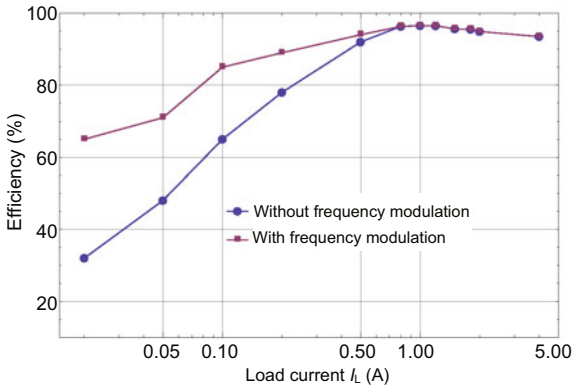

Fig. 16 Measured power efficiency with or without the frequency modulation method

Fig. 16 also shows the effect of frequency modulation. At low load, with operating frequency fixed at 500 kHz, the power efficiency will decrease drastically due to the relatively large switching loss. Using the proposed optimization method, the switching loss is reduced as the operation frequency decreases, and the power efficiency is improved by 30%.

Table 2 compares the proposed dual-branch SC divider and the gate-driving method with other high-power SC converters. The proposed design features dual-branch interleaved operation and is unique because it reuses the flying capacitor as the bootstrap capacitor. Unlike Xu et al. (2006), in which the converter was realized with discrete components, the power switches and driving circuits of this design are on-chip, verifying the feasibility of a highly integrated high-power SC converter solution. Because the power switches in Xu et al. (2006) are off-chip, power switches with smaller on-resistance can be chosen conveniently to maximize the power efficiency. This also indicates that the current consideration of power efficiency in Section 2.2 is not sufficient, and that there is still room to optimize the power efficiency of the proposed integrated SC divider. Compared with Meyvaert et al. (2015), an auxiliary rail generator is no longer needed, thus simplifying the design of driving circuit, and the chip area occupied by the rail generator can be saved. Xu et al. (2006) and Schaef and Stauth (2018) did not need an auxiliary rail generator either, but they did need bootstrap capacitors. Because there is no reuse of flying capacitor, the number of bootstrap

Table 2 Performance summary and comparison with other methods

Performance	Xu et al. (2006)	Meyvaert et al. (2015)	Schaef and Stauth (2018)	This work
Process	Discrete components	140 nm SOI, 3.3 V MOS 20 V LDMOS with 3.3 V gate oxide	180 nm CMOS, 5 V MOS, 15 V LDMOS with 5 V gate oxide	180 nm BCD, 5 V MOS, 12 V LDMOS with 5 V gate oxide
Converter topology	2:1 SC	11:1 SC	3:1 ReSC (inductor needed)	2:1 SC (dual-branch)
C_{fly} number	1	5	2	2
C_{fly} size (μF)	6×22	10	330×10^{-3}	2×47
Gate driver	Bootstrapping with C_{BS}	Auxiliary rail generator designed	Bootstrapping with C_{BS}	Bootstrapping with C_{BS} and C_{fly}
Reuse of C_{fly}	No	No	No	Yes
Number reduction of C_{BS}	0	N/A	0	2
V_{in} (V)	12–16	37.42	12	5–12
V_{out} (V)	6–8	3.3	3.7	2.5–6
Maximum I_{L} (A)	8	0.042	1.2	4
f_{sw} (kHz)	350	100	1700	500
$\mathrm{Efficiency}_{\mathrm{peak}}$	98%	95.5%	87.5%	96.5%

SC: switched-capacitor; ReSC: resonant SC; N/A: not applicable

capacitors cannot be reduced. Xu et al. (2006) needed two bootstrap capacitors to drive the same SC 2-to-1 voltage divider. If the power stage is dual-branch, four bootstrap capacitors are needed, and thus the solution size and cost will be increased. Schaef and Stauth (2018) adopted a resonant SC (ReSC) converter rather than an SC one and the converter worked at a higher operation frequency, making it inappropriate to directly compare the power efficiency. However, the driving technique can be compared, and because there was no reuse of flying capacitor in Schaef and Stauth (2018), the number of bootstrap capacitors and the corresponding cost and space taken up cannot be reduced. In contrast, the proposed structure reuses the flying capacitor as a bootstrap capacitor, thus reducing the number of needed bootstrap capacitors, simplifying the driving circuit, and reducing the solution cost.

6 Conclusions

This paper proposes an SC voltage divider with dual interleaved operation and a self-powered gate-driving technique for high-voltage high-power SC DC-DC converters. With the interleaved operation of the dual-branch power stage, the power supply of this divider is always connected to the circuit, and the EMI noise is continuously reduced by the input current. Using the proposed self-powered structure, the flying capacitor itself is also a bootstrap capacitor, and the number of needed bootstrap capacitors is reduced, thus simplifying the driving circuit and reducing the cost. In addition, a capacitively coupled high-speed floating-voltage level shifter is designed to implement the gate driver. A prototype chip using a 180 nm triple-well BCD process is designed. Measured power efficiency and experimental results of the voltage waveforms of key nodes verify the feasibility of the proposed dual-branch power stage and the self-powered gate-driving method. The digital frequency modulation method to improve light-load efficiency is also verified through experiment. The proposed self-powered gate-driving technique with the flying capacitor being reused can be readily applied in other SC DC-DC converter topologies.

Contributors

Sheng LIU, Zhao YANG, and Haonan WU designed the converter and performed the test. Menglian ZHAO supervised the research work. Sheng LIU drafted the paper. Xiaobo WU helped organize the paper. Sheng LIU and Menglian ZHAO revised and finalized the paper.

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Compliance with ethics guidelines

Sheng LIU, Menglian ZHAO, Zhao YANG, Haonan WU, and Xiaobo WU declare that they have no conflict of interest.

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