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# Design and optimization of a gate-controlled dual direction electro-static discharge device for an industry-level fluorescent optical fiber temperature sensor*

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**Abstract:** The input/output (I/O) pins of an industry-level fluorescent optical fiber temperature sensor readout circuit need on-chip integrated high-performance electro-static discharge (ESD) protection devices. It is difficult for the failure level of basic N-type buried layer gate-controlled silicon controlled rectifier (NBL-GCSCR) manufactured by the 0.18 μm standard bipolar-CMOS-DMOS (BCD) process to meet this need. Therefore, we propose an on-chip integrated novel deep N-well gate-controlled SCR (DNW-GCSCR) with a high failure level to effectively solve the problems based on the same semiconductor process. Technology computer-aided design (TCAD) simulation is used to analyze the device characteristics. SCRs are tested by transmission line pulses (TLP) to obtain accurate ESD parameters. The holding voltage (24.03 V) of NBL-GCSCR with the longitudinal bipolar junction transistor (BJT) path is significantly higher than the holding voltage (5.15 V) of DNW-GCSCR with the lateral SCR path of the same size. However, the failure current of the NBL-GCSCR device is 1.71 A, and the failure current of the DNW-GCSCR device is 20.99 A. When the gate size of DNW-GCSCR is increased from 2 μm to 6 μm, the holding voltage is increased from 3.50 V to 8.38 V. The optimized DNW-GCSCR (6 μm) can be stably applied on target readout circuits for on-chip electrostatic discharge protection.

**Key words:** Electric breakdown; Semiconductor device reliability; CMOS technology
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## 1 Introduction

In the application of industry-level fluorescent optical fiber temperature sensors, a harsh environment with strong electrostatic interference often results in damage to the sensor core chip. The working principle of the temperature sensor is that the fluorescent substance emits a fluorescent signal after being excited by an external light source. When the external excitation light source stops, its fluorescent signal does not disappear immediately, but will show an exponential decay. The decay time is the fluorescence lifetime. The fluorescence lifetime has a single

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functional relationship with the external temperature. As the temperature increases, the fluorescence lifetime decreases. The back-end signal processing circuit can detect the fluorescence lifetime to know the change of the outside temperature. The slew rate of the integrated operational amplifier used in an industry-grade fluorescent fiber temperature sensor system is 8.5–10.5 V. The protection level of traditional electro-static discharge (ESD) protection devices is between 2 kV and 8 kV. When industry-grade fluorescent optical fiber temperature sensors work in extreme outdoor environments, it is difficult for traditional ESD devices to resist ESD pulses higher than 8 kV, and they cannot ensure the reliability and stability of the sensors. To improve the reliability of industry-level sensors, it is necessary to strengthen the ESD protection of the chip input port and output port. The input/output (I/O) pins of the chip readout circuit need to integrate on-chip ESD protection devices with a human body model (HBM) level greater than 30 kV. Dual direction silicon controlled rectifiers (DDSCRs) have received attention as high-performance on-chip integrated ESD devices. The on-chip integrated ESD device has rigorous requirements for its ESD window. More and more on-chip protection requires ESD devices with bidirectional electrostatic discharge to ensure that the I/O pins of chips are not affected by ESD pulses. Designing a high-failure-level SCR device that can be applied to industry-level strong electromagnetic interference environments is one of the most difficult problems to be solved at present.

With the development of integrated circuits, SCRs have been optimized and advanced scientific research has been conducted (Chen XJ et al., 2019; Wang et al., 2020). To achieve high-speed electrostatic discharge protection, Zhang et al. (2019) improved the diode-triggered SCR (DTSCR), which can be applied to nanosecond-level ESD events. Liang et al. (2019) studied a gate diode-triggered SCR (GDTSCR) for high-voltage ESD protection, which has a trigger voltage of less than 17 V, a holding voltage of 15 V, and a powerful current handling capability. More importantly, GDTSCR can be effectively applied to a specific high-voltage area for bidirectional ESD protection. Du et al. (2019) proposed an enhanced bidirectional modified lateral SCR (EBMLSCR) for advanced ESD protection applications with a low trigger voltage (7.7 V) and high failure current (6.5 A). SCR can meet various ESD windows (Chen JT et al., 2017; Yen et al., 2017; Hou et al., 2019; Qi et al., 2019; Zheng et al., 2019) by changing the structure and layout of the device, so it is applied to various ESD environments. However, in the context of high-voltage, high-power chip applications, higher requirements are placed on on-chip integrated SCR devices. Wang et al. (2015) proposed a bidirectional SCR device (laterally diffused metal oxide semiconductor DDSCR) for a communication bus with a 33 V trigger voltage and a current release capability of 87 mA/μm. Zhan et al. (2013) proposed a high-voltage bidirectional SCR device for automotive applications. The current release capability of the device reached 120 mA/μm through transmission line pulses (TLP) test. All the above studies solve many problems in the application field of specific ESD devices (Huang et al., 2016; Dai and Ker, 2018; Hu et al., 2018; Lee et al., 2018). In this paper we analyze the ESD protection index requirements of the readout circuit of an industry-level fluorescent optical fiber temperature sensor. The normal operating voltage of the circuit is −5–5 V. The minimum gate oxide breakdown voltage (BV) is 30 V, and the safety margin is 20%. Therefore, the trigger voltage of the ESD device needs to be between 6 V and 24 V. The holding voltage is higher than 6 V, and the secondary clamp-voltage is lower than 24 V. In addition, because the application environment of industry-grade sensors is very harsh, the ESD protection level of the readout circuit needs to be optimized. The HBM level of the improved ESD device needs to be greater than 30 kV (when the clamp-voltage of the ESD device reaches 24 V, its release current needs to be greater than 20 A) to ensure the reliability of the sensor core circuit. The on-chip integrated single photon detection chip ESD application circuit is shown in Fig. 1. A single photon avalanche diode (SPAD) can convert optical signals into DC signals. The photocurrent signal is converted into a voltage signal through a sampling resistor. The unit operational amplifier amplifies the converted voltage signal, so that its voltage amplitude can reach the voltage value that the internal chip can handle. Protection devices used in the input port and output port are the dual direction ESD devices designed in this study. The traditional gate-to-drain PMOS (GDPMOS) device is used for ESD protection

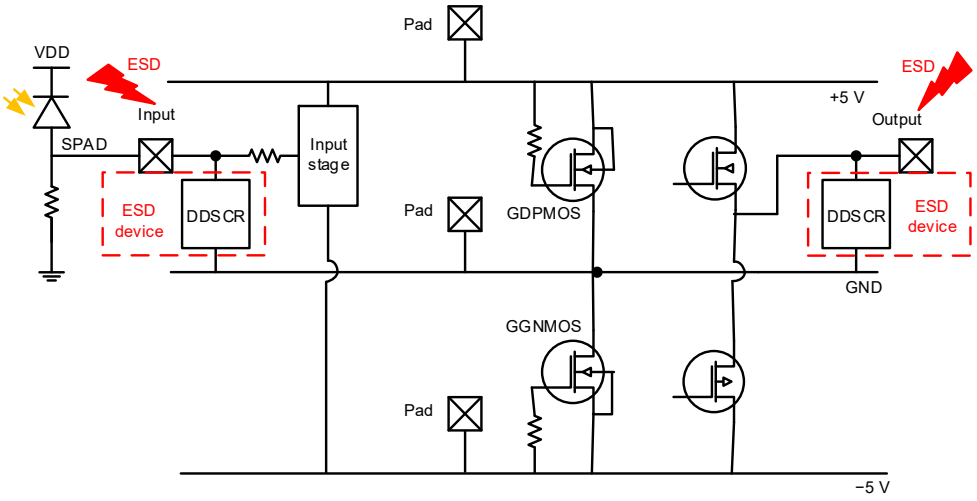


**Fig. 1 Electro-static discharge (ESD) application circuit**

between the +5 V power rail and ground, and the traditional grounded-gate NMOS (GGNMOS) device is used for ESD protection between the −5 V power rail and ground. The protection level of traditional ESD devices is 4 kV. For the ESD window requirements of the circuit input port and output port, two types of SCR structure are compared. The core idea of device design is using the electric field effect to improve the carrier transportation of the SCR based on the gate-controlled principle (Wang et al., 2019). The first type of basic device uses a heavily doped N-type buried layer as the main conduction path, NBL gate-controlled SCR (NBL-GCSCR), and the device has a high holding voltage. Because of the presence of the NBL, it is difficult for the device to turn on the SCR path in a short time. Therefore, the device operates in the bipolar junction transistor (BJT) mode at a lower failure level, and it is difficult to meet the ESD window of the application circuit. The second type of optimized device uses a deep N-well structure (DNW-GCSCR) with a conduction path that is a lateral SCR path approaching the surface of the device. This provides the device with a higher failure current and a lower holding voltage. By analyzing the physical structure of the electrostatic discharge device, and the relationship between the conductive path and the electrostatic discharge parameters, it can be seen that the holding voltage and failure current of the SCR device affect each other. Experimental and comparative analyses show that when the gate size (D4) of DNW-GCSCR is optimized to 6 μm, the test index of the device meets the ESD window requirements of the readout circuit of industry-level fluorescent optical fiber temperature sensors. This can ensure the reliability of the sensor in a harsh environment with strong electrostatic interference.

## 2 Structure and equivalent circuit of SCR devices

For the ESD window requirements of an industry-level fluorescent optical fiber temperature sensor, based on the proposed gate-controlled principle, two types of DDSCR structure are designed. The principle of gate control is shown in Fig. 2. When the ESD stress triggers the device, the NBL or DNW region inside the device is at an intermediate potential relative to the anode and cathode. The anode composed of P+, N+, and P-well on the right has a higher potential than the N-type region. From the same principle, the cathode composed of P+, N+, and P-well on the left has a lower potential than the N-type region. Therefore, the gate of the anode generates a vertical downward electric field force to adjust the movement of carriers in the anode P-well and N-type regions, thereby promoting the ESD current from the anode into the N-type region. Similarly, the gate of the cathode generates a vertical upward electric field force to adjust the movement of carriers in the N-type region and the cathode P-well, thereby promoting the ESD current from the N-type region to the cathode. For NBL-GCSCR, the N-type region is represented as NBL. For DNW-GCSCR, the N-type

region is represented as DN-well. Since the direction of the electric field force is always consistent with the direction of current discharge, the purpose of promoting carrier release is achieved and the ESD parameters of the device can be improved. The cross section of a basic NBL-GCSCR device with bidirectional release capability is shown in Fig. 3. The device uses the avalanche breakdown of the reverse biased PN junction of P-well, P-EPI, and N-well to turn on the internal parasitic path. NBL and DN-well are used to prevent external noise carriers from affecting the characteristics of the device. Similarly, the cross section of the optimized DNW-GCSCR device with bidirectional release capability is shown in Fig. 4. It is clearly depicted that the trigger surface of the deep well device consists of P-well, DN-well, and N-well. Therefore, compared to NBL-GCSCR devices, there is a certain difference in their trigger voltage. It can be clearly seen from the cross section that NBL-GCSCR has a high concentration of N-type buried layers inside, and that the current main path of the device is concentrated in the NBL. The current path of DNW-GCSCR approaches the surface of the device and gradually releases ESD stress from the inside of the device.

Both types of device structure turn on the internal parasitic low-resistance path by avalanche breakdown of the trigger surface. In NBL-GCSCR, the parasitic resistance of P-well is $R_{P1}$, and the parasitic resistance of NBL is $R_{N1}$. In DNW-GCSCR, the parasitic resistance of P-well is $R_{P2}$, and the parasitic resistance of N-well is $R_{N2}$. The $R_P$ and $R_N$ of two devices are both located in the region of the parasitic NPN and PNP base regions of the SCR device. When the avalanche carrier creates a voltage drop across the well resistor, the parasitic PNP and NPN transistors are gradually turned on. With a similar latch-up effect, a low-resistance PNPN path is quickly formed under the positive feedback mechanism to release the ESD current stress. Based on the difference of the conduction paths of two types of device structure, the influence of the longitudinal path and lateral path on the ESD parameters is analyzed. The ideal equivalent circuit of the NBL-GCSCR device is shown in Fig. 5a. The high concentration of NBL constitutes the collector region of the parasitic NPN transistor inside the device and the base region of the parasitic PNP transistor. Because of the presence of high concentration and low resistance NBL, the SCR path of the device consists of anode P+, anode P-well, NBL, cathode P-well, and cathode N+. The ideal equivalent circuit of the DNW-GCSCR device is shown in Fig. 5b. The DN-well encapsulates the entire device structure. The N-well constitutes the collector region of the parasitic NPN transistor inside the device and the base region of the parasitic PNP transistor. A PNPN path consists of an anode P+, an anode P-well, an N-well, a cathode P-well, and a cathode N+. In addition, the surface path of DNW-GCSCR is significantly affected by the gate electric field effect, so that the ESD stress is uniformly released inside the device under the action of the electric field. Because of the existence of the main path in NBL-GCSCR, the electric field effect of the gate can only regulate the carrier movement in a

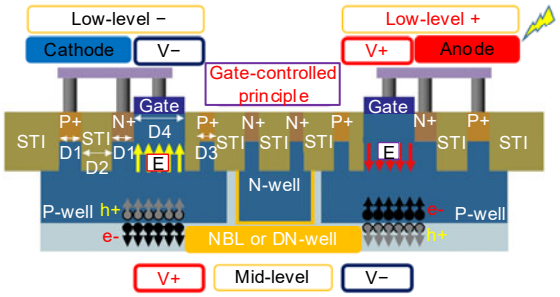


**Fig. 2 Schematic of the gate-controlled principle**

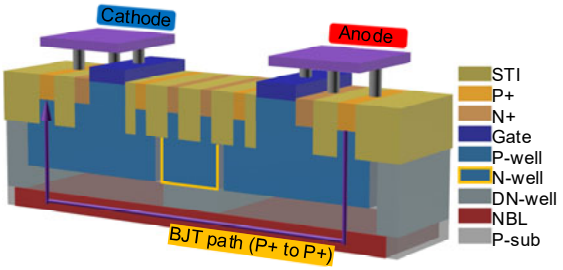


**Fig. 3 Cross section of basic NBL-GCSCR**

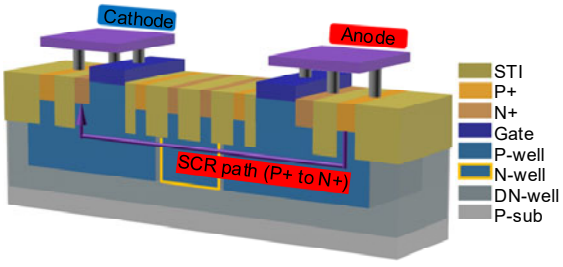


**Fig. 4 Cross section of optimized DNW-GCSCR**

part of the P-well and NBL region, and it is difficult to affect the release path of the device. The length of the conduction path of NBL-GCSCR is significantly larger than that of DNW-GCSCR, and this can directly affect the ESD index of the device. Therefore, the holding voltage of NBL-GCSCR will be significantly higher than that of DNW-GCSCR, but the failure current of NBL-GCSCR will be lower than that of DNW-GCSCR.

In the case of actual testing, NBL-GCSCR is fabricated based on the 0.18 μm bipolar-CMOS-DMOS (BCD) process. Since the junction depth of the buried layer NBL of the device is deep, the electric field effect cannot affect the conduction path of the device. It is difficult for the device to quickly turn on the SCR path in a short time. When the ESD pulse comes, the avalanche carrier can only turn on a BJT within a few nanoseconds, releasing the ESD pulse stress. NBL-GCSCR devices have limited magnifications in the BJT mode, and it is difficult to release more ESD stress, resulting in a lower failure level of the device. Because the lateral SCR path of DNW-GCSCR is close to the device surface, when ESD stress reaches the device anode, the PNPN path of DNW-GCSCR can be opened directly. Because of the significant positive feedback effect of two BJTs, the magnification of the device increases significantly. As a result, the device is able to release more carrier stress and the failure level is significantly improved. Also, there are two conduction paths for the DNW-GCSCR device. The BJT path and SCR path together release the ESD current stress. The actual forward conduction paths of the NBL-GCSCR device and DNW-GCSCR device are shown in Figs. 6a and 6b, respectively. The blue path is the BJT path, and the red path is the SCR path.

## 3 DC simulation and TLP simulation of SCR devices

### 3.1 DC simulation

Both types of device structure use Silvaco's atlas for two-dimensional DC simulation of the device to obtain various ESD parameters of the device. Technology computer-aided design (TCAD) is used to perform a DC scan of the device. The initial scan point and the progressive step size are set and the DC simulation results of the device are obtained when the current scan is stopped to 1 mA. Fig. 7 shows the impact ionization distribution of two types of device structure. It can be clearly seen that the peak impact ionization regions of NBL-GCSCR and DNW-GCSCR are between the P-well and the N-well. When the two types of device are fully turned on, the ESD stress is released from the low-resistance path, as shown in Fig. 8. The main conduction path of NBL-GCSCR has a higher current density in the NBL region. The SCR path of DNW-GCSCR will gradually replace the PNP path as the primary ESD release path. TCAD simulation cannot quantitatively describe the working behavior of the device, but it can predict and analyze the working modes of two types of device in

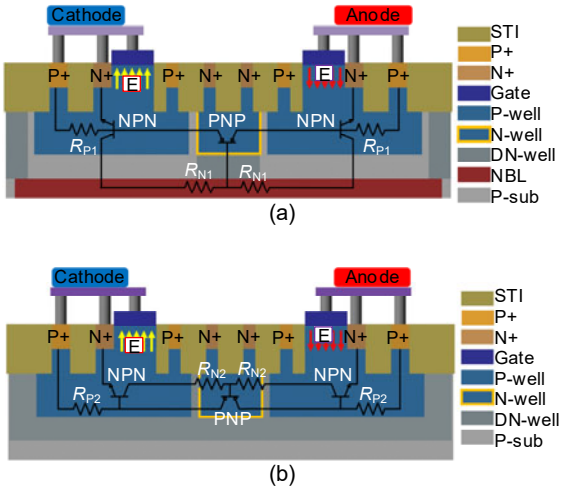


**Fig. 5 The basic NBL-GCSCR ideal equivalent circuit (a) and optimized DNW-GCSCR ideal equivalent circuit (b)**

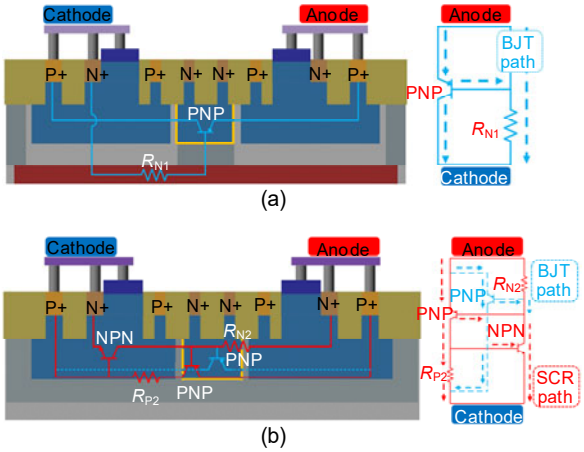


**Fig. 6 The basic NBL-GCSCR actual equivalent circuit (a) and optimized DNW-GCSCR actual equivalent circuit (b)**
References to color refer to the online version of this figure

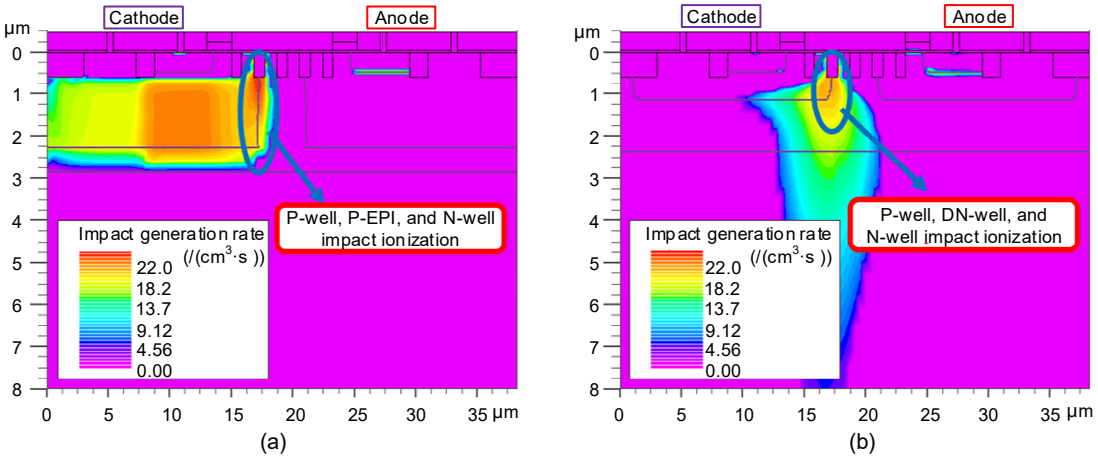


**Fig. 7 Impact ionization of NBL-GCSCR (a) and DNW-GCSCR (b)**

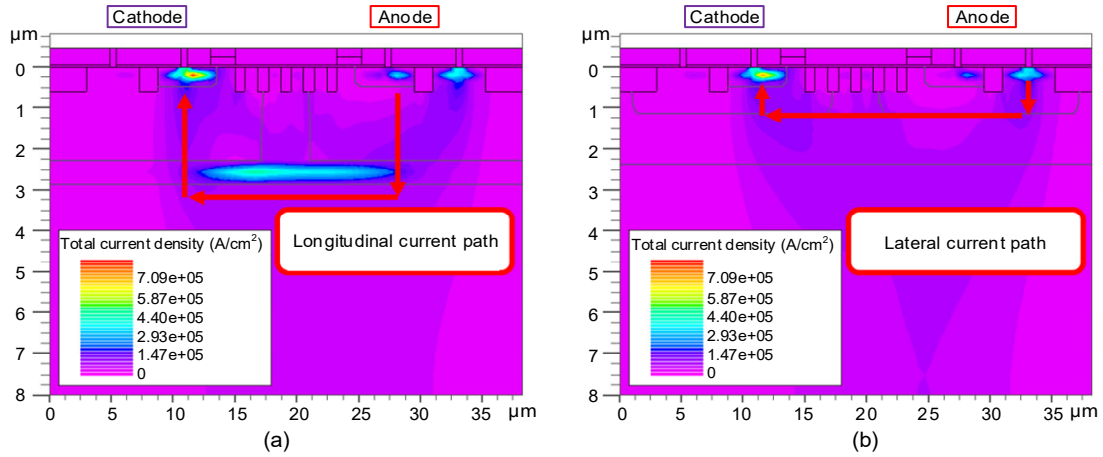


**Fig. 8 The SCR paths when NBL-GCSCR (a) or DNW-GCSCR (b) is fully turned on**

combination with the simulation results and principles. The simulation results show that both types of device structure can open the SCR path. Since the simulation parameters cannot fully match the actual process parameters, there is deviation in the comparison of the ESD parameters of the actually manufactured device from the simulation results of TCAD. As shown in Fig. 9, there is a high-density electric field distribution under the gate of the anode for both types of device structure, and the peak electric field distribution of DNW-GCSCR is higher than that of NBL-GCSCR. Fig. 10 shows the electron current distribution and hole current distribution of the two types of device structure, respectively. The electron current flows from the anode N+ to the cathode N+, and the hole current flows from the anode P+ to the cathode P+. The electron current in NBL-GCSCR is concentrated in the NBL region, but the hole current in DNW-GCSCR has a deeper release path than that in NBL-GCSCR. Moreover, because the gate of the anode of the device generates a vertical downward electric field force, the ESD current is promoted to enter the NBL or DN-well under the action of the electric field force. Therefore, no matter the electron current or the hole current, there is no obvious current density distribution under the anode gate. The lattice temperature after NBL-GCSCR or DNW-GCSCR is fully turned on is shown in Figs. 11a and 11b, respectively. The peak of the lattice temperature of NBL-GCSCR is located in the N-well, and the peak of the lattice temperature of DNW-GCSCR is located in the P-well of the anode. Moreover, the hot spot of DNW-GCSCR is obviously lower than that of NBL-GCSCR. When the device is fully turned on, the probability of thermal breakdown of DNW-GCSCR is lower than that of NBL-GCSCR, and thus the failure level of DNW-GCSCR is higher than that of NBL-GCSCR.

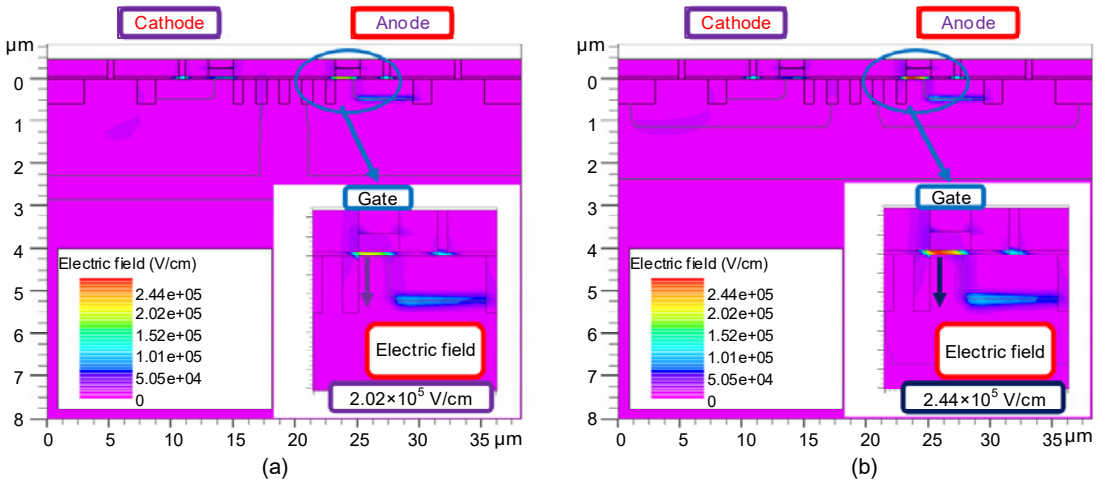


**Fig. 9 The electric field distribution when NBL-GCSCR (a) or DNW-GCSCR (b) is fully turned on**

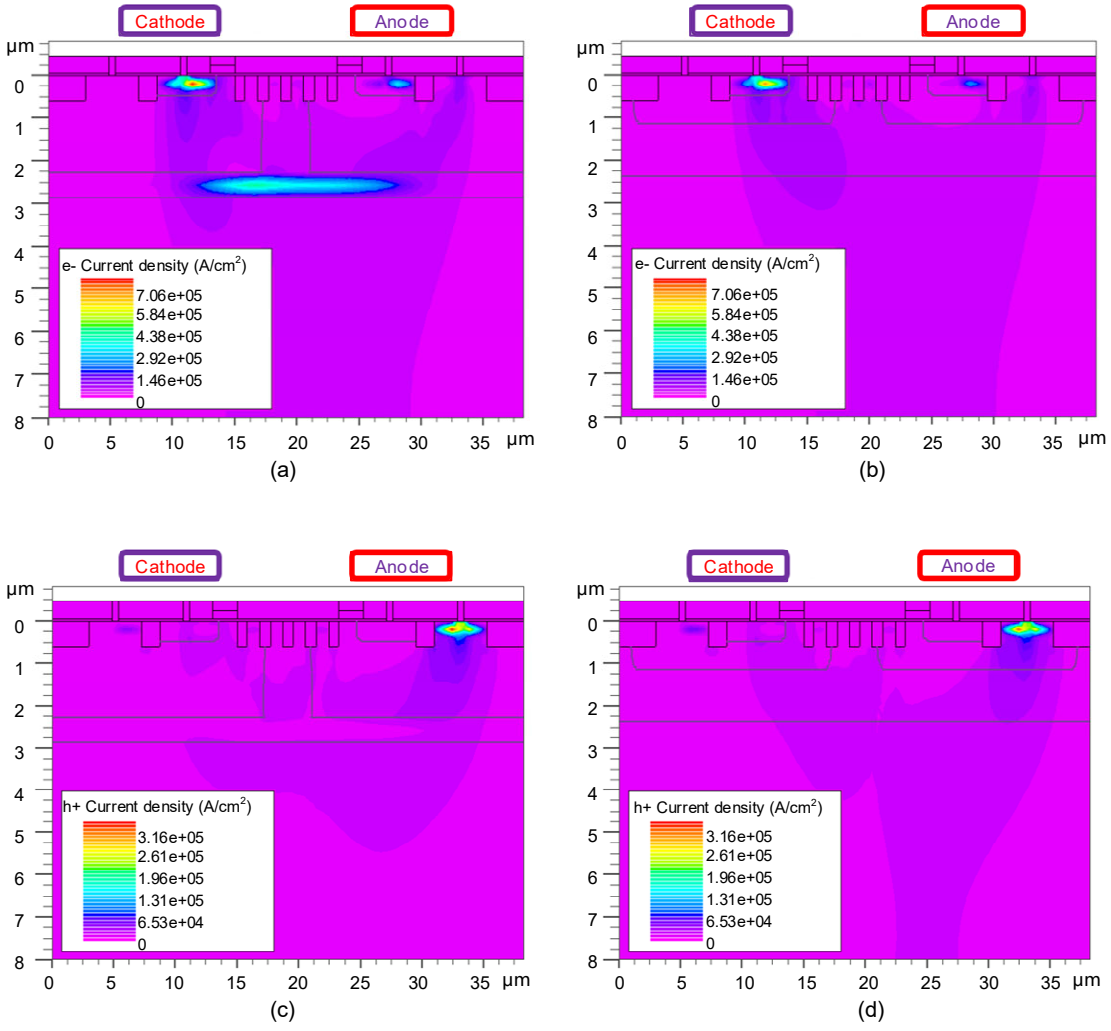


**Fig. 10 The electron current density distribution when NBL-GCSCR (a) or DNW-GCSCR (b) is fully turned on and the hole current density distribution when NBL-GCSCR (c) or DNW-GCSCR (d) is fully turned on**

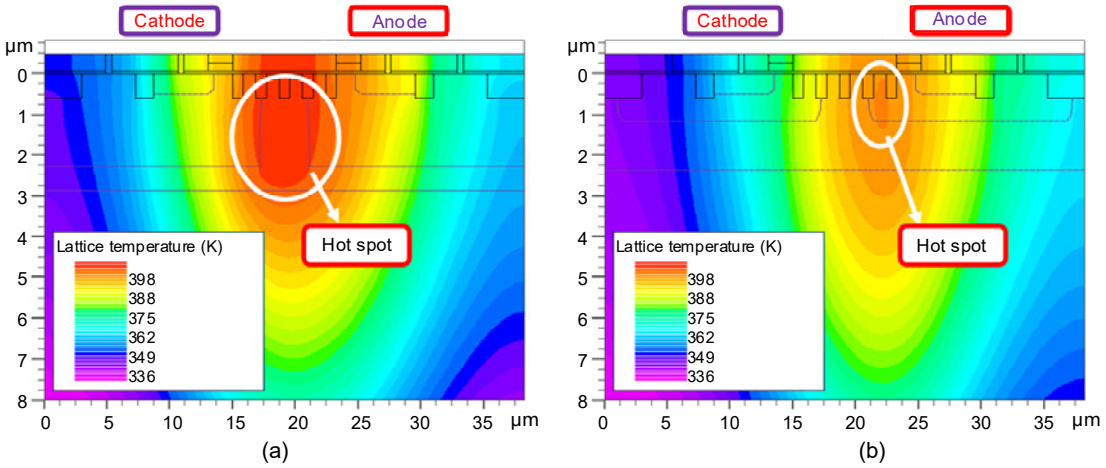


**Fig. 11 The lattice temperature when NBL-GCSCR (a) or DNW-GCSCR (b) is fully turned on**

### 3.2 TLP simulation

To further verify the ESD principle of the device, TLP simulation is used to analyze its ESD behavior. A simulation of the global device temperature and time ($2.0\times10^{-14}$–$1.2\times10^{-7}$ s) for both types of device at a transient current of 10 mA is shown in Fig. 12. The temperature of the DNW-GCSCR device is significantly lower than that of the NBL-GCSCR device. This means that when the device is triggered, the thermal breakdown probability of DNW-GCSCR is lower than that of NBL-GCSCR. DNW-GCSCR has a lateral SCR path that is easy to open, so it can release more ESD current in a short time. NBL-GCSCR has a buried layer with high concentration, and the ESD current is concentrated in the NBL region. The main release path when NBL-GCSCR is initially turned on is the PNP path. It is difficult for the BJT path to release more ESD current in a short time. The accumulation of carriers will increase the internal temperature of the device. This increases the possibility of thermal breakdown on the surface of the device. The clamp-points of the two types of device can be clearly found in the transient simulation. The clamp-time of NBL-GCSCR is 21.4 ns, and the clamp-time of DNW-GCSCR is 3.67 ns. Fig. 13 shows the electric field distribution at the clamp-time of the two devices. The simulation results are consistent with the DC simulation results. The electric field distribution density of DNW-GCSCR is higher than that of NBL-GCSCR. Fig. 14 shows the current density distribution at the clamp-time of the two types of device. TLP simulation results are similar to those of the DC simulation. There is no significant current density distribution below the anode gate.

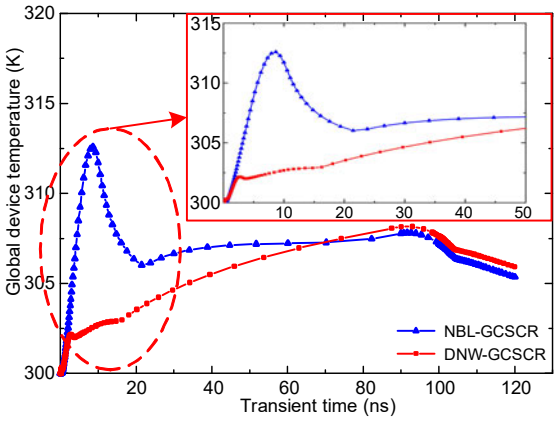


**Fig. 12 Simulated global device temperature curves for NBL-GCSCR and DNW-GCSCR in the ESD current discharging process (transient current: 10 mA)**

## 4 Experiment and analysis of SCR devices

Based on the proposed gate-controlled principle, the 8-finger basic NBL-GCSCR device and 8-finger optimized DNW-GCSCR device are both fabricated using a 0.18 μm BCD process. A microscope image of the devices is shown in Fig. 15. Both types of device have a finger length of 50 μm and have exactly the same size information. The SCR devices have the D1 size of 4.28 μm, the D2 size of 1.46 μm, the D3 size of 1 μm, and the D4 size of 4 μm. Devices have passed the thermo-scientific-celestron transmission line pulses (TSC-TLP) test, using a current pulse with a

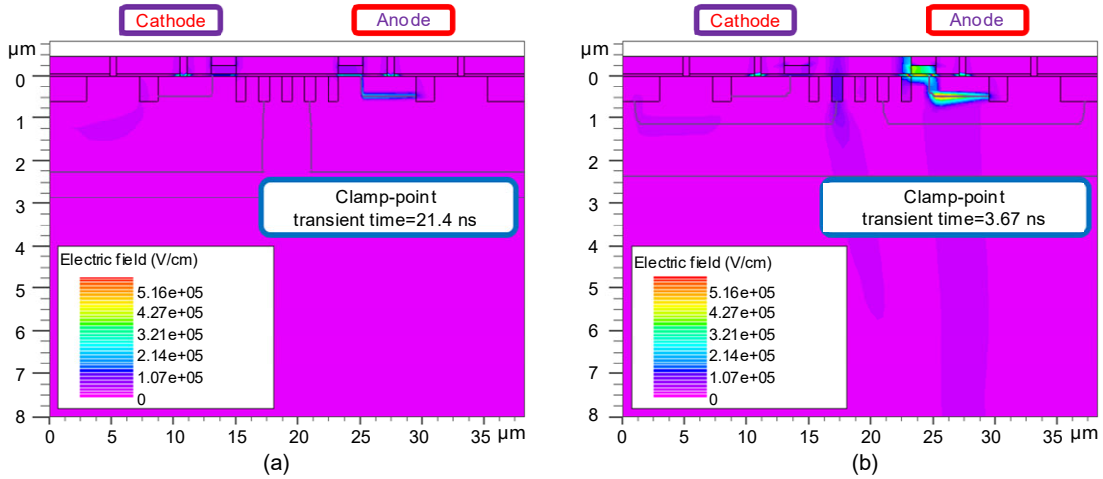


**Fig. 13 The electric field distribution of the NBL-GCSCR clamp-point (a) or DNW-GCSCR clamp-point (b)**

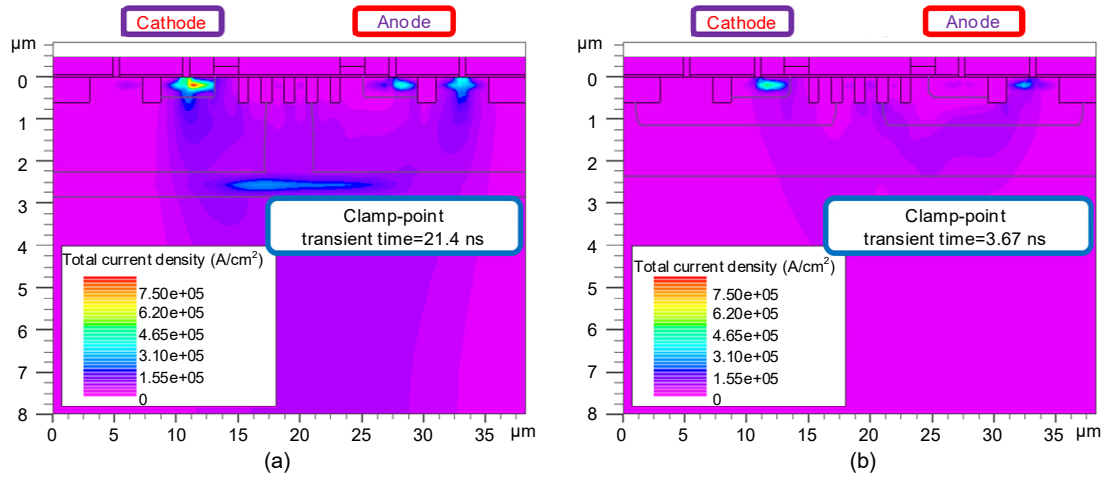


**Fig. 14 The current density distribution of the NBL-GCSCR clamp-point (a) and the DNW-GCSCR clamp-point (b)**

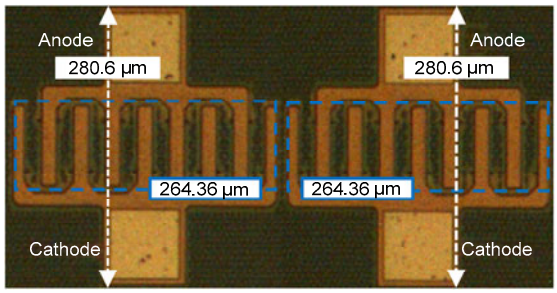


**Fig. 15 Microscope image of basic NBL-GCSCR and optimized DNW-GCSCR**

rise time of 10 ns and a width of 100 ns to detect ESD parameters. The overshoot curve, DC curve, trigger voltage, holding voltage, and failure current of the devices are acquired from the TLP.

First, the DC characteristics of the two types of SCR device are obtained through the TLP test system, and the curves are shown in Fig. 16. The BV of NBL-GCSCR is 20 V, and the BV of DNW-GCSCR is 18 V. It shows that DNW-GCSCR can maintain good transparency under the voltage of 18 V, and will not generate leakage current drift in advance. Since the BV of the device is higher than the normal working voltage (−5–5 V) of the industry- level fluorescent optical fiber temperature sensor readout circuit, when the system is working normally, the SCR device will not affect the integrity of the circuit's signal transmission.

Second, the voltage-time and current-time curves of the two types of device are shown in Fig. 17. The NBL-GCSCR and DNW-GCSCR breakdown points have the same time (7.8 ns). The 70–90 ns time in the test curve is chosen to estimate the clamp-voltage and clamp-current of the device. NBL-GCSCR has a clamp-voltage of 23.85 V and a

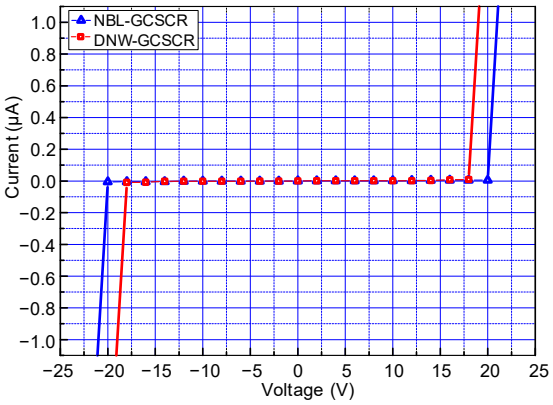


**Fig. 16 DC *I-V* curves of 8-finger basic NBL-GCSCR and optimized DNW-GCSCR**

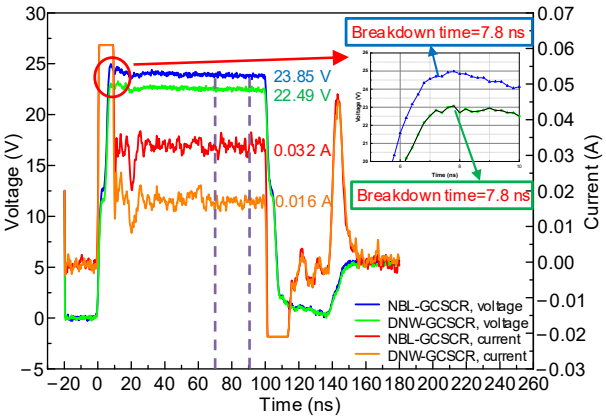


**Fig. 17 Response time and turn-on time curves of 8-finger basic NBL-GCSCR and optimized DNW-GCSCR**

clamp-current of 0.032 A. The clamp-voltage of DNW-GCSCR is 22.49 V and the clamp-current is 0.016 A. It can be concluded from the test results that the transient voltage clamping capabilities of the NBL-GCSCR device and DNW-GCSCR device are the same. When the ESD current stress comes to the device anode, the voltage can be clamped below 24 V instantly. The transient clamp-voltage of this type of device is much lower than the minimum gate oxide BV (30 V) of the circuit, thus ensuring the effectiveness of the on-chip SCR device.

Fig. 18 shows the forward TLP test curves for the same size of the two types of device. The trigger voltage ($V_{t1}$) of NBL-GCSCR is 24.22 V. The holding voltage ($V_h$) is 24.03 V, and the failure current ($I_{t2}$) is 1.71 A. The trigger voltage ($V_{t1}$) of DNW-GCSCR is 22.48 V. The holding voltage ($V_h$) is 5.15 V, and the failure current ($I_{t2}$) is 20.99 A. The test results show that the two types of SCR device cannot meet the ESD window requirements of the industry-level

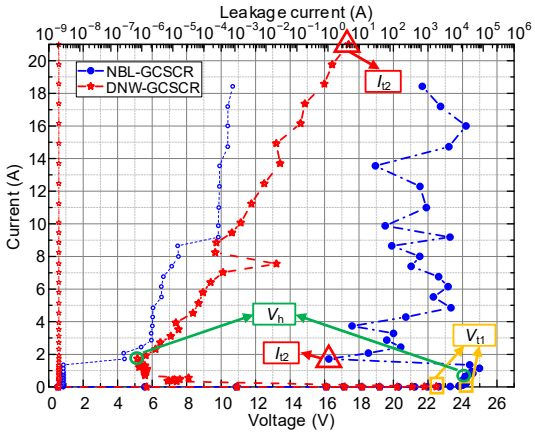


**Fig. 18 TLP *I-V* curves of 8-finger basic NBL-GCSCR and optimized DNW-GCSCR**

fluorescent optical fiber temperature sensor readout circuit. Moreover, there is a 4 V deviation in the avalanche BV of the two types of device between the TLP test results and DC test results. The reason is that, when the trigger surface of the two types of device is broken down by impulse stress, it is difficult for the current generated to reach the turn-on current of the ESD release path. As the voltage continues to increase, the low-resistance ESD path opens, and the device begins to release the ESD pulse stress. It is apparent from the data that the holding voltage of device is significantly higher than that of the lateral SCR path due to the longer ESD release distance of the longitudinal BJT path. The deep snapback characteristic of SCR is also a major factor in the low holding voltage of the DNW-GCSCR device. However, the holding voltage and failure current are mutually influential, and the failure current of the lateral SCR path is significantly higher than that of the longitudinal BJT path. In NBL-GCSCR, since the main path is located in the N-type buried layer of the device and the junction depth of the buried layer is deep, the avalanche carriers cannot easily turn on parasitic PNP and NPN paths. In the TLP curve, NBL-GCSCR has multiple snapbacks after triggering. That is, after the BJT path is quickly turned on, the SCR path cannot be turned on in a very short time. Moreover, when the NBL-GCSCR device generates a deep snapback, it indicates that the SCR path of the device has gradually turned on under the action of a large current. However, as the current increases, the BJT mode cannot maintain the steady state of the ESD release path. While the SCR path is turned on, the

NBL-GCSCR device has generated a leakage drift. In DNW-GCSCR, the lateral SCR path of the surface is easily turned on, and the device forms a low-resistance SCR path immediately after the avalanche breakdown. Due to the small release length of the surface path, the holding voltage of the device is low. However, the linearity of the device after reaching the holding point is good, indicating that the SCR path can stably release the ESD current stress, so that the failure current of DNW-GCSCR can be significantly higher than that of NBL-GCSCR. Due to the trigger voltage and failure current of NBL-GCSCR, it is difficult to meet the ESD window of the application circuit. The trigger voltage of DNW-GCSCR is between 6 V and 24 V, and the failure level meets the index requirements of the ESD window. To enable DNW-GCSCR to be applied stably to the on-chip ESD protection of the target readout circuit, it is necessary to further improve the holding voltage of DNW-GCSCR. Since the electric field effect generated by the short-circuited polysilicon gate significantly affects the ESD parameters of DNW-GCSCR, the gate size (D4) is set to 2 μm and 6 μm, as shown in Fig. 19. The positive and negative TLP curves of the three different gate lengths of DNW-GCSCR show good symmetry. When D4 is 2 μm, the trigger voltage of the device is 22.22 V. The holding voltage is 3.50 V and the failure current is 34.14 A. When D4 is 6 μm, the trigger voltage of the device is kept at almost 22 V. The holding voltage obviously increases to 8.38 V and the failure current is 25.68 A. The size change of 4 μm can make the holding voltage of the DNW- GCSCR device produce a 5 V change, which proves that the D4 size is one of the main factors affecting the holding voltage of the device. The trigger voltage, holding voltage, and failure level of DNW-GCSCR (gate=6 μm) meet the ESD window requirements of the industry-level fluorescent optical fiber temperature sensor readout circuit. The HBM level of the device can be calculated using Eq. (1):

$$\mathrm{HBM} = I_{t2} \cdot R_{\mathrm{HR}(1.5\,\mathrm{k\Omega})}. \tag{1}$$

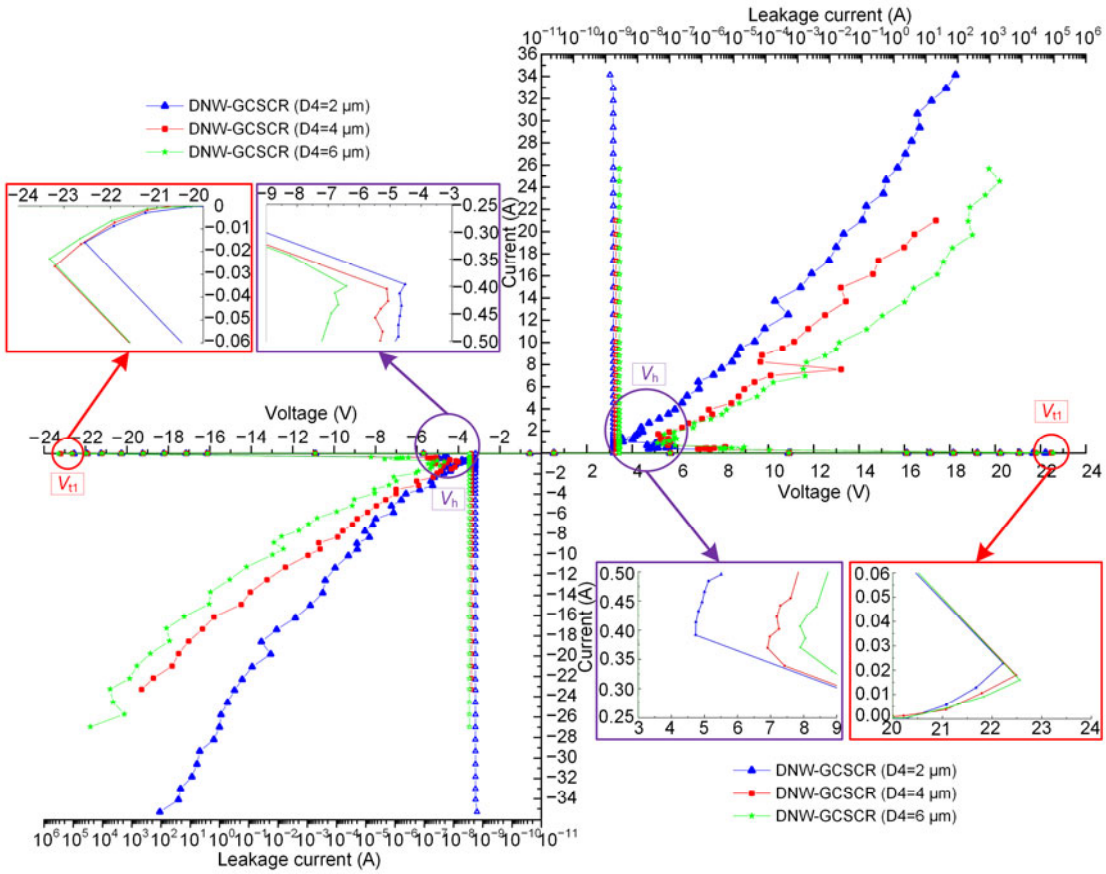


**Fig. 19 TLP *I-V* curves of 8-finger optimized DNW-GCSCR (D4=2, 4, 6 μm)**

The result shows that $HBM_{DNW\text{-}GCSCR(6\ \mu m)}$ is 38.52 kV. The ESD characteristics of forward and reverse meet the requirements. When the HBM level of the DNW-GCSCR device (gate=6 μm) is greater than 30 kV, the reliability of the chip can be guaranteed in harsh environments.

It can be found that as the size of D4 increases, the holding voltage of DNW-GCSCR increases significantly. First, due to the increase in the D4 size, the length of the lateral current path between the anode and cathode of the device increases, causing the holding voltage of the device to increase. In the longitudinal current path of the device, since the increase in the gate size (D4) leads to a larger range of electric field effects, more ESD stress is released inside the device with the help of electric field forces. This results in an increase in the length of the longitudinal current release path of DNW-GCSCR, which further increases the holding voltage. The TLP test cannot accurately describe the failure behavior of the device under high current conditions. Therefore, the failure currents of the three sizes of DNW-GCSCR are different, but the failure current of the device can be maintained above 20 A. When D4 is 6 μm, the DNW-GCSCR device can be stably applied to the on-chip ESD protection of the target readout circuit. The figure of merit (FOM) of two types of SCR device is calculated using Eq. (2):

$$\mathrm{FOM}=\frac{I_{t2}\cdot V_{h}}{N\cdot W\cdot V_{t1}}, \tag{2}$$

where $N$ is the number of fingers and $W$ is the width of the fingers. When the gate size (D4) is 4 μm, $FOM_{NBL\text{-}GCSCR}$ is 0.0004, and $FOM_{DNW\text{-}GCSCR}$ is 0.012. When the gate size (D4) is 6 μm, $FOM_{DNW\text{-}GCSCR}$ is 0.024. The results show that the DNW-GCSCR (gate=6 μm) device has better robustness than the DNW-GCSCR (gate=4 μm) device.

The test data of the ESD performance of SCR devices with different application backgrounds is shown in Table 1. The test data of DNW-GCSCR at different D4 sizes is shown in Table 2. By optimizing the size of DNW-GCSCR, the holding voltage of the device can be significantly increased and the failure current is not significantly reduced. When the DNW-GCSCR (gate=6 μm) device is used for on-chip ESD protection of the industry-level fluorescent optical fiber temperature sensor readout circuit, it can ensure a stable operation of the system without affecting the integrity of circuit signal transmission.

## 5 Conclusions

In this paper, we consider the ESD window of the industry-level fluorescent optical fiber temperature sensor readout circuit. The relationship among the physical structure, conduction path, and ESD parameters of the ESD device is studied based on a proposed gate-controlled principle. Two types of ESD device are analyzed and verified. They are manufactured using the 0.18 μm BCD process. The results of two-dimensional simulation and a TLP test show that the electric field effect of the gate significantly affects the ESD parameters of the device. The longitudinal BJT path of the basic NBL-GCSCR device will produce a higher holding voltage, but the failure current is lower, making it difficult to meet the on-chip ESD protection requirements of the readout circuit. The

**Table 1 Comparison of ESD performance of SCR devices**

| Device name | $V_{t1}$ (V) | $V_h$ (V) | $I_{t2}$ (A) | HBM (kV) |
|---|---|---|---|---|
| GDTSCR (Liang et al., 2019) | 16.50 | 13.60 | 3.80 | 5.70 |
| LDPMOS (Wang et al., 2015) | 33.11 | 11.74 | 4.37 | 6.56 |
| DS-SCR (Hu et al., 2018) | 6.00 | 4.90/4.30 | 0.53 | 0.80 |
| NBL-GCSCR (D4=4 μm) | 24.22 | 24.03 | 1.71 | 2.56 |
| DNW-GCSCR (D4=4 μm) | 22.48 | 5.15 | 20.99 | 34.48 |

**Table 2 Test results of DNW-GCSCR devices at different D4 sizes***

| D4 size | $V_{t1}$ (V) | $V_h$ (V) | $I_{t2}$ (A) | HBM (kV) |
|---|---|---|---|---|
| 2 μm | 22.22 (F)/22.54 (R) | 3.50 (F)/3.78 (R) | 34.14 (F)/35.32 (R) | 51.21 (F)/52.98 (R) |
| 6 μm | 22.22 (F)/23.30 (R) | 8.38 (F)/8.21 (R) | 25.68 (F)/26.96 (R) | 38.52 (F)/40.44 (R) |

*8-finger, with the finger length being 50 μm. F: forward test; R: reverse test

lateral SCR path of the optimized DNW-GCSCR device will generate a higher failure current, but the gate size (D4) needs to be increased to increase the holding voltage. When D4 is 6 μm, each ESD index of the DNW-GCSCR device meets the on-chip ESD protection window of the target readout circuit. In summary, in a harsh environment with strong electrostatic interference, the DNW-GCSCR device can provide a solution to the on-chip ESD protection of the signal readout circuit of industry-level fluorescence detection technology.

## Contributors

Yang WANG and Xiangliang JIN designed the research. Jian YANG, Feng YAN, and Yujie LIU processed the data. Yang WANG drafted the paper. Xiangliang JIN helped organize the paper. Yan PENG, Jun LUO, and Jun YANG revised and finalized the paper.

## Compliance with ethics guidelines

Yang WANG, Xiangliang JIN, Jian YANG, Feng YAN, Yujie LIU, Yan PENG, Jun LUO, and Jun YANG declare that they have no conflict of interest.

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