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A 9.8–30.1 GHz CMOS low-noise amplifier with a 3.2-dB noise figure using inductor- and transformer-based g_m-boosting techniques*

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Abstract: A 9.8–30.1 GHz CMOS low-noise amplifier (LNA) with a 3.2-dB minimum noise figure (NF) is presented. At the architecture level, a topology based on common-gate (CG) cascading with a common-source (CS) amplifier is proposed for simultaneous wideband input matching and relatively high gain. At the circuit level, multiple techniques are proposed to improve LNA performance. First, in the CG stage, loading effect is properly used instead of the conventional feedback technique, to enable simultaneous impedance and noise matching. Second, based on in-depth theoretical analysis, the inductor- and transformer-based g_m-boosting techniques are employed for the CG and CS stages, respectively, to enhance the gain and reduce power consumption. Third, the floating-body method, which was originally proposed to lower NF in CS amplifiers, is adopted in the CG stage to further reduce NF. Fabricated in a 65-nm CMOS technology, the LNA chip occupies an area of only 0.2 mm^2 and measures a maximum power gain of 10.9 dB with −3 dB bandwidth from 9.8 to 30.1 GHz. The NF exhibits a minimum value of 3.2 dB at 15 GHz and is below 5.7 dB across the entire bandwidth. The LNA consumes 15.6 mW from a 1.2-V supply.

Key words: CMOS; g_m-boosting; Low-noise amplifier; Transformer; Common-gate
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1 Introduction

Recent progress in the development of fifth-generation (5G) wireless communication systems has given rise to further evolution of millimeter-wave (mmWave) transceivers which are often used as the key elements in such systems. For one receiver, a signal-to-noise ratio (SNR) should be preserved throughout the signal processing chain. For this purpose, a radio frequency (RF) amplifier with a low noise figure (NF), i.e., low-noise amplifier (LNA), is therefore often the first active component after the antenna or duplexer/diplexer. Other than the common narrowband LNAs, the wideband LNAs have attracted a lot of attention due to the stimulation of multi-band, multi-standard, and ultra-wideband (UWB) radios. In addition to low NF and high fractional bandwidth, a wideband LNA should be capable of providing high gain and the modest linearity simultaneously. However, the performance of wideband LNAs is compromised due to the limited

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transistor gain-bandwidth product.

Conventionally, wideband LNAs are realized in compound semiconductor technologies (e.g., SiGe and GaAs), taking advantage of superior intrinsic frequency response and noise performance (Çaişkan et al., 2019; Qayyum et al., 2019). On the other hand, thanks to the continuous technology scaling, the unity-gain frequency (i.e., f_T) of the NMOS transistor has increased to hundreds of GHz for the latest deep submicron processes, leading to the feasibility of mmWave frequency circuits in CMOSs. Therefore, to co-integrate RF and digital baseband in a single technology and reduce costs in mass production, implementation of wideband LNAs has shifted from III-V compound semiconductors to CMOSs.

Over the past years, many techniques have been developed to enhance the bandwidth of CMOS LNAs. Two of the most representative and widely used techniques in mmWave LNAs are neutralization (Pan et al., 2019; Zhang et al., 2020) and negative feedback (Reiha and Long, 2007; Fu et al., 2010; Leung and Luong, 2012; Wu et al., 2017). In neutralized LNAs, compensating capacitors are added between the gate and drain of the two common-source (CS) transistors in a differential pair, so the currents that are fed back through the compensating capacitors can cancel the drain-gate feedback. In this way, the Miller effect is eliminated and the bandwidth is broadened accordingly. For example, Pan et al. (2019) demonstrated that a 60–90 GHz double-neutralized LNA with a 6.3-dB NF can be achieved in 65-nm CMOS. In addition to neutralization, negative feedback is a common technique for implementing wideband LNAs. By introducing a capacitive feedback and an inductive feedback, a CS LNA operating from 3 to 11 GHz with simultaneous impedance and noise matching (SINM) was reported by Fu et al. (2010). Wu et al. (2017) used a transformer as a shunt feedback from the output to the input for wideband work in another design. Implemented in 65-nm CMOS, the measured NF for the LNA was 6.8 to 9 dB over the frequency range of 55 to 65 GHz, and the maximum gain was 16.4 dB with the power consumption of 33.6 mW.

The above-mentioned designs are based on a CS amplifier, and extra neutralization/feedback components are required for bandwidth enhancement. Conversely, a pure common-gate (CG) amplifier with low input impedance is suitable for wideband implementation without any additional components, but with some disadvantages such as low gain and significant noise (Chen WL et al., 2009; Lo and Kiang, 2011; Parvizi, 2016a; Li N et al., 2017).

Therefore, in this work, an LNA is proposed to realize wideband input matching that adopts one CG stage as the first stage. To improve the noise performance, the loading effect is used and a large transconductance is achieved that exceeds the conventional input matching limit. Furthermore, a CS stage is cascaded after the CG stage for gain enhancement. In addition, the inductor- and transformer-based g_m-boosting techniques are adopted in the CG stage and CS stage, respectively, aiming to boost the gain (or reduce the power consumption).

2 SINM CG-LNA using loading effect

When building a wideband LNA, the CG configuration has intrinsic advantages due to its low input impedance characteristics. In particular, the input impedance of a CG stage can be simplified as $1/g_m$ when operating in a low frequency. Thus, in a 50-Ω system, the transconductance g_m is restricted to 20 mS for good input matching. On the other hand, the voltage gain of the CG-LNA is proportional to g_m and the NF is inversely proportional to g_m (Guan and Hajimiri, 2004). As a result, once the g_m value is restricted for input matching, the CG-LNA suffers from a low gain and high NF. To mitigate this problem, some conventional techniques based on feedback (including positive feedback and negative feedback) have been adopted, as discussed in this section.

2.1 Conventional technique for SINM in CG-LNA

As described above, to achieve a high-gain, low-NF CG-LNA, g_m should be increased, which adversely affects the input impedance matching for a conventional CG-LNA. The basic idea to improve the noise performance is to introduce a feedback mechanism to decouple the input matching condition and the NF. Fig. 1 shows three feedback-based techniques reported in the literature for SINM, including the positive feedback technique (Liscidini et al., 2006), the dual negative feedback technique (Ye et al., 2011), and the positive-negative feedback technique (Woo et al., 2012). The input impedances

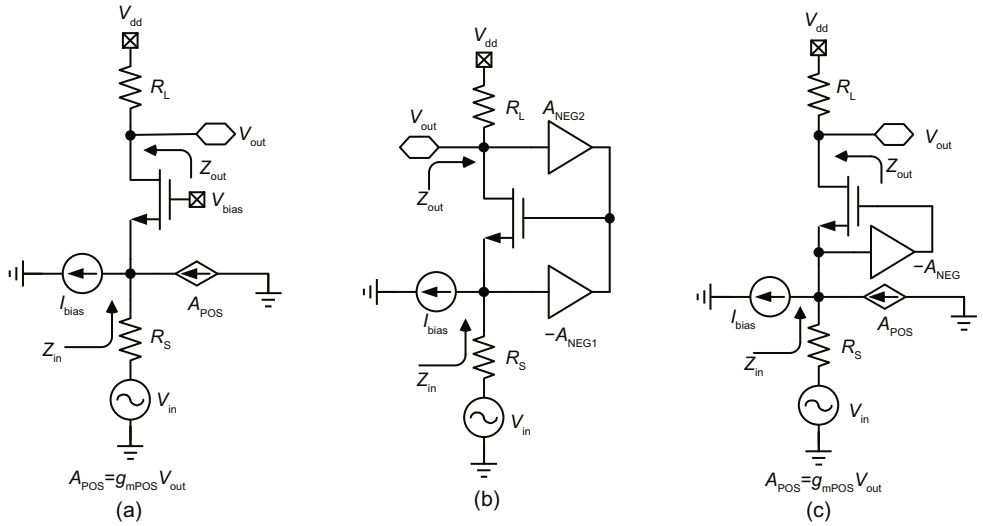

Fig. 1 Conventional techniques for SINM in CG-LNA: (a) positive feedback; (b) dual negative feedback; (c) positive-negative feedback

of these topologies are summarized in Table 1. Here, A_{POS}, A_{NEG}, A_{NEG1}, and A_{NEG2} are feedback factors. These expressions of input impedance indicate that g_{m} can be higher than 20 mS by increasing A_{POS} or A_{NEG2} in each case, while maintaining 50-Ω input matching.

Table 1 Input impedances of feedback-based CG-LNAs

Technique	Input impedance Z_{in}
Positive feedback	$\dfrac{1}{g_{\mathrm{m}}(1-A_{\mathrm{POS}})}$
Dual negative feedback	$\dfrac{1+A_{\mathrm{NEG2}}}{g_{\mathrm{m}}(1+A_{\mathrm{NEG1}})}$
Positive-negative feedback	$\dfrac{1}{g_m(1+A_{\mathrm{NEG}})(1-A_{\mathrm{POS}})}$

In the circuit design, larger transconductance, i.e., g_{m}, is desired to optimize the NF. Hence, feedback-based techniques allow the CG-LNA to have a larger g_{m} than the conventional CG-LNA. Consequently, NF would be improved because it decreases as g_{m} increases, and the SINM CG-LNA is realized.

However, the feedback-based SINM CG-LNAs realized in previous works (Liscidini et al., 2006; Ye et al., 2011; Woo et al., 2012) are suitable only for frequencies below several GHz for the following reasons: First, the parasitic capacitance at the gate-source junction is ignored, which should be resonated out by an additional source inductance to obtain pure resistive input impedance at high frequencies. Second, the loading effect is neglected. When the MOS gate length becomes shorter, the output resistance is reduced and the input matching becomes more susceptible to loading, which should be taken into account.

2.2 SINM CG-LNA using loading effect at millimeter waves

Few works have been reported involving the design of an SINM CG-LNA when the frequency rises to millimeter waves. This may be due to the fact that an active feedback used in conventional SINM CG-LNAs will introduce a certain amount of noise, and noise reduction techniques such as noise canceling do not work well at mmWave bands. To address this issue, a novel SINM CG-LNA using loading effect is proposed here. Compared with the conventional feedback-based techniques mentioned above, this method provides a solution to the problem of mmWave SINM CG-LNA design. No additional components are required for feedback in this way, so no more noise is introduced.

Fig. 2 shows the equivalent small-signal model of the CG stage, where the gate-to-source parasitic capacitance C_{gs1} and the channel resistance R_{ds1} are considered. Here, L_{s1} is the source inductance, g_{m1} is the transconductance, and Z_{in2} represents the load impedance which is also the input impedance looking into the second stage in a multi-stage architecture. Different from g_{m1} obtained at low frequencies, the

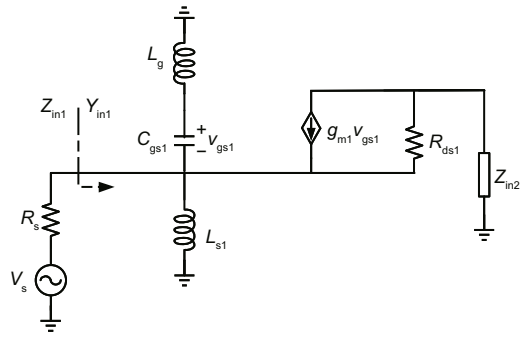

Fig. 2 Equivalent small-signal model of the CG stages

input admittance $Y_{\rm in1}$ can be derived as follows:

$$Y_{\rm in1}=\frac{1+g_{\rm m1}R_{\rm ds1}}{R_{\rm ds1}+Z_{\rm in2}}+sC_{\rm gs1}+\frac{1}{sL_{\rm s1}}. \tag{1}$$

From Eq. (1), it can be observed that the input admittance is no longer a pure conductance, and that the load impedance $Z_{\rm in2}$ affects it dramatically because the channel resistance decreases to 100–300 Ω in the 65-nm CMOS process. Assuming that $Z_{\rm in2}=R_2+{\rm j}X_2$, Eq. (1) can be rewritten as

$$\begin{aligned}Y_{\rm in1}=&\frac{(1+g_{\rm m1}R_{\rm ds1})(R_{\rm ds1}+R_2)}{(R_{\rm ds1}+R_2)^2+X_2^2}\\&-{\rm j}\frac{(1+g_{\rm m1}R_{\rm ds1})X_2}{(R_{\rm ds1}+R_2)^2+X_2^2}+sC_{\rm gs1}+\frac{1}{sL_{\rm s1}}.\end{aligned} \tag{2}$$

Clearly, the second term in the right-hand side of Eq. (2) is the imaginary part and can be resonated out with the third and fourth terms. Consequently, only the pure conductance in Eq. (2) is kept, and converting it to impedance, the real part of impedance can be given by

$${\rm Re}(Z_{\rm in1})=\frac{(R_{\rm ds1}+R_2)^2+X_2^2}{(1+g_{\rm m1}R_{\rm ds1})(R_{\rm ds1}+R_2)}. \tag{3}$$

As indicated by Eq. (3), a relatively large transconductance $g_{\rm m1}$ is available by adjusting the load impedance $Z_{\rm in2}=R_2+{\rm j}X_2$ while keeping the input matching ${\rm Re}(Z_{\rm in1})=50\ \Omega$ unchanged. Therefore, using the loading effect, an SINM CG-LNA can be accomplished without introducing extra feedback components.

To observe the loading effect more intuitively, Fig. 3 shows the variation of input impedance ${\rm Re}[Z_{\rm in1}]$ with load impedance $Z_{\rm in2}$, where both the real and imaginary parts of $Z_{\rm in2}$ are included. Here, a $g_{\rm m1}$ of 40 mS instead of 20 mS is selected to lower the noise. In addition, it should be noted that a larger $g_{\rm m1}$ can be used to further improve the NF, which depends on the load impedance and increases the power consumption. Thus, Fig. 3 demonstrates that with the changing of ${\rm Re}[Z_{\rm in2}]$ and ${\rm Im}\,[Z_{\rm in2}]$, the desired input impedance close to 50 Ω can be realized when $g_{\rm m1}$ is as high as 40 mS, to minimize the NF; i.e., an SINM CG-LNA is achieved accordingly.

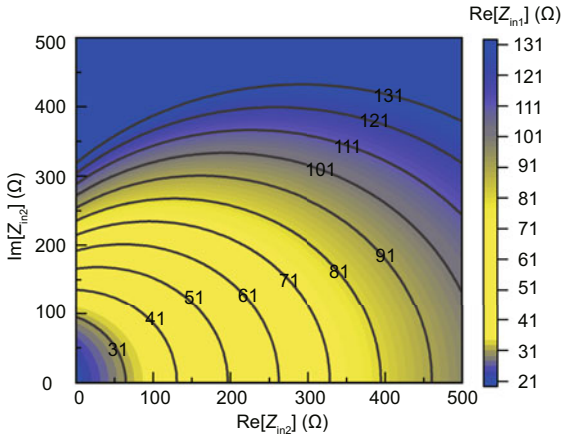

Fig. 3 Correspondence from $Z_{\rm in2}$ to input resistance ${\rm Re}[Z_{\rm in1}]$ via the loading effect ($g_{\rm m1}=40$ mS and $R_{\rm ds1}=140\ \Omega$ are assumed)

3 Inductor- and transformer-based $g_{\rm m}$-boosting

A common way to enhance the gain of an LNA is to cascade multiple amplifiers at the cost of higher power consumption. Conversely, the $g_{\rm m}$-boosting technique can alleviate such a tradeoff, leading to an LNA design with high gain and relatively low power consumption (Chen HC et al., 2019). Thus, the $g_{\rm m}$-boosting techniques (including inductor- and transformer-based $g_{\rm m}$-boosting techniques) are discussed in this section.

3.1 Benefits of the $g_{\rm m}$-boosting technique

The $g_{\rm m}$-boosting technique is a well-known method in designing a high-gain and low-NF LNA, despite the low intrinsic $g_{\rm m}$ of the MOS transistors. In practice, a higher $g_{\rm m}$ always implies a wider transistor gate width and would cause higher power consumption. Thus, by adopting the $g_{\rm m}$-boosting technique, tradeoff between power consumption and gain is alleviated. For demonstration, CG-LNAs with and without the $g_{\rm m}$-boosting technique are compared in Table 2, where $g_{\rm m}$ is the intrinsic transconductance of

the MOS transistor and G_m is the effective transconductance. Herein, a perfect input matching is assumed and thus the value of g_m will not be restricted for input matching. Table 2 indicates that for the same g_m, i.e., the same power consumption, a CG-LNA with g_m-boosting has higher G_m and higher gain. In contrast, when G_m is kept constant, i.e., for the same gain, only a smaller g_m is needed in a CG-LNA with g_m-boosting, hence less power consumption.

Table 2 Comparison of a CG-LNA with and without g_m-boosting

	Without g_m-boosting	With g_m-boosting
	G_m=g_m	G_m=$(1+A)g_m$
Fixed g_m	Small G_m	Large G_m
Fixed G_m	Large g_m	Small g_m

A is the boost factor

However, in the mmWave band, noise issues prohibit active realizations of the inverting gain loop in the g_m-boosting technique (Kim et al., 2010). In addition, among the passive implementations, capacitor cross coupling (CCC) is available and widely used, but it can be employed only in a differential topology (Zhuo et al., 2000; Ye et al., 2013). Therefore, in this study, an inductor-based g_m-boosting technique and a transformer-based g_m-boosting technique are adopted in the CG stage and CS stage, respectively, which will be discussed in detail.

3.2 Inductor-based g_m-boosting in the CG stage

As far as we know, the CG stage has better linearity and higher isolation than the CS stage, but it exhibits a low gain. Given that the gate terminal in the CG stage does not need to be a pure direct current (DC) node for correct operation, the transformer-based g_m-boosting technique for CG configuration was proposed (Li XY et al., 2005; Guo et al., 2014, 2016). Actually, as stated below, a gate inductor instead of a transformer can boost the transconductance, leading to a simple design and a small chip area. The schematic is shown in Fig. 4a.

Fig. 4b shows the equivalent small-signal circuit at the CG stage with inductor-based g_m-boosting, where L_g is the boosting inductor. According to Fig. 4b, the effective transconductance of M_1, i.e., G_{m1}, can be derived as

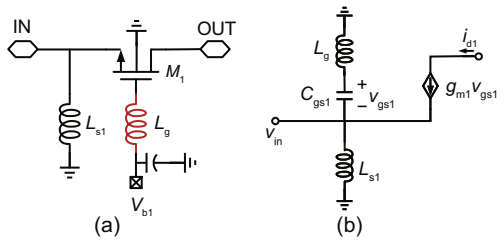

Fig. 4 Schematic (a) and equivalent small-signal circuit (b) at the CG stage with inductor-based g_m-boosting

$$G_{m1}=\frac{i_{d1}}{v_{in}}=g_{m1}(1+A), \tag{4}$$

where A is the boost factor and is defined as

$$A=\omega L_g\Big/\Big(\frac{1}{\omega C_{gs1}}-\omega L_g\Big). \tag{5}$$

From Eqs. (4) and (5), it can be found that the effective transconductance of M_1, i.e., G_{m1}, is boosted from g_{m1} by a factor of $1+A$, as long as A is positive. To ensure that A is positive, the following condition should be satisfied:

$$L_g<\frac{1}{\omega^2 C_{gs1}}. \tag{6}$$

Therefore, once inequality (6) is valid, increasing L_g can increase A, and hence G_{m1}.

To verify the conclusion drawn above, the magnitude and phase of the source node and gate node of M_1 in the cases with and without L_g are simulated in Figs. 5a and 5b, respectively. Note here that the decrease in the magnitude of V_s at low frequencies is due to the limited inductance of L_s, which is treated as a low impedance at low frequencies and conducts the incoming signal to ground. As can be seen, with the use of L_g, an out-of-phase voltage is generated at the gate node, resulting in a larger voltage drop across C_{gs1}. Accordingly, a higher G_{m1} is achieved, as shown in Fig. 5c. It is worth noting that as the frequency increases to the resonance frequency of L_g and C_{gs1}, the enhancement of G_{m1} is more significant. However, once the working frequency is higher than the resonance frequency of L_g and C_{gs1}, instability issues will occur.

3.3 Transformer-based g_m-boosting in the CS stage

As discussed above, a g_m-boosting CG stage can be obtained by adding an inductor at the gate terminal in the basic CG stage. However, intuitively

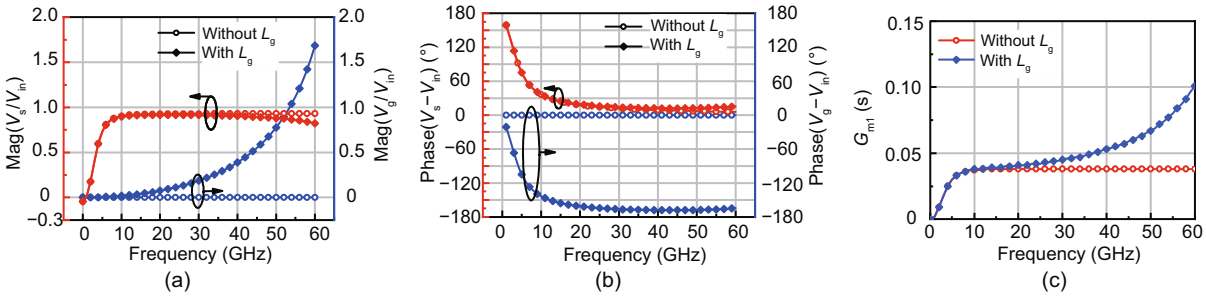

Fig. 5 Simulated magnitude (a), phase (b) of V_g and V_s, and simulated effective transconductance G_{m1} (c) with and without L_g (L_g = 100 pH)

inserting an inductor at the source terminal in a basic CS stage cannot boost transconductance. On the contrary, this topology leads to a source degeneration CS stage, which reduces effective transconductance (Andreani and Sjoland, 2001). Therefore, in this study, a g_m-boosting CS stage is established with the help of a transformer.

Fig. 6a shows the schematic at the CS stage with transformer-based g_m-boosting. By introducing an additional transformer TR_1, the RF signal at the source of M_2 is coupled with the primary winding L_{d1} and has the opposite sign, so the incoming signal is fed to M_2 at both the gate and the source terminal to increase the V_{GS} swing, and boosts the effective transconductance of M_2, i.e., G_{m2}. Using the small-signal model shown in Fig. 6b, the overall effective transconductance G_{m2} can be derived as

$$G_{m2}=\left(1+\frac{k\sqrt{L_{d1}L_{s2}}}{L_{d1}^{'}}\right)g_{m2}, \tag{7}$$

where k is the coupling coefficient, g_{m2} is the transconductance of M_2, and $L_{d1}^{'}$ is the equivalent inductance of the first winding of TR_1, which is defined as

$$L_{d1}^{'}=\frac{v_1}{si_1}. \tag{8}$$

To verify the transformer-based g_m-boosting CS stage, Fig. 7 presents the simulated G_{m2} for different coupling coefficient (k) values. When $k=0$, G_{m2} is the smallest. By increasing the transformer coupling, the effective transconductance is increased. Therefore, a larger coupling coefficient can be adopted to increase G_{m2}, hence the gain.

In practice, however, a perfect coupling, i.e., $k=1$, is unavailable, and an achievable k ranging from 0 to 0.7 would result in G_{m2} decreasing at higher frequencies, as shown in Fig. 7. To compensate for

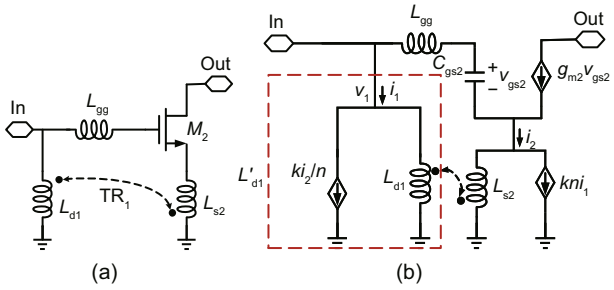

Fig. 6 Schematic (a) and equivalent small-signal circuit (b) at the CS stage with transformer-based g_m-boosting

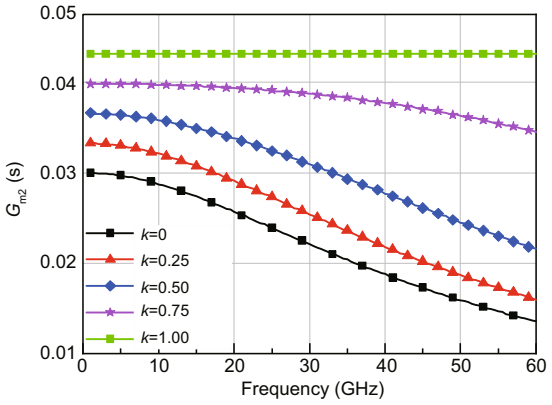

Fig. 7 Simulated effective transconductance of M_2 varying with k (L_{gg} = 0 pH is assumed)

the G_{m2} drop, a series inductor L_{gg} is inserted into the transformer-based CS stage, as shown in Fig. 6. By doing so, a series peaking will occur as L_{gg} increases, leading to a flat gain for one wideband LNA, as shown in Fig. 8. Here, the peaking frequency can be approximately calculated by

$$f_{peak}\approx\frac{1}{2\pi}\sqrt{\frac{1}{L_{gg}C_{gs2}}}, \tag{9}$$

where the small inductance L_{s2} is ignored.

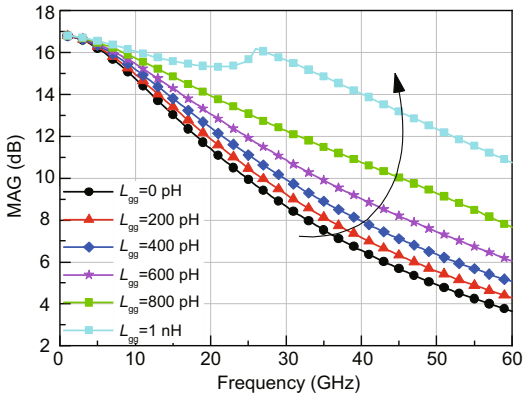

Fig. 8 Simulated maximum available gain (MAG) varying with L_{gg} where k equals 0.5

4 Implementation of the proposed LNA circuit

Based on above design considerations, a complete design methodology has been developed for the g_m-boosting CG-CS LNA. The schematic of the proposed LNA is depicted in Fig. 9, where capacitors C_{in}, C_{mid}, and C_{out} are used for DC decoupling and implemented by metal-insulator-metal (MIM) capacitors. To reduce the noise generated by parasitic resistance from passives, all the inductors or transformers are implemented using the top two thick metal layers. The bias of transistor M_1 is fed directly through the gate inductance L_g, while M_2 is biased to V_{b2} via a large resistor R_2.

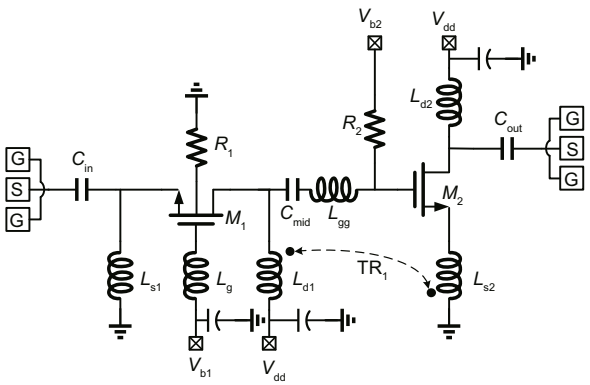

Fig. 9 Schematic of the proposed CG-CS LNA

4.1 Design considerations at the CG stage

At the CG stage, the loading effect is used to achieve simultaneous input and noise matching, as mentioned in Section 2. In this way, a relatively high g_m can be used to lower NF, while the input impedance is maintained at 50 Ω. Thus, in the design, a g_m=40 mS is selected. Fig. 10 demonstrates the working mechanism of the loading effect. Fig. 10a shows the load impedance at the CG stage (i.e., the input impedance at the CS stage), and the real part of the input impedance can be obtained using Eq. (3), as shown in Fig. 10b. Note that the imaginary part of the input impedance, including the inductor L_{s1}, the gate-source capacitor C_{gs}, and other imaginary parts generated from load impedance via the loading effect, is resonated out to zero over the whole operating bandwidth, as the solid gray line shows in Fig. 10c. Eventually, in the case of g_m=40 mS, i.e., low NF, the input matching bandwidth is effectively broadened, as shown by the pink line in Fig. 10d, when compared with the situation where the loading effect is neglected (that is to say, the channel resistor R_{ds1} is assumed to be infinite), shown as the black line in Fig. 10d.

In addition, as mentioned in Section 3, to reduce the power consumption or boost the gain, the gate inductor L_g is adopted for the g_m-boosting function. As stated in Section 3, by introducing L_g, the effective conductance of M_1 is boosted by a factor of $1+A$, where A is denoted in Eq. (5). Besides, after adding L_g, the input admittance can be expressed as

$$Y'_{in1}=\frac{1+g_{m1}R_{ds1}+sC_{gs1}(R_{ds1}+Z_{in2}+sL_g)}{(1+s^2C_{gs}L_g)(R_{ds1}+Z_{in2})}+\frac{1}{sL_{s1}}. \tag{10}$$

Comparing Eq. (10) with Eq. (1), it can be inferred that if L_g is small enough, i.e., $s^2C_{gs}L_g\approx 0$, Y'_{in1} is equal to Y_{in1}. This observation reveals that a small value of L_g does not influence the input matching, and fortunately, a small value of L_g leads to a stable amplifier because inequality (6) is satisfied. Thus, $L_g=100$ pH is chosen in this design.

Other than the above-mentioned techniques to obtain a low NF, the floating-body method originally proposed to lower NF in CS amplifiers (Chen HK and Chen, 2005) is adopted in the CG stage here to further reduce the noise. As shown in Fig. 9, the body terminal of transistor M_1 is grounded via a resistance R_1 instead of grounding directly. With the substrate resistance R_1 increasing to infinite (floating), the output admittance is decreased; i.e., the drain node of M_1 has a large impedance path to the substrate and decreases the signal loss through the

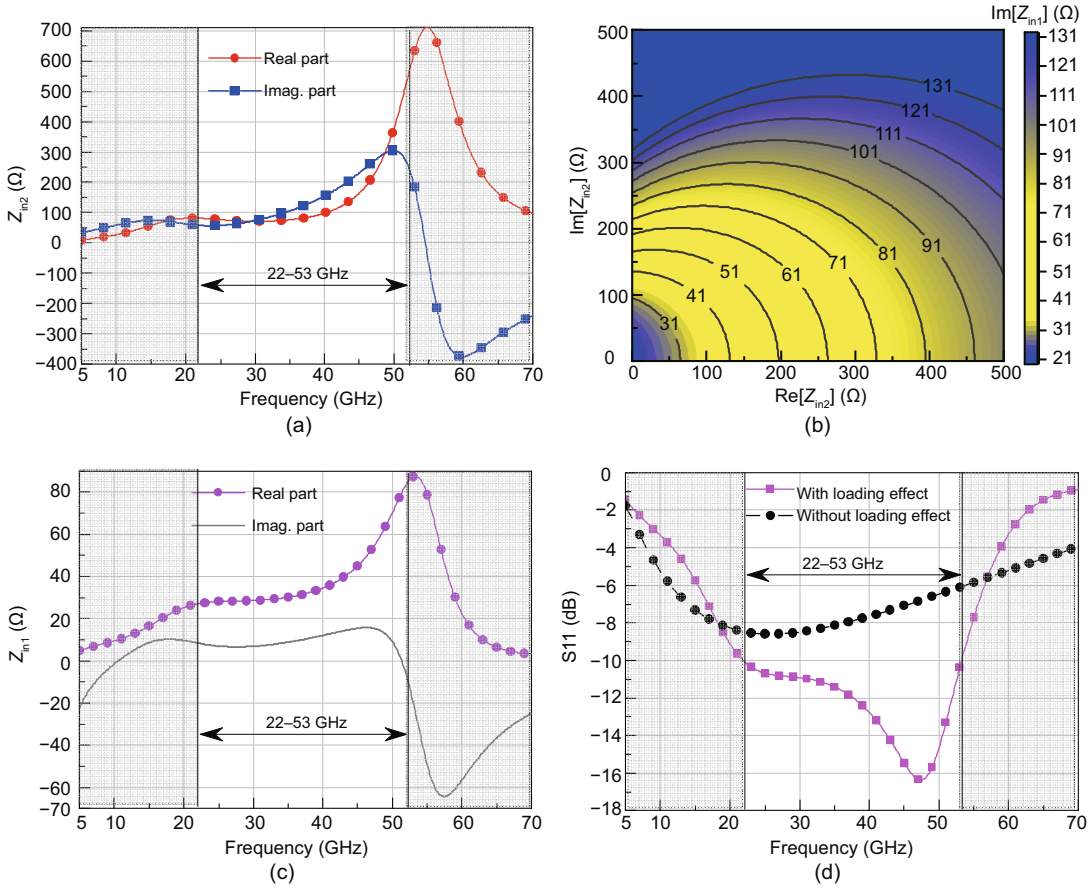

Fig. 10 Simulated Z_{in2} including the real and imaginary parts (a), correspondence from Z_{in2} to input resistance Re[Z_{in1}] via the loading effect (b), the obtained Z_{in1} varying with frequency (c), and simulated S11 with and without considering the loading effect (d) (References to color refer to the online version of this figure)

substrate, leading to gain and NF improvement. To study how much resistance is needed for noise suppression, NF_{min1} with various R_1 is investigated and illustrated in Fig. 11. As expected, increasing R_1 can improve NF_{min1} at high frequencies, but the improvement is marginal when $R_1 > 2$ kΩ.

4.2 Design considerations at the CS stage

For the second stage the CS stage is employed to further increase the LNA gain. As Fig. 9 shows, one transformer TR_1 is placed between the two stages to boost the effective transconductance at the CS stage, which was analyzed in Section 3. According to previous analysis and Fig. 7, a coupling coefficient as large as possible is preferred to obtain a high G_{m2}. However, due to the low gain at the CG stage, the noise contribution of the subsequent stages cannot be simply neglected. Therefore, NF_{min} at the CS stage (Fig. 6a) is investigated and plotted in Fig. 12. As

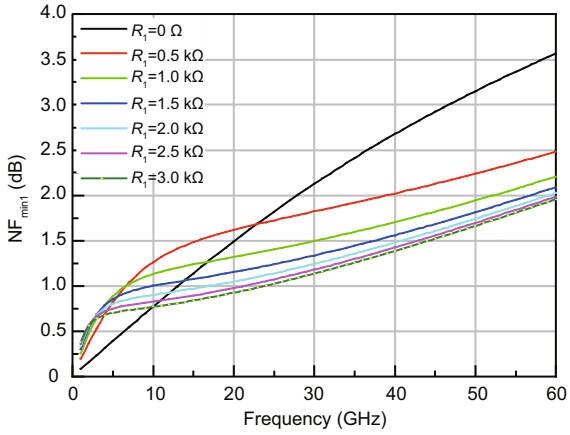

Fig. 11 NF_{min1} in the CG stage varying with R_1

References to color refer to the online version of this figure

can be seen from Fig. 12, unexpectedly, a larger coupling coefficient does not result in a lower NF_{min2}. In contrast, a moderate value around 0.25 would bring the lowest NF. Therefore, considering the tradeoff

between the gain and NF, a coupling coefficient ranging from 0.3 to 0.5 can be picked. Fig. 13a shows the physical layout of the transformer TR_1. As can be seen, to reduce the metal loss, the two transformer windings are implemented by the top metal layer (M9 layer), except for a short underpass realized in the M8 layer. Note that the input and output of the primary winding L_{d1} are in opposite directions, which facilitates connecting with the supply voltage (V_{dd}). The electromagnetic (EM) simulation results of the transformer are shown in Figs. 13b–13d. It can be seen that the maximum Q value is more than 15 due to the proper layout, and that the coupling coefficient is around 0.4, where a relatively good NF and gain are realized.

5 Measurement results

A micrograph of the LNA prototype fabricated in the TSMC 65-nm CMOS process is shown in Fig. 14. The total chip area (including bond pads) is 0.2 mm^2, and the active area occupies only about 0.1 mm^2. This prototype draws 13 mA from a supply voltage of 1.2 V, consuming a total power of 15.6 mW. The S-parameters, NF, input third-order intercept point (IIP3), and input 1-dB gain

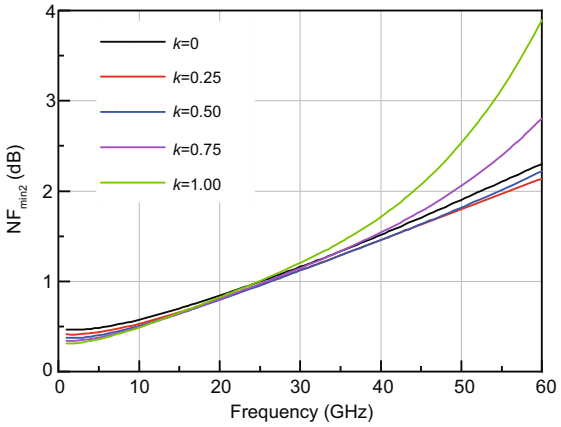

Fig. 12 NF_{min2} at the CS stage with various k

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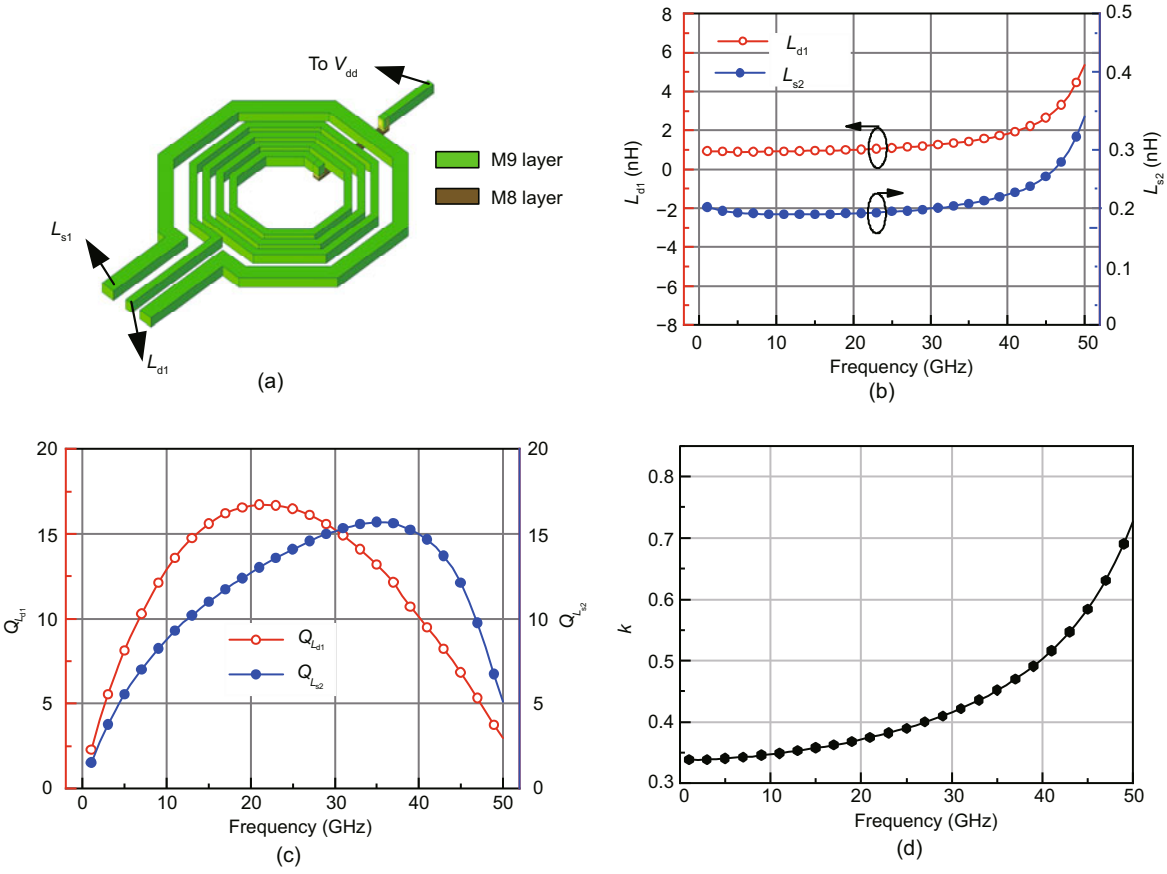

Fig. 13 Physical layout in three-dimensional view of the transformer TR_1 (a), and electromagnetic (EM) simulation results of TR_1: (b) self-inductance; (c) quality factor; (d) coupling coefficient

compression point (IP_{1dB}) measured on-wafer are reported in this section.

The two-port S-parameters of the LNA within the frequency ranging from 5 to 40 GHz are measured using the R&S ZVA 67 vector network analyzer. Fig. 15 shows the simulated and measured S11 and S21. The measured peak gain is 10.9 dB at 13 GHz. The gain deterioration at high frequencies between the simulation and measurement results is probably caused by the following factors: the model inaccuracy from transistors, the process variation, and the parasitic effect caused by dummy metal. From Fig. 15, the measured −3-dB bandwidth (BW) is 9.8 to 30.1 GHz (i.e., 20.3 GHz BW), giving a gain-BW (GBW) product of 221 GHz. Fig. 15 also shows the simulated and measured input return loss (S11), indicating that the input impedance is near 50 Ω (i.e., >10 dB return loss) from 14 to 40 GHz. Note that the measured S11 is shifted to a lower frequency, which is caused mainly by the parasitic capacitance of the RF pad. To evaluate the operation BW comprehensively, the GBW and input matching BW are combined into one metric, which is called the effective BW (BW_{eff}) (Cui and Long, 2020). The BW_{eff} is defined as the frequency range where the gain S21 is within −3 dB of its peak value and S11 is below −10 dB. Therefore, the measured BW_{eff} of this prototype is 16 GHz (i.e., from 14.1 to 30.1 GHz).

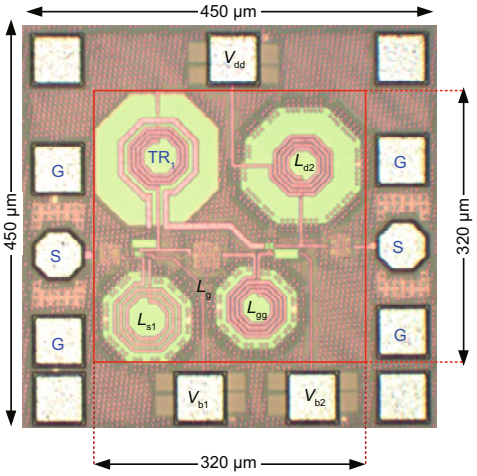

Fig. 14 Die photograph of the fabricated wideband LNA

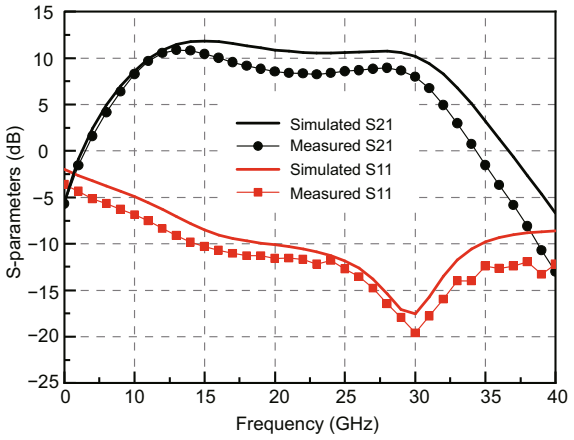

Fig. 15 Simulated and measured S-parameters of the proposed LNA

The NF measurement was conducted on-wafer using the classic Y-factor method. The characterization setup is illustrated in Fig. 16, where a noisecom NC346V 0.1–55 GHz noise source and an R&S FSW67 signal & spectrum analyzer with NF measurement option FSW-K30 are used to measure the NF of the LNA. Note that a built-in amplifier in the FSW67, with a gain of about 30 dB, is turned on as a pre-amplifier to provide sufficiently high gain to minimize the measurement uncertainties. As shown in Fig. 17, the measured NF is in excellent agreement with the simulated one, ranging from 3.2 to 5.7 dB. It should be noted that in a CG configuration, a 3.2-dB minimum NF is achieved due to the adoption of the SINM technique as described in Section 2, at the cost of power consumption.

To characterize the linearity of the proposed LNA, the frequency sweep and power sweep are conducted simultaneously in keysight N5245A to measure the input 1 dB compression point IP_{1dB}. As shown in Fig. 18, the measured IP_{1dB} is flat and ranges from −7.7 to −5 dBm from 10 to 30 GHz. IIP3 was also measured using the keysight N5245A at 25 GHz with 1 MHz tone spacing, and the measured IIP3 is 1.3 dBm.

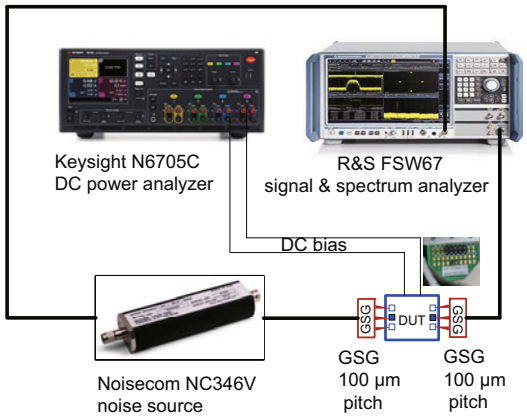

Fig. 16 NF measurement setup

To comprehensively demonstrate the advantages of our design, Table 3 shows the performance comparison among the state-of-the-art wideband LNAs and this work. Note that NF increases with the frequency; thus, for comparison, the LNAs working in the same frequency band as this prototype in the literature are selected. Two figures of merit (FoMI and FoMII) are used to compare the overall performance of LNAs, given by (Borremans et al., 2008; Parvizi et al., 2016b)

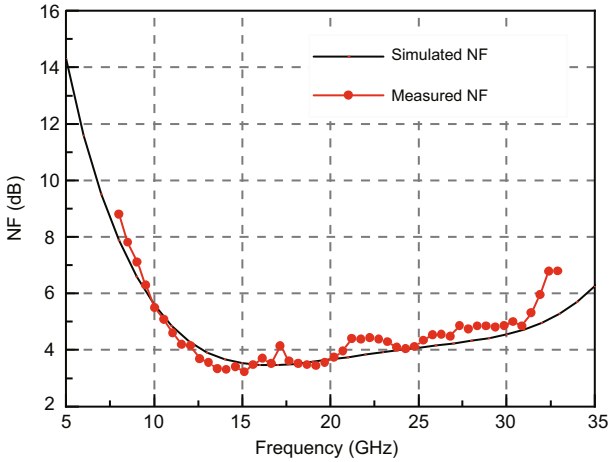

Fig. 17 Simulated and measured NF of the proposed LNA

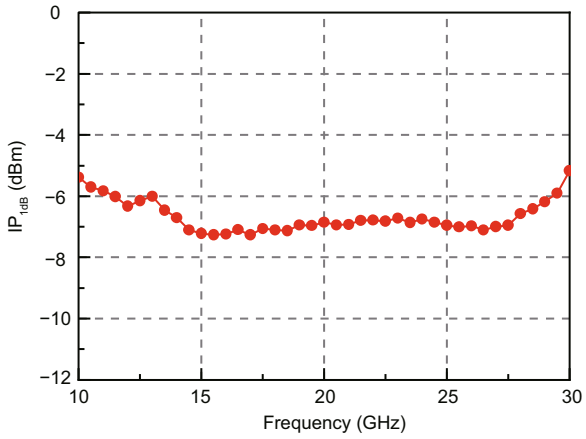

Fig. 18 Measured IP_{1dB} of the LNA across the whole bandwidth

$$\mathrm{FoMI} = 20\lg\frac{\mathrm{S21_{max}[lin]BW_{eff}[GHz]}}{(\mathrm{NF_{min}[lin]}-1)P_{\mathrm{dc}}[\mathrm{mW}]}, \tag{11}$$

$$\mathrm{FoMII} = 20\lg\frac{\mathrm{S21_{max}[lin]BW_{eff}[GHz]IIP3[mW]}}{(\mathrm{NF_{avg}[lin]}-1)P_{\mathrm{dc}}[\mathrm{mW}]A[\mathrm{mm^2}]}. \tag{12}$$

Note here that, to eliminate the randomness caused by noise measurement, the average NF instead of the minimum NF is adopted in FoMII.

Because of the employment of the SINM and g_m-boosting techniques described in Section 2 and Section 3, respectively, the proposed LNA exhibits comparable performance in terms of bandwidth, gain, NF, and linearity, indicating a high FoMI and the highest FoMII (where the area and linearity are included). It should be noted that this proposed LNA, fabricated in the 65-nm process, is comparable to the LNAs that are implemented with more advanced technologies, such as 45 nm CMOS SOI and 22 nm FD SOI.

6 Conclusions

A wideband LNA fabricated in 65-nm CMOS has been proposed and investigated in this work. The LNA has been cascaded with a CG stage and a CS stage. To alleviate the tradeoff among the input

Table 3 Performance summary of state-of-the-art LNAs and this work

Reference	BW_1 (band) (GHz)	BW_2 (band) (GHz)	BW_{eff} (band) (GHz)	Peak gain (dB)	NF (dB)	P_{dc} (mW)
Qin and Xue (2017a)	14.5 (15.8–30.3)	11.5 (18–29.5)	11.5 (18–29.5)	10.2	3.3–5.7	12.4
Qin and Xue (2017b)	21.4 (7.6–29)	8 (8–12.5&20.5–24)	8 (8–12.5&20.5–24)	10.7	4.5–5.6	12.1
Li CJ et al. (2018)	17 (14–31)	2 (26–28)	2 (26–28)	12.8	1.3–1.6	15
Cui and Long (2020)	17 (19–36)	10 (22–32)	10 (22–32)	21.5	1.7–2.2	17.3
This work	**20.3 (9.8–30.1)**	**26 (14–40)**	**26 (14.1–30.1)**	**10.9**	**3.2–5.7**	**15.6**

Reference	IIP3@freq (dBm@GHz)	Size (mm^2)	Process	FoMI	FoMII
Qin and Xue (2017a)	−0.5@22	0.18	65 nm CMOS	8.8	18.1
Qin and Xue (2017b)	1.4@21.5	0.30	65 nm CMOS	1.9	13.4
Li CJ et al. (2018)	4@24	0.30	45 nm CMOS SOI	4.4	21.8
Cui and Long (2020)	−13.4@22	0.17	22 nm FD SOI	23.1	10.2
This work	**1.39@25**	**0.20**	**65 nm CMOS**	**10.4**	**22.3**

BW_1: −3 dB gain bandwidth; BW_2: −10 dB input matching bandwidth; BW_{eff}: overlapping bandwidth of BW_1 and BW_2. P_{dc}: DC power consumption. The results of this work are in bold

matching, NF, and gain in the CG stage, the loading effect has been used instead of conventional feedback techniques to achieve SINM. Furthermore, to enhance the gain (or save the power consumption), the inductor- and transformer-based g_m-boosting techniques have been analyzed in detail and adopted in the CG stage and CS stage, respectively. Moreover, the floating-body method, which was proposed to lower NF in CS amplifiers, has been adopted in the CG stage here to further reduce the NF. Fabricated in a 65-nm CMOS technology, the LNA achieves the highest FoMII with competitive linearity and bandwidth performance.

Contributors

Hongchen CHEN and Quan XUE designed the research, measured the chip, and drafted the manuscript. Haoshen ZHU helped with the chip measurement and revised the paper. Liang WU helped revise the paper. Wenquan CHE gave a lot of guidance and finalized the paper.

Compliance with ethics guidelines

Hongchen CHEN, Haoshen ZHU, Liang WU, Wenquan CHE, and Quan XUE declare that they have no conflict of interest.

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