Frontiers of Information Technology & Electronic Engineering
www.jzus.zju.edu.cn; engineering.cae.cn; www.springerlink.com
ISSN 2095-9184 (print); ISSN 2095-9230 (online)
E-mail: jzus@zju.edu.cn

High linearity U-band power amplifier design: a novel intermodulation point analysis method*

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Received Mar. 4, 2022; Revision accepted Aug. 21, 2022; Crosschecked Oct. 20, 2022

Abstract: A power amplifier's linearity determines the emission signal's quality and the efficiency of the system. Nonlinear distortion can result in system bit error, out-of-band radiation, and interference with other channels, which severely influence communication system's quality and reliability. Starting from the third-order intermodulation point of the milimeter wave (mm-Wave) power amplifiers, the circuit's nonlinearity is compensated for. The analysis, design, and implementation of linear class AB mm-Wave power amplifiers based on GlobalFoundries 45 nm CMOS silicon-on-insulator (SOI) technology are presented. Three single-ended and differential stacked power amplifiers have been implemented based on cascode cells and triple cascode cells operating in U-band frequencies. According to nonlinear analysis and on-wafer measurements, designs based on triple cascode cells outperform those based on cascode cells. Using single-ended measurements, the differential power amplifier achieves a measured peak power-added efficiency (PAE) of 47.2% and a saturated output power (P_{sat}) of 25.2 dBm at 44 GHz. The amplifier achieves a P_{sat} higher than 23 dBm and a maximum PAE higher than 25% in the measured bandwidth from 44 GHz to 50 GHz.

Key words: CMOS silicon-on-insulator (SOI); Linearity analysis; Milimeter wave (mm-Wave); Power amplifier
https: //doi.org/10.1631/FITEE.2200082 **CLC number:** TN92; TN43

1 Introduction

CMOS technology offers low fabrication cost, high integration capability, and process consistency for implementing wireless transceivers for communication, radar, and other applications (Ghorbani and Ghaznavi-Ghoushchi, 2017; Vigilante and Reynaert, 2018; Li et al., 2019). Compared to low-power modules such as low-noise amplifiers, mixers, frequency synthesizers, and analog digital converters, which can easily achieve good performance in scaled CMOS technologies (Elkholy et al., 2018; Xu and Kinget, 2018; Chen HC et al., 2021), CMOS power amplifiers (PAs) are notoriously difficult to implement. CMOS PAs have two main drawbacks of poor linearity and low efficiency because of the low device breakdown voltage and the lossy silicon substrate. Generally, PAs' linearity is evaluated by nonlinear distortion metrics such as the adjacent channel power ratio (ACPR) and error vector magnitude (EVM) for complex modulated signals, third-order intercept point (input intercept point (IIP_3) and output intercept point (OIP_3)) for harmonic signals, and intermodulation distortion for two tones. Nonlinear distortion results in out-of-band radiation and interference with other channels, which severely influence the signal-to-noise ratio (SNR) and bit error ratio (BER) (Wang H et al., 2015).

Linear PAs required in the 4th and 5th generation mobile communication standards are weakly nonlinear systems. Feedforward, feedback, and digital predistortion (DPD) all compensate for the nonlinear distortion

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of the PA circuit by adding auxiliary circuits. The control of the accuracy of the component parameters of the auxiliary circuit, the problems of stability, and the additional power consumption make the circuit design complicated and practical application difficult (Varahram et al., 2014; Borel et al., 2021). Linearity and efficiency are two contradictory indicators of PA circuits. The combination of crest factor reduction (CFR) and DPD can improve efficiency while improving PA linearity. However, a good CFR/DPD model structure is difficult to establish (Wang SQ et al., 2020).

There are two main methods for linearity analysis of weakly nonlinear systems, namely, power series and Volterra series (Cripps, 2006). The power series models the nonlinearity of the PA while ignoring the parasitic capacitances and inductances of the design, resulting in insufficient timing coefficients in modeling. Volterra series based on a behavioral model, on the other hand, is much more accurate for the linearity analysis of weakly nonlinear systems since it takes parasitic capacitance and memory effect into consideration. When the nonlinear orders are high, generalized memory polynomial (GMP) models are prone to numerical problems (Reina-Tosina et al., 2015; Lopez-Bueno et al., 2016). This study considers the parasitic parameters of CMOS devices in the form of power series and analyzes the linearity of the PA from the intermodulation distortion point, while taking into account the circuit parasitic parameters, which avoids complicated numerical problems.

In this work, we present a theoretical analysis of the linearity of CMOS stacked cell PAs. To further demonstrate this, a differential stacked PA based on modified triple cascode cells operating in the U-band (44–50 GHz) is presented and compared with our previous work PA1–3 in the reference (Helmi and Mohammadi, 2016). To the best of our knowledge, this new differential design achieves the highest reported PAE and one of the highest saturated output powers P_{sat} along with linear power among previously reported mm-Wave CMOS PAs.

2 Linearity analysis

The CMOS PAs investigated here are based on nanoscale CMOS silicon-on-insulator (SOI) technology, in which the transistor is operating under short-channel effects. To be able to perform linearity analysis, one has to understand the nonlinearity mechanisms in the transistor.

2.1 Theoretical analysis

First, a compact semiempirical DC model I_D (V_{GS}, V_{DS}) for short channel 45 nm CMOS SOI technology applicable in all regions of device operation is analyzed, taking the consideration of computer-aided-design and accurate fittings to device characteristics over a range of geometry and layout features, as shown in Eq. (1):

$$I_D = g_m V_{gs} \frac{V_{DS}/V_{Dsat}}{\left[1 + \left(V_{DS}/V_{Dsat}\right)^{\beta}\right]^{\frac{1}{\beta}}}, \tag{1}$$

where g_m is the device transconductance, V_{Dsat} is the saturation voltage of the NMOS transistors extracted to be ~0.2 V in strong inversion, and β is an empirical smoothing parameter equal to 1.8 in this technology.

Fig. 1 presents the relationship between the drain current normalized by width (I_D/W), gate-source voltage V_{GS}, and drain-source voltage V_{DS}. It is obvious that the measured data (circle) agree with our model (line). The I_D/W–V_{GS} dependence when V_{DS}=1 V is almost linear, leading to a constant transconductance per width g_m/W of 1.2 ms/μm for NMOS transistors in this technology. The supposed virtual-source model is simple and reasonably accurate, as it is based on the physics of short channel device transport characteristics and two fitting parameters; detailed information can be found in our previous work (Shen et al., 2017). In addition, the historical virtual source model in the literature produces good agreement with the Si MOSFET and other InGaAs HEMTs (Yeh and Fossum, 1995).

Eq. (1) can be approximated with a power series:

$$I_D = a_0 + a_1 V_{DS} + a_2 V_{DS}^2 + a_3 V_{DS}^3, \tag{2}$$

where a_0 to a_3 are constants for a given V_{GS} bias. The nonlinearity of the NMOS transistors is partially due to nonlinear gate-drain capacitance (C_{gd}) extracted using bias-dependent *S*-parameters, as shown in Fig. 2a (Kondoh, 1986; Le et al., 2021). For a specific V_{GS}, C_{gd} may be approximated by

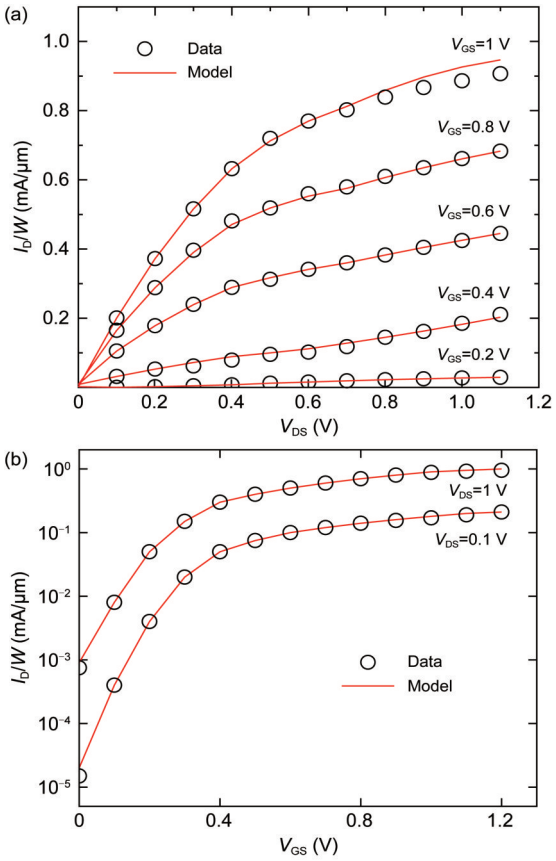

Fig. 1 Virtual source model (curves) vs. measured DC data (circles): (a) I_D/W vs. V_{DS} when V_{GS} varies from 0.2 V to 1.0 V in a step of 0.2 V; (b) I_D/W vs. V_{GS} in linear scale when V_{DS} is 0.1 V or 1 V

$$C_{gd} = c_0 + c_1 V_{DS} + c_2 V_{DS}^2 + c_3 V_{DS}^3 , \quad (3)$$

where c_0 to c_3 are constants for a given V_{GS} bias. As shown in Fig. 2b, the drain-body capacitance C_{db} is relatively constant with respect to V_{DS} (and V_{GS}), as long as the device is in strong inversion.

2.2 Power cells

There are two types of power cells used in stacked PAs considered in this work: the standard cascode cell and the triple cascode cell. The cells along with two important capacitances that affect the high-frequency linearity response are shown in Fig. 3. According to our previous analysis (Cui et al., 2016; Helmi et al., 2016), M_i (i=1, 2, 3) is based on the 45 nm CMOS process and 120 μm wide transistor. All capacitances except for those at the output node can be ignored at high frequencies, as they can be shunted by large conductance or tuned out with input inductance.

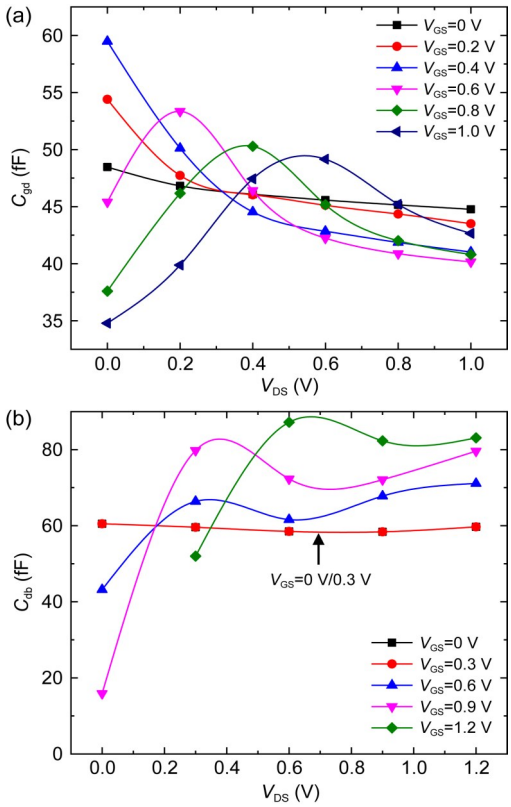

Fig. 2 Bias dependence of extracted C_{gd} (a) and C_{db} (b) as functions of V_{DS} for a 120 μm wide transistor

Capacitor C_{pari} (i=2, 3) to the ground is the parasitic capacitance of the source leaking to the substrate but also includes the parasitic capacitance caused by the metal connection of the layout. If these cells are optimally designed to handle maximum power, the V_{GS}'s of all transistors in each design are identical, and the sum is equal to the input voltage V_{in}. Similarly, each transistor drain-source voltage swing of V_{DS} is added to obtain the output voltage V_{out}. Therefore, the individual transistor V_{DS} is identical and equal to $V_o/2$ for the cascode cell (Fig. 3a) and $V_o/3$ for the triple cascode cell (Fig. 3b).

For the cascode cell, Eqs. (2) and (3) can be rewritten as

$$I_D = a_0 + \frac{a_1}{2} V_o + \frac{a_2}{4} V_o^2 + \frac{a_3}{8} V_o^3 , \quad (4)$$

$$C_{gd2} = c_0 + \frac{c_1}{2} V_o + \frac{c_2}{4} V_o^2 + \frac{c_3}{8} V_o^3 . \quad (5)$$

The output current of the cell I_o can be written as

$$I_o = I_D + I_{Cgd2} + I_{Cpar2} , \quad (6)$$

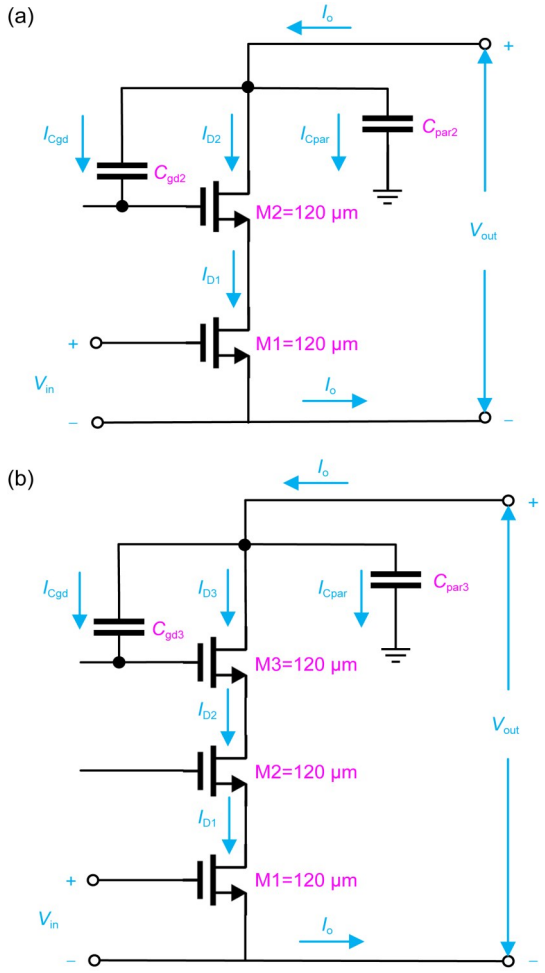

Fig. 3 Schematic of cascode (a) and triple cascode (b) cells and their main capacitances (Cui et al., 2016)

where I_D is the drain current, I_{Cgd2} is the parasitic current flowing through the capacitance C_{gd2}, and I_{Cpar2} is the current of C_{par2}, which are shown in Fig. 3a. As all transistors' V_{GS}'s are optimized to be equal, M2's V_{GS} is the same as M1's V_{in}. According to Ohm's law, I_{Cgd2} can be written as

$$I_{Cgd2} = j\omega C_{gd2}\left(\frac{V_o}{2} - V_{in}\right). \tag{7}$$

Assuming a linear gain mechanism in these short-channel transistors, one obtains

$$V_{in} = \left(V_{oQ} - V_o\right)/g_m R_L, \tag{8}$$

leading to

$$I_{Cgd2} = j\omega C_{gd2}\left(\frac{V_o\left(2 + g_m R_L\right)}{2g_m R_L} + \frac{V_{oQ}}{g_m R_L}\right), \tag{9}$$

where V_{oQ} is the quiescent output voltage of the cascode cell and is equal to 2 V (1 V per transistor). In the above equation, C_{gd2} can be substituted by Eq. (5), leading to an equation for I_{Cgd2} in terms of the power series of V_o. The current through parasitic capacitor C_{par2}, which is mostly formed by drain-to-body capacitance (C_{db2}) and hence is a linear function of V_o, is

$$I_{Cpar2} = i \cdot j\omega C_{par2} \cdot V_o, \tag{10}$$

where i is the stack number, meaning that if the cascode cell is at the bottom of the stacked CMOS PA, then i=1, and if the cell is the second from the bottom, then i=2, and so on. Next, one can substitute different components of Eq. (6) with the power series shown above to achieve a relationship describing I_o as a function of V_o. Note that the function is frequency dependent as it includes the effect of output capacitances C_{gd2} and C_{par2}. The output third-order intercept point OIP_3 can be found by dividing the coefficient of the linear term of the I_o–V_o relationship by the product of 3/4 of its cubic coefficient and $2R_L$:

$$\mathrm{OIP}_{3\mathrm{casc}} = 10\lg\left(\frac{8}{3R_L}\cdot\left|\frac{a_1 g_m R_L + j\omega\left(2iC_{par3}g_m R_L + c_0\left(2 + g_m R_L\right) - c_1 V_{oQ}\right)}{a_3 g_m R_L + j\omega\left(c_2\left(2 + g_m R_L\right) - c_3 V_{oQ}\right)}\right|\right). \tag{11}$$

A similar approach can be applied to the triple cascode cell design. The overall drain current I_D and the gate-drain capacitance at the output node C_{gd3} can be written as

$$I_D = a_0 + \frac{a_1}{3}V_o + \frac{a_2}{9}V_o^{\,2} + \frac{a_3}{27}V_o^{\,3}, \tag{12}$$

$$C_{gd3} = c_0 + \frac{c_1}{3}V_o + \frac{c_2}{9}V_o^{\,2} + \frac{c_3}{27}V_o^{\,3}. \tag{13}$$

From Fig. 3b, I_{Cgd3} can be written as

$$I_{Cgd3} = j\omega C_{gd3}\left(\frac{V_o}{3} - V_{in}\right). \tag{14}$$

Assuming a linear gain mechanism, one obtains

$$I_{Cgd3} = j\omega C_{gd3}\left(\frac{V_o\left(3 + g_m R_L\right)}{3g_m R_L} + \frac{V_{oQ}}{g_m R_L}\right), \tag{15}$$

where V_{oQ} is equal to 3 V (1 V per transistor). The output current of the cell I_o can be written as

$$I_o = I_D + I_{Cgd3} + I_{Cpar3}, \tag{16}$$

where

$$I_{Cpar3} = i \cdot j\omega C_{par3} \cdot V_o. \tag{17}$$

These equations lead to the following equation:

$$\mathrm{OIP}_{3\mathrm{triple\_casc}} = 10\lg\left(\frac{6}{R_L}\cdot\left|\frac{a_1 g_m R_L + j\omega\left(3iC_{par3}g_m R_L + c_0\left(3+g_m R_L\right) - c_1 V_{oQ}\right)}{a_3 g_m R_L + j\omega\left(c_2\left(3+g_m R_L\right) - c_3 V_{oQ}\right)}\right|\right). \tag{18}$$

Therefore, one can obtain a basic idea of cascode or triple stacked cell, or a combination of multiple cascodes or stacked cells' OIP_3 according to the above equations. Fig. 4 shows the values of OIP_3 of both cascode and triple cascode cells obtained from the above analysis as functions of frequency. It also shows the measured $P_{1\,\mathrm{dB}}$ values for a triple cascade cell and a cascade amplifier. In general, the OIP_3 values are approximately 10 dB higher than the $P_{1\,\mathrm{dB}}$ values, which is consistent with the equation for weakly nonlinear class A and AB amplifiers:

$$P_{1\,\mathrm{dB}} \approx \mathrm{OIP}_3 - 9.6\ \mathrm{dB}. \tag{19}$$

Table 1 summarizes all the parameters and biasing values used in Eqs. (11) and (18) for the cascode and triple cascode cells. Note that in this table, the cascode cell has a higher parasitic capacitance than that of the triple cascode due to its standard layout implementation as opposed to the triple cascade cell with a combined layout, which leads to suppressed parasitic capacitance by a factor of 3 (Helmi et al., 2016).

Table 1 Extracted parameters of cascode and triple cascode cells based on measurement

Parameter	Value	Parameter	Value
V_{oQ} (V)	(3, 2)*	a_0 (A)	0.005 562
V_{Dsat} (V)	0.2	a_1 (A/V)	0.030 61
β	1.8	a_2 (A/V^2)	−0.0221
c_0 (F)	6.00E-14	a_3 (A/V^3)	0.005 75
c_1 (F/V)	−6.45E-14	C_{par} (F)	(2.00E-14, 6.00E-14)*
c_2 (F/V^2)	7.81E-14	g_m (A/V)	0.18
c_3 (F/V^3)	−3.26E-14	R_L (Ω)	50

* In the brackets, the former value corresponds to triple cascode, and the latter corresponds to cascode; as for others, the parameters of cascode and triple cascode cells are of the same value

Fig. 5 shows the analytically calculated OIP_3 of the PAs with two stacked triple cascode cells and three stacked cascode cells (PA1 and PA2 in Helmi et al. (2016)). Additionally, the measured output $P_{1\,\mathrm{dB}}$ of PA1 to PA3 as well as a differential PA (PA4) is designed based on modified triple cascode cells. Note that the parasitic capacitances responsible for efficiency and linearity degradations are mitigated in PA1 and PA4 by using a combined layout technique for triple cascode cells (Helmi and Mohammadi, 2016).

Again, the difference between the analytically calculated OIP_3 and measured $P_{1\,\mathrm{dB}}$ in PA1 and PA2 is

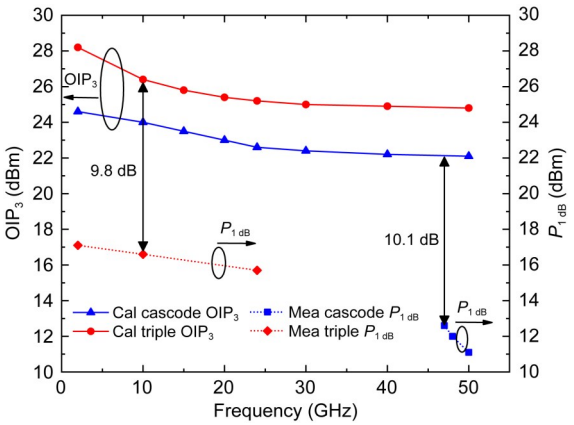

Fig. 4 Calculated OIP_3 and measured $P_{1\,\mathrm{dB}}$ for cascode and triple cascode cells as functions of frequency using the analytical approach (Eqs. (11) and (18))

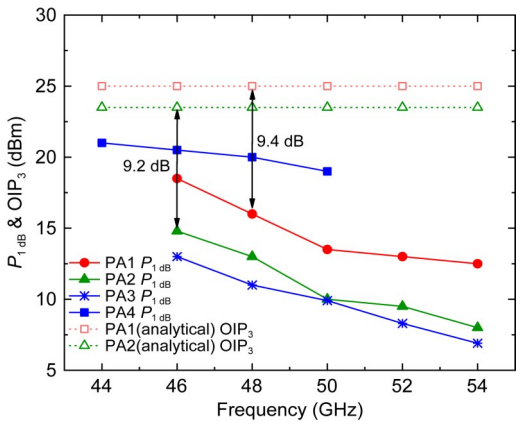

Fig. 5 Measured $P_{1\,\mathrm{dB}}$ values for PA1 to PA4 as functions of frequency and analytical OIP_3 values for PA1 and PA2 vs. frequency for comparison

approximately the expected 10 dB value, indicating that the analytical technique is reliable not only for cascode cells but also for integrated PA designs. Although the variation in measured $P_{1\,\mathrm{dB}}$ with frequency is much more emphasized than the trend observed in calculated OIP_3 values due to the phase variation of combining signals, the overall trends are similar to performance degradation as frequency increases.

Observing Eqs. (11) and (18), it can be found that in addition to the frequency and stacked transistor's size affecting the value of OIP_3, the bias voltage is an influencing factor. In the next section, we will analyze the influence of bias voltage on linearity in combination under two bias conditions, 4.8 V and 6 V.

3 mm-Wave CMOS power amplifier design with linearity analysis

3.1 Differential power amplifier design

A schematic of the differential PA design (PA4) and a photograph of the fabricated chip in GlobalFoundries 45 nm CMOS SOI technology are shown in Fig. 6. To ensure the operation of the frequency band, a 120 μm wide transistor is chosen. Considering that the knee voltage of the transistor is approximately 0.3 V, the peak source-drain swing is 1.2 V. To prevent breakdown of the uppermost transistor in the stack structure and stabilize the circuit operation, the maximum bias voltage of the transistors used in this work is selected to be 1 V.

The input signal is converted through the transformer network to a differential signal amplified by two stacked power units, each giving a DC bias voltage of 6 V. The single-sided circuit has a triple stack per power cell, and the overall voltage swing can reach six transistors. Compared with the common source and cascode, the triple stack structure has higher gain, better isolation, better stability, and higher output impedance. C1 blocks the DC signal. C2 regulates the output signal phase while forming part of the impedance matching network. Compared to the single-ended design PA1, PA4 is further optimized to push the operation into deep class AB, resulting in a lower power gain, but slight improvements in both output power and PAE. Two-way differential combination increases the output power, and PAE improvement is achieved

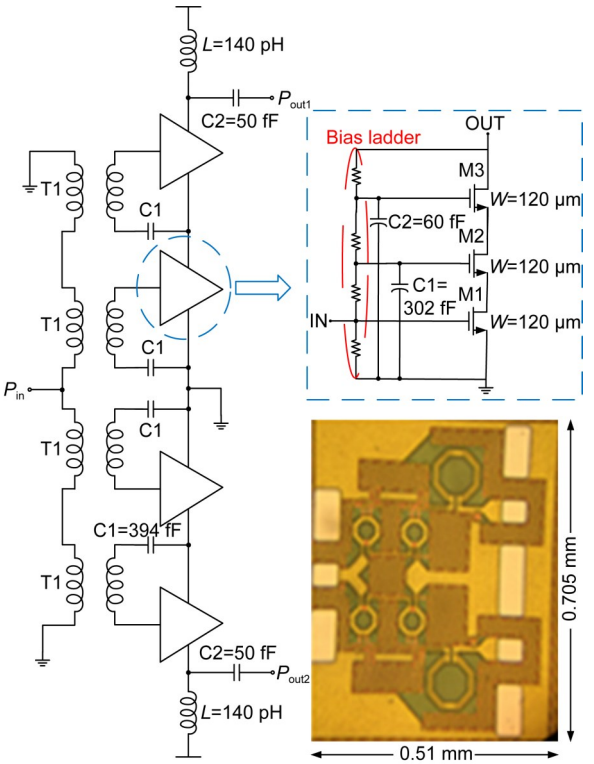

Fig. 6 Schematic and chip photograph of the differential power amplifier (PA4) implemented in this work

by adjusting the values of the resistors in the resistor ladder to set a slightly smaller drain current in the stack to make the transistor work in the deep class AB region.

Two voltage transformers T1 in series are used at each input, and the main coil is connected in series to 50 Ω to match the input, coupling the power into the transistor. To optimize the planar input transformer T1's width, radius and metal gaps, ANSYS Electronics is applied to realize a reasonably high Q and suitable inductance for input matching. As Fig. 7 shows, the transformer uses the top metal lb as the primary coil, and metal ua and ub work together for the secondary coil. A coupling coefficient of nearly 0.7 is achieved to eliminate the magnetic flux and thus hysteresis loss and eddy current in transformer operation.

3.2 Measurement results

Power measurements were preformed using Keysight E4419B power meters along with a Keysight N8488A power sensor at room temperature. The input power was provided by a Keysight E8361A vector network analyzer (VNA) and a Giga-Tronics GT-1050A

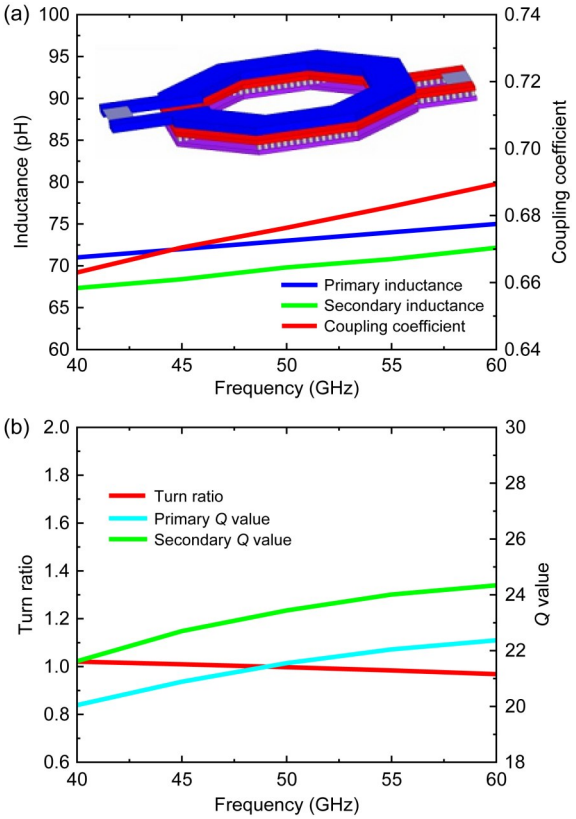

Fig. 7 Simulated transformer performance: (a) primary and secondary inductance and coupling coefficient; (b) primary and secondary *Q* value and turn ratio

driver amplifier. Set the VNA as the signal source to continuous wave mode, and the operating frequency was 44 GHz. The input power sweep range was from −20 dBm to 20 dBm. The characterization setup is illustrated in Fig. 8.

Before testing, the vector network instrument was turned on for a period of time to prevent subsequent temperature deviation. Use the GSG (ground–signal–ground) probe to calibrate the vector network analyzer, and use the SOLT (short circuit, open circuit, load, through) calibration technique, that is, by measuring the calibration piece with known characteristics. After calibration, import the calibration results. The sweep frequency range was set to 35–55 GHz, the input signal power was set to 0 dBm, and the four *S*-parameter curves were obtained. Fig. 9 shows the measured *S*-parameters of PA4, which closely confirm the simulation results. A small signal gain of a maximum of 13.4 dB can be seen at 47 GHz. Not considering the electromagnetic coupling and external interference will cause the small signal result to shift to high frequency. During simulation, we matched the circuit to high frequency to approximately 48 GHz.

Use the continuous wave generated by the signal source to test the power performance of the PA. To accurately calibrate the power to the probe level, we tested all input power and input frequency three times for straight-through, loaded only the input cable and only the output cable, calculated the actual transmission loss of each probe, and then weighted them separately according to the actual input power and output power for high on-chip performance. Fig. 10 shows the simulation and measurement power performance, including output power P_{out}, power gain (Gain), and PAE versus input power at 44 GHz under two bias conditions of 4.8 V (0.8 V/transistor) and 6 V (1 V/transistor).

PA used a single-ended measurement technique, where one output was terminated with a 50 Ω load. Upon switching the output terminals, there was no

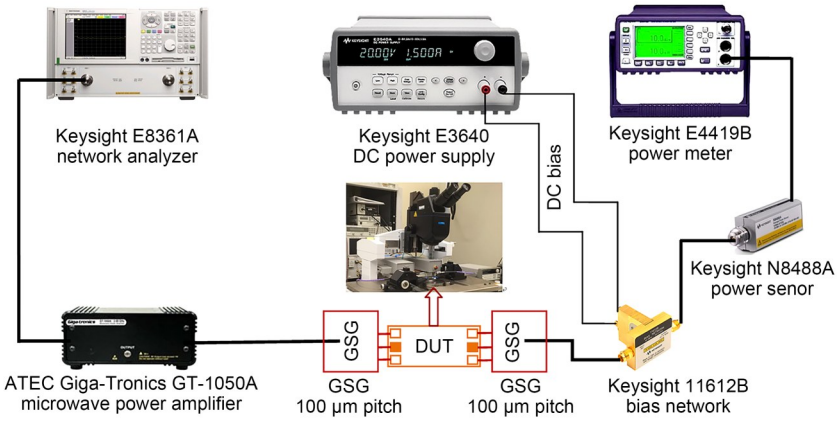

Fig. 8 Power measurement setup

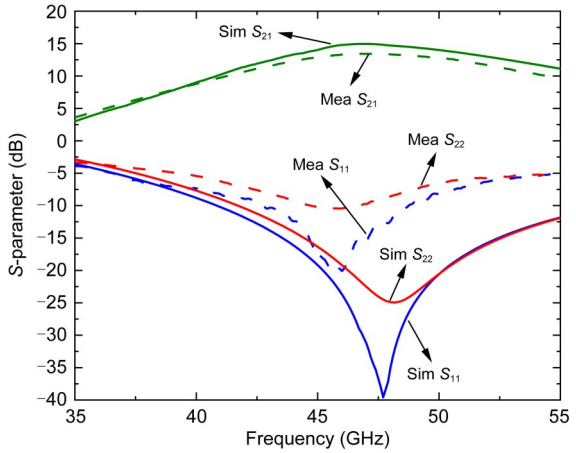

Fig. 9 Simulated (solid line) and measured (dashed line) *S*-parameters of the fabricated differential PA4 chip under 6 V supply

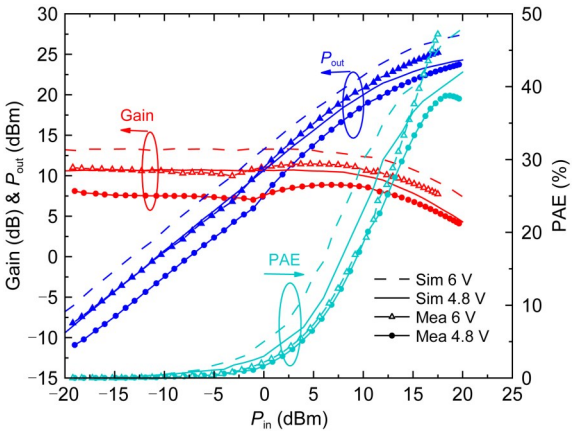

Fig. 10 Simulated and measured power for the differential PA (PA4) at 44 GHz under two bias conditions (4.8 V and 6 V)

discrepancy between the two output levels. Under a supply voltage of 6 V at 44 GHz, differential PA4 delivered a maximum differential output power of 25.2 dBm and a maximum PAE of 47% with a linear differential gain of 11.4 dB, which agreed well with the simulation results. As shown in Fig. 10, the output power of the PA was still not saturated, and the maximum PAE point was not yet achieved. The setup losses, relatively small power gain, and limited output power capability of the driver amplifier are the reasons that this PA cannot be characterized to its full potential. Moreover, the design showed a class AB behavior with a gain expansion for input powers up to 7 dBm and gain compression for higher input powers. With a smaller supply voltage of 4.8 V, the maximum differential output power was reduced to 23.7 dBm and PAE was reduced to 38%. Comparing the simulation and measurement results under the two bias conditions, increasing the value of V_{oQ} improved the overall circuit performance including linearity, output power, gain, and PAE. The increase in power supply energy allowed the device gain to be maintained.

Fig. 11 shows the simulation and measurement results of power characterizations of the differential PA (PA4) over a frequency range of 44 to 50 GHz. The comparison was also performed using two different values of supply voltage, namely, 4.8 V and 6 V. As shown in the figure, the best output power and PAE performance were achieved at 44 GHz under a supply bias of 6 V. The maximum PAE under this bias condition decreased monotonically to 25% at 48 GHz and then increased slightly to 26% at 50 GHz. The maximum output power decreased from 25.2 dBm to 24.2 dBm as the frequency increased from 44 GHz to 50 GHz. The power gain reached 13 dB at 46 GHz and then slightly decreased as the frequency increased to 50 GHz, which agreed with the simulation results. The saturated output power remained close to 25 dBm for all the measured frequencies at a bias supply of 6 V. When the supply voltage was reduced to 4.8 V, all power performance metrics deteriorated except for the maximum PAE at 48 GHz and 50 GHz, which were slightly higher than those achieved with a 6 V power supply. In general, this mm-Wave PA delivers excellent output power and PAE performance in the measured frequency range from 44 to 50 GHz.

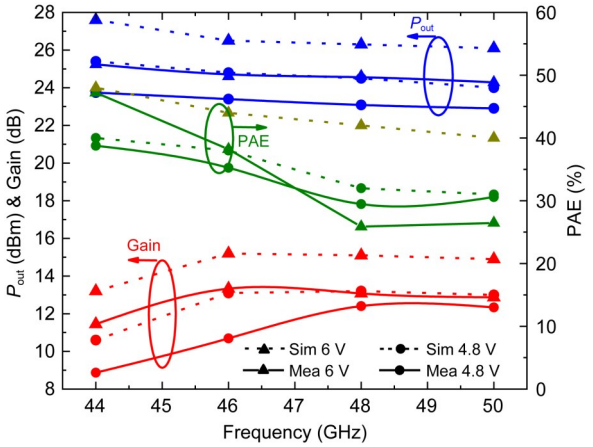

Fig. 11 Simulated and measured power P_{out}, Gain, and PAE vs. frequency for the differential PA (PA4) under two bias conditions (4.8 V and 6 V)

3.3 Linearity analysis

As only one mm-Wave signal source was available for testing, linearity characterizations based on two-tone measurement and complex modulation schemes (such as the WCDMA test) were not feasible. Instead, an IIP_3 simulation for the proposed differential PA4 under 6 V supply is shown in Fig. 12. It lists the 44 GHz and 50 GHz IIP_3 results of gain and third-order intermodulation distortion points with a 50 MHz gap. They further demonstrated our linearity analysis mentioned before for weakly nonlinear PAs operating in class AB mode such as the mm-Wave PA studied here. The measurement results in Fig. 5 validate the linearity theory as indicated in Eq. (18). The differential PA4 design outperformed the other PAs (PA1–3) in terms of maximum linear output power $P_{1\,dB}$ by at least 2 dB.

Table 2 shows the performance comparison of U-band CMOS amplifiers. CMOS SOI shows its advantages in power and efficiency. Based on GlobalFoundries 45 nm CMOS SOI technology, to improve the linearity of the circuit, after the calculation of OIP3, we can roughly estimate the value of $P_{1\,dB}$, and then select the size of the stacked transistor appropriately. We combined the single-ended and differential two-way power amplification to improve the output power, which will bring about the result of decreased efficiency. We improved PAE by adjusting the bias current of the power cell, reducing the DC power consumption of each channel, and making the transistor work in the deep AB region. To the authors' knowledge, PA4 with a maximum linear power of 25.2 dBm and a maximum PAE of 47.2% measured at 44 GHz is the most efficient mm-Wave CMOS power amplifier reported to date.

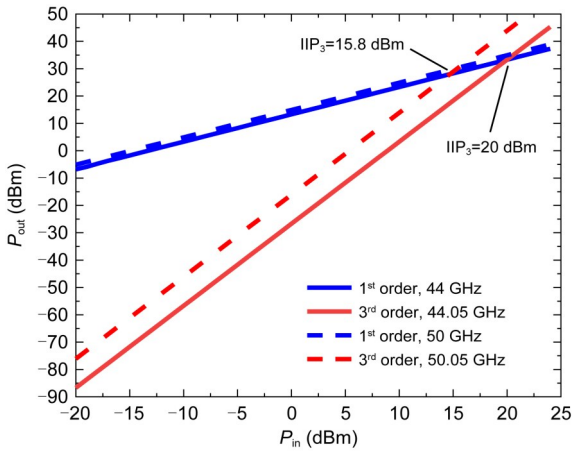

Fig. 12 IIP_3 simulation results of the differential PA4

4 Conclusions

A linearity analysis that takes into account the nonlinearities of the transistor current and capacitances is introduced. The analysis leads to calculated OIP_3 values for cascode and triple cascode cells (Eqs. (11) and (18), respectively). The analysis also predicts the linearity of PA1 and PA2, indicating that the designs of PA1 and PA4 based on the stacking of triple cascode cells are superior in terms of linearity. The differential power amplifier (PA4) has the best $P_{1\,dB}$ value (21.5 dBm at 44 GHz) and is better than all the single-ended power amplifiers presented here. Considering

Table 2 Comparison with state-of-the-art U-band CMOS power amplifiers

Reference	Technology	Frequency (GHz)	Gain (dB)	P_{sat} (dBm)	Peak PAE (%)	$P_{1\,dB}$ (dBm)
Chen B et al., 2014	130 nm CMOS	60	8.6	10.8	8.4	9.4
Jiang et al., 2017	90 nm CMOS	45	20.3	21.0	14.5	17.8
Vigilante and Reynaert, 2018	28 nm CMOS	43	20.8	15.9	18.4	11.1
Xia et al., 2018	45 nm CMOS SOI	57.2	15.0	18.5	25.5	16.2
Li et al., 2019	45 nm CMOS SOI	39	15.6	18.9	36.0	17.4
Park et al., 2019	28 nm CMOS	38.5	25.8	16.8	32.9	14.9
Wang CW et al., 2020	28 nm CMOS	41	17.6	14.7	26.2	13.0
Mayeda et al., 2021	22 nm FD-SOI	37	10.9	17.1	21.7	16.6
This work	45 nm CMOS SOI	44	11.4	25.2	47.2	21.5
		50	12.8	24.2	26.1	19.3

the troublesome testing process of the differential structure, we will find a way to design a differential-to-single-ended balun to synthesize two paths of power to facilitate testing.

Contributors

Jie CUI designed the research. Peipei LI and Weixing SHENG processed the data. Jie CUI drafted the paper. Weixing SHENG and Peipei LI helped organize the paper. Jie CUI, Peipei LI, and Weixing SHENG revised and finalized the paper.

Compliance with ethics guidelines

Jie CUI, Peipei LI, and Weixing SHENG declare that they have no conflict of interest.

Data availability

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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