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Low-power, high-speed, and area-efficient sequential circuits by quantum-dot cellular automata: T-latch and counter study*

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Abstract: Quantum-dot cellular automata (QCA) is a new nanotechnology for the implementation of nano-sized digital circuits. This nanotechnology is remarkable in terms of speed, area, and power consumption compared to complementary metal-oxide-semiconductor (CMOS) technology and can significantly improve the design of various logic circuits. We propose a new method for implementing a T-latch in QCA technology in this paper. The proposed method uses the intrinsic features of QCA in timing and clock phases, and therefore, the proposed cell structure is less occupied and less power-consuming than existing implementation methods. In the proposed T-latch, compared to previous best designs, reductions of 6.45% in area occupation and 44.49% in power consumption were achieved. In addition, for the first time, a reset-based T-latch and a T-latch with set and reset capabilities are designed. Using the proposed T-latch, a new 3-bit counter is developed which reduces 2.14% cell numbers compared to the best of previous designs. Moreover, based on the 3-bit counter, a 4-bit counter is designed, which reduces 0.51% cell numbers and 4.16% cross-section area compared to previous designs. In addition, two selective counters are introduced to count from 0 to 5 and from 2 to 5. Simulations were performed using QCADesigner and QCAPro tools in coherence vector engine mode. The proposed circuits are compared with related designs in terms of delay, cell numbers, area, and leakage power.

Key words: Quantum-dot cellular automata (QCA); Quantum-dot; T-latch; T-flip-flop; Counter; Selective counter; QCADesigner; QCAPro

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1 Introduction

In recent years, quantum-dot cellular automata (QCA) has attracted a great deal of interest among researchers due to the growing demand for nano-sized computers (Fazili et al., 2022). At this size, the QCA has a significant advantage over conventional integrated circuits such as complementary metal-oxide-semiconductor (CMOS) technology. As the size of the components decreases in QCA, the efficiency increases. That means there is a direct relationship between size and efficiency whereas size reduction in CMOS will result in reduced efficiency (Ahmadpour et al., 2022). It may not yet be clear whether this technology can replace CMOS, but the designs and modeling show that QCA has many benefits that CMOS lacks. Compared to QCA circuits, CMOS circuits occupy a very large area and their power consumption is much higher. This is why QCA with its unique characteristics is considered a great development in the field of computer science and logic circuits. QCA is much smaller than CMOS, and the dimensions of the QCA cell can even be implemented at the order of molecules or atoms. QCA has very

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low power consumption compared to CMOS because there is no current or output capacitor in the circuit. Research indicates that the operating frequency of QCA will be in the range of terahertz waves. In addition, many of the barriers to QCA manufacturing are being addressed. The simple form of QCA design is very attractive. QCA topologies differ from conventional logic circuits, so new ideas for converting standard logic units into equivalent QCA circuits are needed (Akbari-Hasanjani and Sabbaghi-Nadooshan, 2022).

Latches and flip-flops are integral parts of a processor. T-type latches and flip-flops are also the most important type of circuits between conventional latches and flip-flops, and have many applications in the design of digital circuits, especially counters (Gholami and Amirzadeh, 2023). In the past, some designs for T-latches and T-flip-flops (TFF) have been introduced into QCA technology, each of which has its advantages and disadvantages. For example, the scheme proposed by Angizi et al. (2015), besides having many cells and a cross-section area, also has high latency and power consumption. The design proposed by Rad and Heikalabad (2017) mitigates all the above problems but the absence of set and reset terminals is one of the weaknesses of this latch. Also, although the design proposed by Majeed et al. (2019) has much improvement over the proposed designs, this is at the cost of high power consumption. In addition, another weakness of this latch structure is the absence of set and reset functions in the final circuit.

Amirzadeh and Gholami (2019) proposed a 3-bit counter using D-flip-flop (DFF), which, despite its good performance, has a large number of cells and a relatively high level of area and delay. Also, Majeed et al. (2019) proposed a TFF-based counter, which, despite its improvement in occupied area and delay, has a large number of cells. In addition, none of the above-mentioned counters are capable of specific counts (such as counting from 2 to 5) due to the lack of set and reset terminals. Zoka and Gholami (2018) proposed a DFF-based counter with reset capability which has many cells, high level of cross-section area and delay. Therefore, we propose a new T-latch and TFF with set and reset terminals with low cell number, small occupied cross-section area, and low delay in this paper. In addition, using the proposed T-latch and TFF, counters with common and specific counts are presented.

2 Fundamentals of QCA technology

QCA is an emerging technology that is recognized as one of the top six technologies in the future of computers (Akbari-Hasanjani et al., 2021). A QCA cell is composed of four quantum dots at four corners. Within each cell, there are two free electrons that can be tuned to adjacent points by tunneling (Dehbozorgi et al., 2022a). Due to the coulomb repulsion between the electrons, they tend to be spaced, so they occupy the corners of a square cell as is illustrated in Fig. 1.

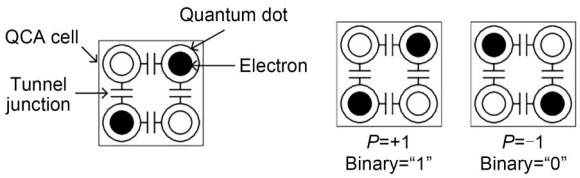

Fig. 1 QCA cellular polarity

To create any digital logic, basic elements are needed to implement the logic. These elements include wire, NOT, AND, OR, and majority gates. Majority and NOT gates are two important gates in QCA logic that are used as basic gates (Nafees et al., 2022). The three-input majority gate consists of three inputs and one output, and will be the basis for the design of many of the more complex QCA gates. The function of this gate is to select the output with the highest number from the three inputs in each case. Also, using the majority gate, two important gates (AND and OR) are made. For example, if the polarity of one of the inputs is set to "0," the AND gate is made, and if the polarity of one of the inputs is set to "1," the OR gates will be made from the majority gate (Bahar and Wahid, 2022). NOT gates are another important and basic gate in QCA logic. In QCA, for a signal to be inverted, the cells are tilted up or down in respect to the input cell (Khan and Arya, 2022). Another important element needed to design circuits in QCA technology is wire; this is formed by placing cells in a series.

Clocks in QCA are used to control the movement of electrons inside the cells. In fact, the clock controls how data are transmitted in QCA cells from inputs to the outputs (Akbari-Hasanjani et al., 2022). This allows the clock to coincide in different parts of the circuit. As shown in Fig. 2, each clock has four zones: switch, hold, release, and relax (Dehbozorgi et al., 2022b).

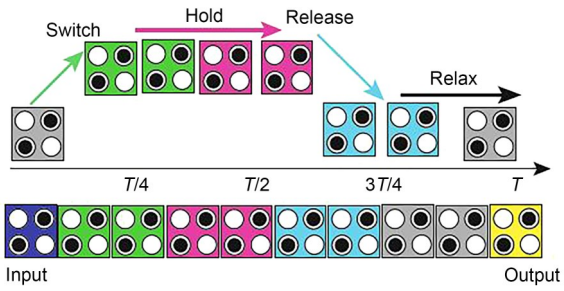

Fig. 2 Clock zones in QCA circuits

3 Proposed T-latch in QCA

Latches are the essential elements of digital logic circuits (Gholami et al., 2022). Unlike many logic gates, latches use feedback to create a circuit (Kalyan et al., 2022). For this reason, these circuits are called sequential circuits. T-latch is one of the most important types of latch. In this latch, if clock is logical zero and also in a case when *T*="0" and Clock="1," the output will be the same as the previous state, and if *T*="1" with the clock as logical one, the output will be the opposite of the previous state. Since TFFs can be made from T-latches using a level-to-edge converter circuit, this section will first examine the design of T-latches.

The proposed T-latch consists of an AND gate and an XOR gate (Fig. 3a). The circuit works as follows: when Clock="0" and for any value of *T*, the output of the circuit retains its previous state. Also, when Clock="1" and *T*="0," the output of the AND gate is zero, and the circuit's output retains its previous state; when both the clock and *T* are logical one, the output of the AND gate will be logical one, and the output of the circuit will be toggled.

Fig. 3b shows the layout of the proposed T-latch comprising 21 QCA cells, 0.0174 μm^2 area, 0.75 clock cycle delay, and 16.22 meV power consumption. The proposed structure is designed according to the pattern in Fig. 3a and the output is available in clock 2. The XOR gate in this design is used from Abutaleb (2018a). All design rules are checked and used to design the proposed circuit (Kim et al., 2005).

Fault analysis is performed for the T-latch structure by considering a single cell missing and addition defects. The layout of the T-latch structure shown in Fig. 4 is used for fault analysis. The cell missing defect is possible for the cells 5, 9, 14, 15, 20, 24, 25, 26, 27, 28, 30, 31, 35, 37, 38, and 39, while the cells

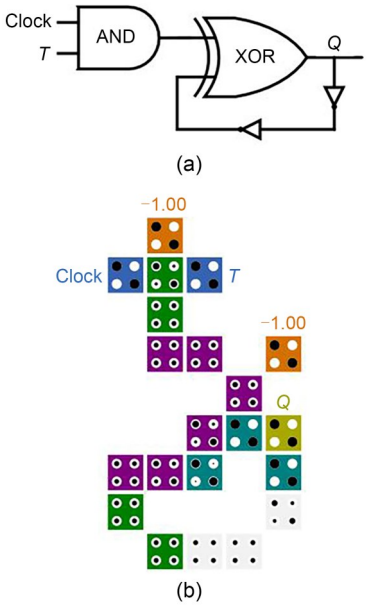

Fig. 3 Logical diagram (a) and layout (b) of the proposed T-latch in QCA

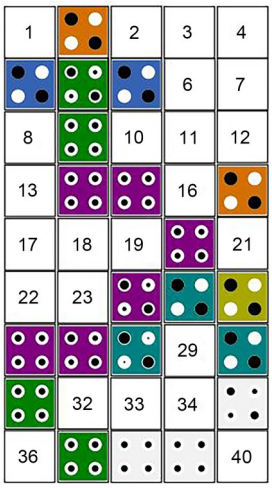

Fig. 4 Fault analysis for T-latch

1, 2, 3, 4, 6, 7, 8, 10, 11, 12, 13, 16, 17, 18, 19, 21, 22, 23, 29, 32, 33, 34, 36, and 40 cause cell addition defects. It is assumed that input and output cells are unchanged in any type of fault defect. The actual output for the T-latch structure is 01000110111. The faults are calculated by matching the actual output with the defect outputs for the different cells. Table 1 presents the faults due to a single cell missing and addition defects.

Table 1 shows that the total faults are 117 out of 440 bits. It shows a 73.40% fault-aware design.

Table 1 Fault calculation for T-latch

Cell	Output (actual=01000110111)	Fault
1	01000110111	0
2	01000110111	0
3	01000110111	0
4	01000110111	0
5	00000000001	5
6	01000110111	0
7	01000110111	0
8	01000110111	0
9	11111111111	5
10	01001001000	7
11	01000110111	0
12	01000110111	0
13	01000110111	0
14	11111111111	5
15	11111111111	5
16	00000000000	6
17	01000110111	0
18	10011010011	6
19	01101101101	5
20	01010101010	5
21	10011010011	6
22	01000110111	0
23	00000000000	6
24	10111010111	6
25	00000000000	6
26	01100101100	5
27	01100101100	5
28	10101010101	6
29	01000110111	0
30	01000110111	0
31	00000000000	6
32	11111111111	5
33	01000110111	0
34	01000110111	0
35	01000110111	0
36	01000110111	0
37	00000000000	6
38	00000000000	6
39	01100101100	5
40	01000110111	0

Since the purpose of this paper is to design the counters in QCA technology, and in some of the counters the TFF needs a reset terminal, a TFF with reset pin is also proposed. Fig. 5a shows the logical diagram of the proposed TFF with reset terminal. As can be seen, for R="0," the output of AND2, which is also the flip-flop's output, should be zero. Based on this figure, the output function of proposed design is:

$$Q(t) = R.[\mathrm{CLK}.T \oplus Q(t-1)], \quad (1)$$

where T, R, CLK, $Q(t)$, and $Q(t-1)$ are T input, reset input, clock input, circuit output, and previous state of output, respectively. According to Eq. (1), when R="1," the TFF works at its normal state. For example, when Clock="0," the output holds the previous state $Q(t)=Q(t-1)$, and for Clock="1," the output will be inverted for T="1" and the same as the previous state for T="0." Also, when R="0," the output will be zero.

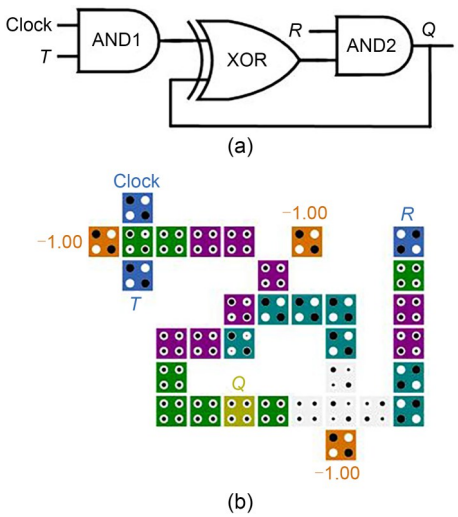

Fig. 5 Logical diagram (a) and layout (b) of the proposed T-latch with reset input in QCA

Fig. 5b shows the proposed T-latch with reset input in QCA. The design has 33 cells, 0.03 μm^2 area, 1.25 clock cycle delay, and 19.01 meV power consumption. The proposed layout consists of two AND gates and one XOR gate according to the logical diagram of Fig. 5a, and the output is available in clock 3.

In some cases, it is also necessary to count specific numbers (such as counting from 2 to 5). In these cases, the flip-flop needs set and reset inputs. The logical diagram is shown in Fig. 6a. Given this logical diagram, the output relation will be (according to the output function of a majority gate)

$$Q(t) = \overline{R}.S + \overline{R}.[\mathrm{CLK}.T \oplus Q(t-1)] + S.\overline{R}.[\mathrm{CLK}.T \oplus Q(t-1)], \quad (2)$$

where S is set input. According to Eq. (2), when S=R="0," the circuit operates like a normal TFF whose output

function is $Q(t)=\overline{R}.[\mathrm{CLK}.T\oplus Q(t-1)]$. Also, when S="1" and R="0," the output is logical one. When S="0" and R="1," the output will be logical zero. Note that the above structure is designed in such a way that when set and reset inputs are activated simultaneously, priority is with set, and output will be in logical one state. The proposed T-latch with set and reset inputs in QCA is shown in Fig. 6b. As can be seen, this circuit consists of 39 QCA cells, 0.035 μm^2 area, 1.25 clock cycle delay, and 22.66 meV power consumption.

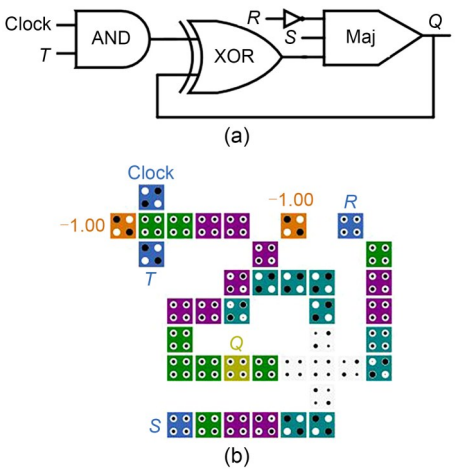

Fig. 6 Logical diagram (a) and layout (b) of the proposed T-latch with set and reset inputs in QCA

Since the latches are sensitive to the clock level and the flip-flops are sensitive to the clock edges, circuits for converting latches to flip-flops have been introduced in Hashemi and Navi (2012). In this paper, these converters are also used to convert latches into flip-flops in the proposed structures.

In the following sections, to illustrate the application of the proposed T-latch in more complex circuits and to show that the designed circuits work correctly in complex circuits, each of the structures will be used in a counter design.

4 Design of the proposed counters in QCA nanotechnology

Counters are circuits that store and display the frequency of an event. This circuit can accurately count and control the number of products. Counters are the most popular circuits in processors and come in many types, such as asynchronous counters, synchronous counters, ring counters, and Johnson counters. A common n-bit counter counts from 0 to 2^n-1. In this section, the proposed designs are used to implement the counters.

Fig. 7 shows a logical diagram of a common 3-bit counter based on a TFF that can count from 0 to 7. A counter that can correctly count numbers is designed in QCA using TFF with the lowest cell number, cross-section area, and power consumption. For this purpose, the proposed simple T-latch scheme is used in this format and the proposed layout is shown in Fig. 8. The proposed 3-bit TFF-based counter consists of 137 QCA cells, 0.16 μm^2 area, and 2 clock cycle delay. The proposed structure consists of three T-latches, a level-to-edge converter, and an AND gate, which are designed in tandem according to Fig. 7.

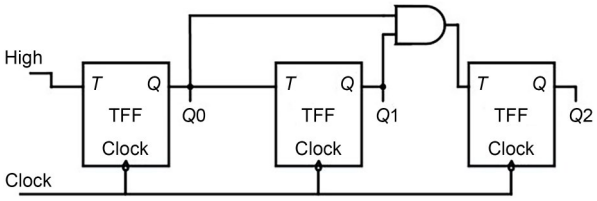

Fig. 7 Logical diagram of a 3-bit counter

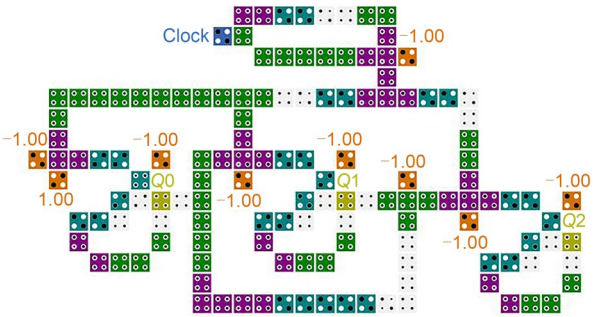

Fig. 8 Layout of the proposed 3-bit counter in QCA technology

Also, in this paper, a common 4-bit counter that counts from 0 to 15 is designed. The logical diagram and layout in QCA technology are illustrated in Figs. 9 and 10, respectively. As can be seen from Fig. 10, the

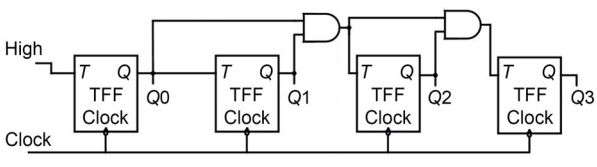

Fig. 9 Logical diagram of a 4-bit counter

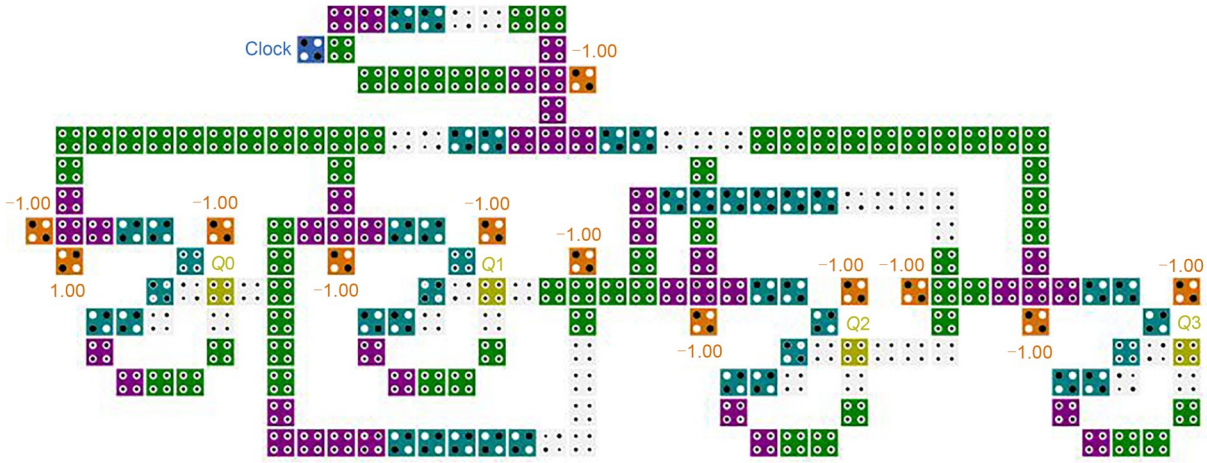

Fig. 10 Layout of the proposed 4-bit counter in QCA technology

proposed 4-bit counter structure in QCA technology consists of 195 cells, 0.23 μm^2 area, and 2 clock cycle delay. The proposed structure consists of four T-latches, a level-to-edge transducer, and two AND gates, which are designed according to Fig. 9.

To show the correct performance of the proposed T-latch with reset input in QCA technology, a counter is designed for specific numbering. For example, a circuit can be made to count from 0 to 5 and after counting number 5, reset will be activated and the circuit will start counting again from 0. Fig. 11 shows the logical diagram of the proposed selected counter that counts from 0 to 5.

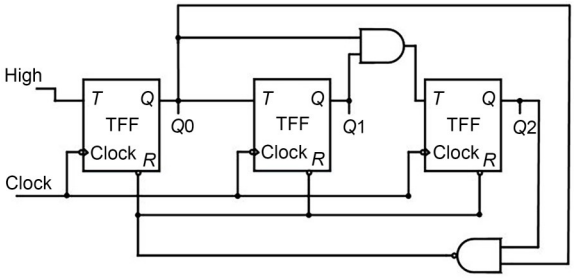

Fig. 11 Logical diagram of the proposed counter, which can count from 0 to 5

To correctly count from 0 to 5, the circuit will automatically reset correctly and start counting again from 0 after counting the number 5. The circuit logical diagram is designed as follows. The outputs of the first and third flip-flops are NAND, and then the output of the NAND gate is directly connected to all the reset inputs of flip-flops. With this logical diagram, this circuit starts counting from 0 to 5, and then counts again from 0.

Fig. 12 shows the 3-bit optional counter structure in QCA technology, which consists of 287 cells, 0.34 μm^2 area, and 2.5 clock cycle delay. The proposed structure consists of three proposed reset-based T-latches, a level-to-edge converter, and an NAND gate designed according to Fig. 11.

In addition, having both set and reset inputs for the T-latch enables the designer to design counters so that the beginning and end of the number count are other than 0 and 2^n-1. That is, a counter can be designed to selectively count the numbers. For example, a circuit that can count from 2 to 5 can be designed. Fig. 13 shows the proposed logical diagram of a selected midpoint counter that counts from 2 to 5. In this design, the proposed circuit can count from 2 to 5, and then after number 5, it can automatically operate set and reset functions and start counting again from 2. Since the set and reset inputs of the proposed flip-flops are highly active, the outputs of the first and third flip-flops are applied to an AND gate, and then the output of the AND gate enters the first and third flip-flops, and resets is applied to the set input of the second flip-flop. With this logical diagram, the counter can count from 2 to 5 correctly.

Fig. 14 shows the proposed 3-bit optional mid-range counter in QCA technology, which can count from 2 to 5. The proposed design consists of 295 QCA cells, 0.37 μm^2 area, and 2.5 clock cycle delay. The proposed structure consists of three proposed T-latches with set and reset inputs, a level-to-edge transducer, and an AND gate based on the structure in Fig. 13.

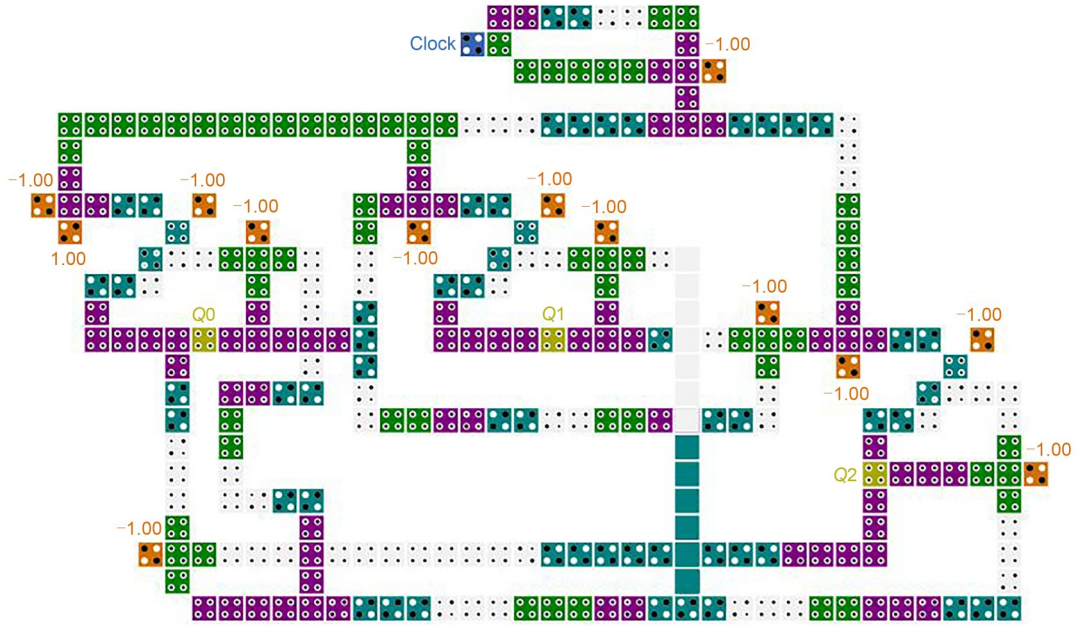

Fig. 12 Layout of the proposed counter, which can count from 0 to 5

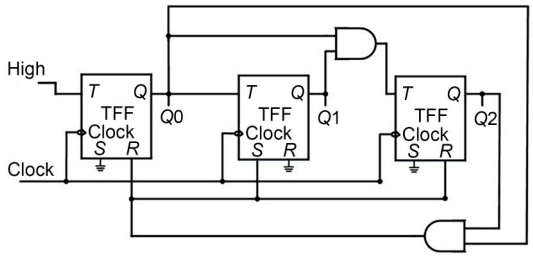

Fig. 13 Logical diagram of the proposed counter, which can count from 2 to 5

5 Simulations and results

In this section, simulations of the proposed circuits are performed using the QCADesigner tool in coherence vector engine mode, and these simulations show the accuracy of the circuit's performance. Coherence vector engine parameters are shown in Table 2.

Fig. 15a shows the simulation results of the proposed T-latch. When Clock="1" and *T*="0," the output retains its previous state; when Clock="1" and *T*="1," the output reverses its previous state. Also, when Clock='0' (for any value of the *T* input), the output retains its previous state. All these conditions are shown in Fig. 15a.

Fig. 15b shows the simulation results of the proposed reset-based T-latch in QCA technology. The output keeps its previous state when Clock="0," independent of the *T* value. Also, when Clock=*T*="1," the output reverses its previous state. When Clock="1" and *T*="0," the output will hold its previous state. In addition, for active reset, whether for any value of the input, the output is logical zero.

Fig. 16 illustrates the simulation results of the proposed T-latch which has both set and reset terminals. When Clock="1" and *T*="0," the output retains its previous state; when Clock=*T*="1," it reverses its previous output state; when Clock="0," independent of the *T* input, the output will retain its previous state. Also, when the reset of the circuit is activated, whether the input is logical one or zero, the output will be logical zero; when the set input is activated, whether *T* input is logical one or zero, the output will be logical one. Note that in the proposed structure, when both set and reset are activated, whether the input is logical one or zero, priority is with set input, and the output will be logical one.

Fig. 17 shows the simulation results of the proposed 3-bit counter in QCA technology, in which the proposed 3-bit counter correctly counts from 0 to 7.

Fig. 18 shows the simulation results of the proposed 4-bit counter in QCA technology. Note that the circuit correctly counts from 0 to 15. Considering the initial values of the flip-flop outputs, the counting starts from 12 and then the counting process continues from 0.

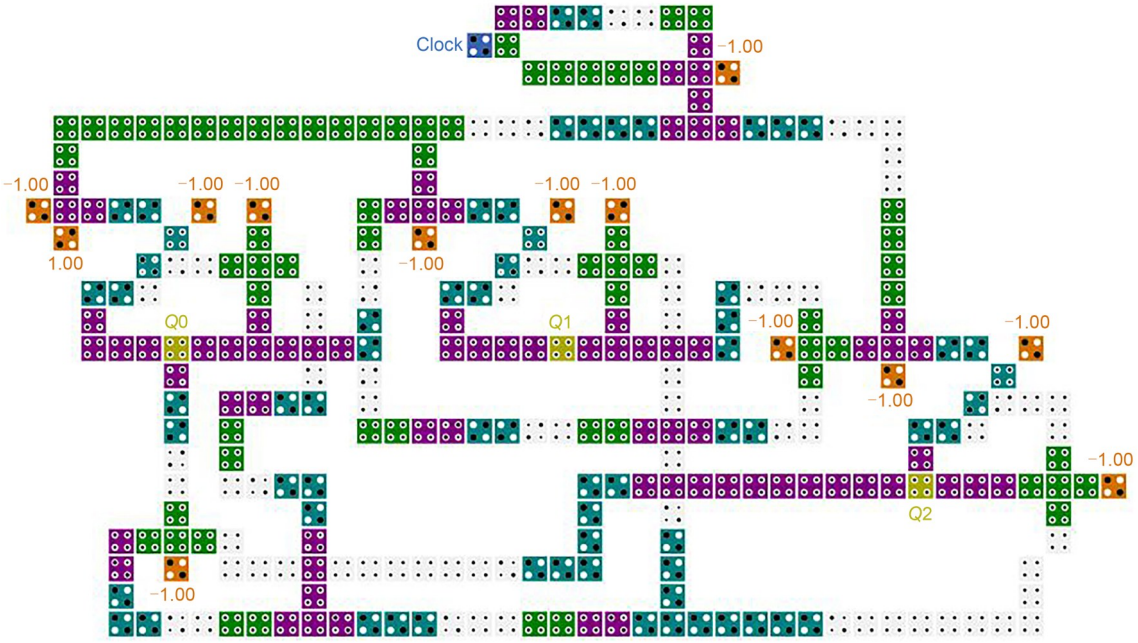

Fig. 14 Layout of the proposed counter in QCA technology which can count from 2 to 5

Table 2 Coherence vector engine parameters

Parameter	Value
Cell size	18 nm×18 nm
Dot diameter	5 nm
Center-to-center distance	20 nm
Temperature	1.000 000 K
Relaxation time	1.000 000e-015 s
Time step	1.000 000e-016 s
Total simulation time	7.000 000e-011 s
Clock high	9.800 000e-022 J
Clock low	3.800 000e-023 J
Clock shift	0.000 000e+000
Clock amplitude factor	2.000 000
Radius of effect	80.000 000 nm
Relative permittivity	12.900 000
Layer separation	11.500 000 nm

Simulation results of the proposed selective counter (counting from 0 to 5) with the proposed T-latch with reset input in QCA technology are shown in Fig. 19. The proposed structure would have to count from 0 to 5, which confirms the accuracy of the proposed selective counter performance.

Fig. 20 shows the simulation results of the proposed intermediate counter in QCA technology for counting from 2 to 5. This figure also confirms the behavioral accuracy of the circuit.

Table 3 shows the comparison of the proposed T-latch designs with other similar circuits in QCA technology. As can be seen, the proposed structure is superior in terms of cell number, cross-section area, and delay. In addition, the proposed circuit as a T-latch has set and reset capabilities (which have not been seen in previous works).

Table 4 shows the comparison of the proposed counter designs with other similar designs in QCA technology. Due to the capability of the set and reset in the proposed scheme, the counter designed in this paper has the capability to count mid-number, which was not available in previous papers. In addition to having set and reset inputs, the proposed structures have more superior performance in terms of the number of used cells, the level of area occupation, and the delay rate compared to previous works. Note that some of the designs did not use the design rules of QCA which were reported in Kim et al. (2005).

The proposed circuits are examined in terms of cost. The cost formula is Cost=$(M^K+I+C^L)D^P$, where M is the number of gates, I is the number of inverters, C is the number of intersections, D is the delay value, and K, L, and P are given ones. The cost value of the proposed circuit increases due to the larger number of inverters compared to the best circuit (Majeed et al., 2019). Since the purpose of this paper is to reduce the

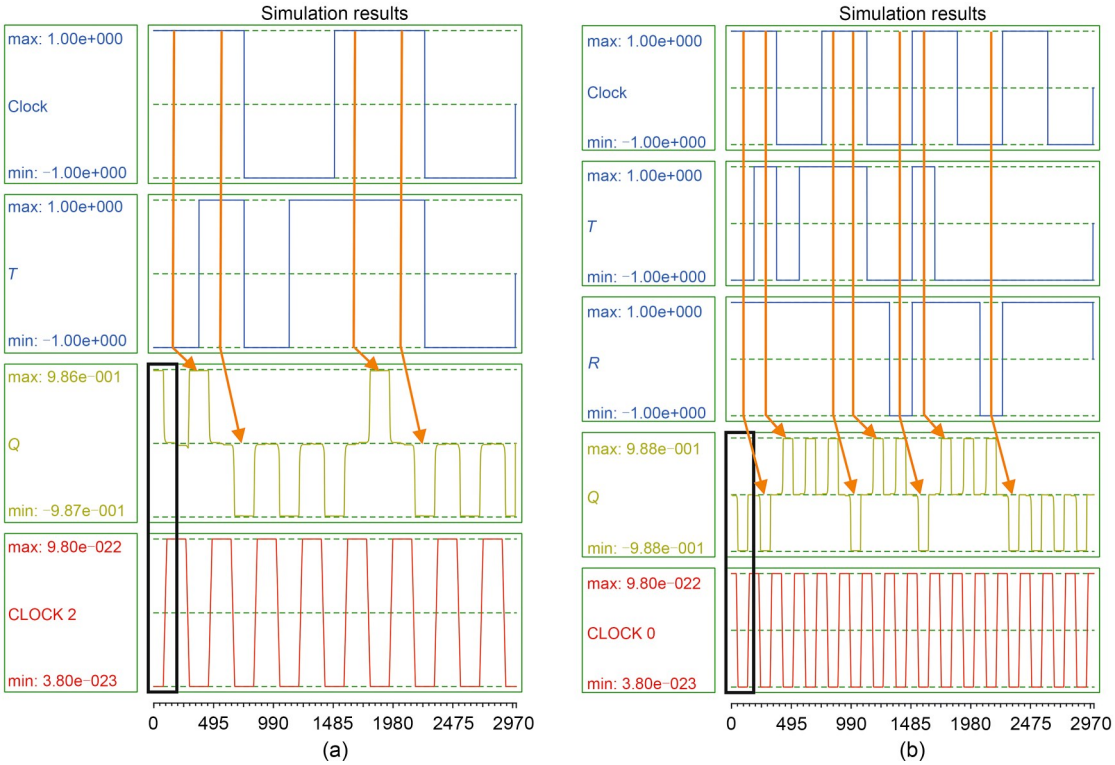

Fig. 15 Output of the proposed T-latch (a) and reset-based T-latch (b)

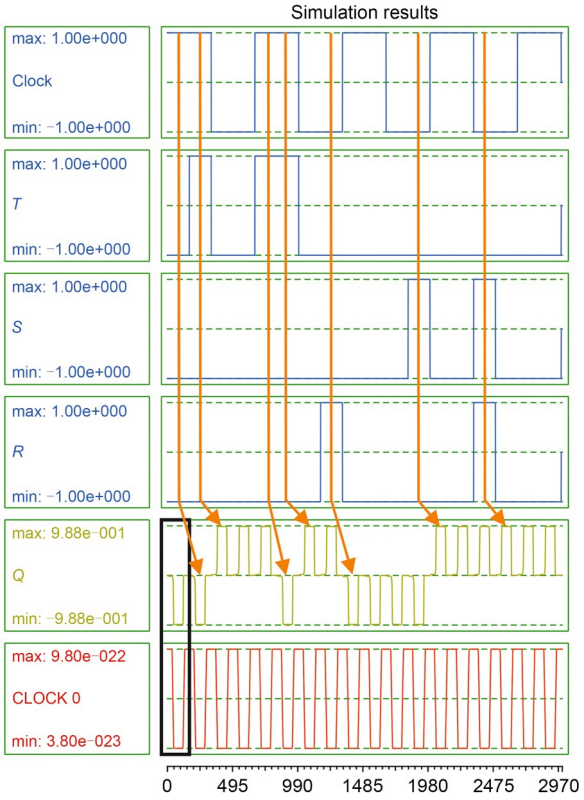

Fig. 16 Output of the proposed T-latch with set and reset inputs

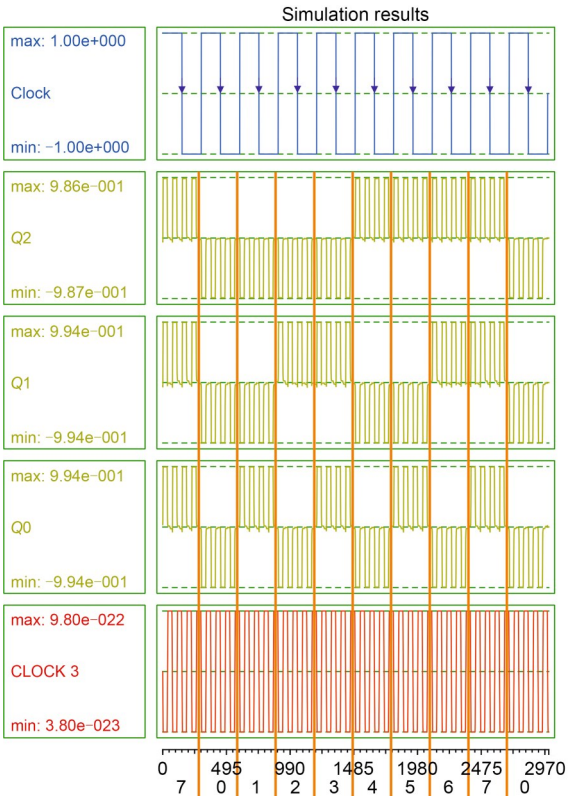

Fig. 17 Output of the proposed 3-bit counter in QCA nanotechnology

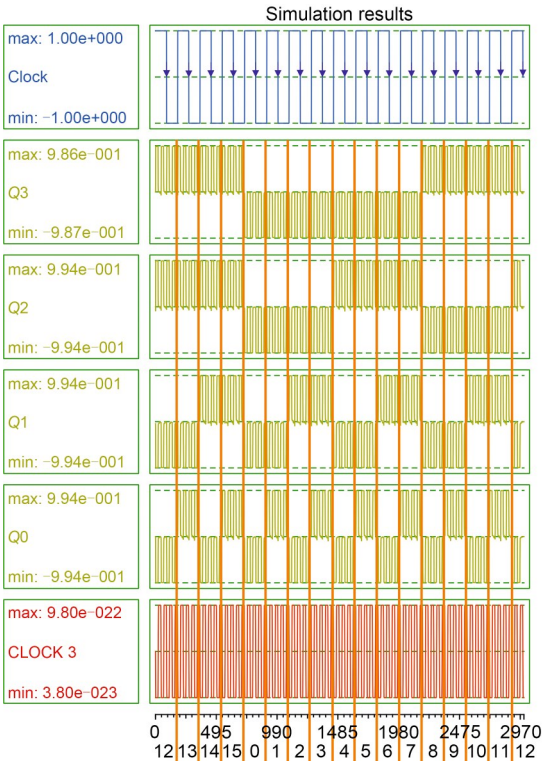

Fig. 18 Output of the proposed 4-bit counter in QCA nanotechnology

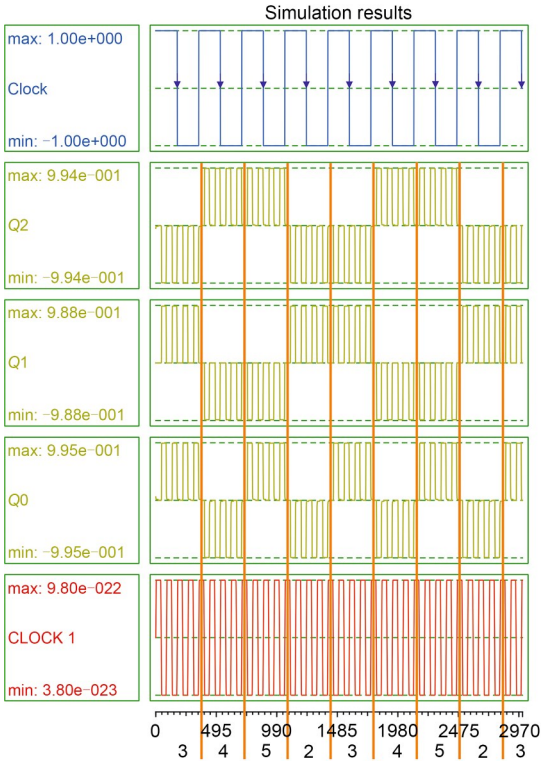

Fig. 20 Output of the proposed selective counter in QCA, which can count from 2 to 5

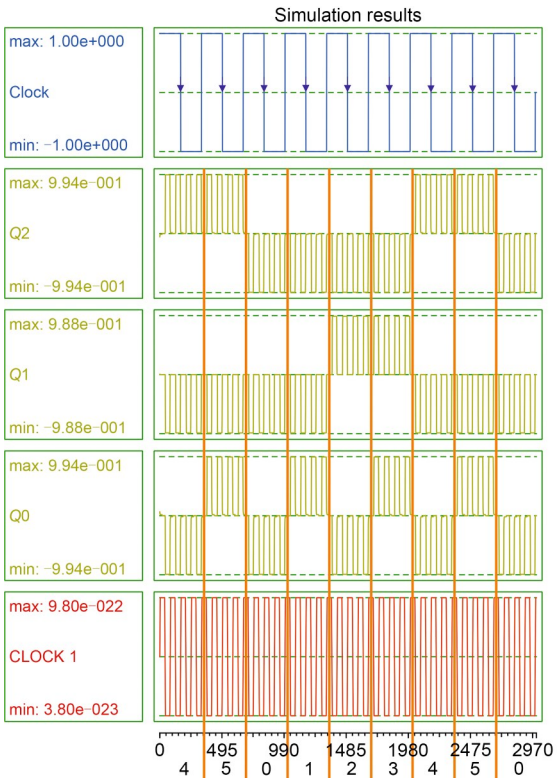

Fig. 19 Output of the proposed selective counter in QCA technology, which can count from 0 to 5

number of cells, occupied area, and energy consumption, and thus to show that the proposed circuits have better performance than the previous designs, a new cost formula is reported as New Cost=Cost×Area×Energy, which includes cost, area, and energy consumption. As can be seen from Tables 3 and 4, in terms of the newly defined cost, the proposed circuits have much better performance than the previous ones.

Various studies show that energy dissipation in QCA is very important. To evaluate energy dissipation, energy estimation software, called QCAPro, is used in QCA. This software divides all energy dissipation in the QCA circuit into two parts, leakage energy and switching energy (Abutaleb, 2018b). Losses that occur during the signal transfer from one clock to another will result in leakage energy, and losses associated with the initial switching of cells will result in switching energy. In the following, all the proposed schemes are examined by considering three different tunneling levels (0.5Ek, 1.0Ek, 1.5Ek) at a temperature of 2 K. The general formula for calculating energy loss is as follows, and all the relationships related to the calculation of energies are given in Torres et al. (2018).

Table 3 Comparison of the proposed designs and others

Reference	Cell number	Area (μm^2)	Latency ($\times 10^{-12}$ s)	Total energy dissipation at 0.5Ek (meV)	Cost	New Cost	Set input	Reset input
Bhavani and Alinvinisha (2015)	67	0.08	1.25	–	–	–	No	No
Torabi (2011)	66	0.06	1.25	88.72	–	–	No	No
Dutta and Mukhopadhyay (2014)	58	0.06	1.25	–	7.5	–	No	No
Angizi et al. (2014)	55	0.06	1.5	55.46	–	–	No	No
Angizi et al. (2015)	46	0.06	1	31.36	4.5	8.46	No	No
Rad and Heikalabad (2017)	23	0.03	0.5	30.87	3.75	3.47	No	No
Majeed et al. (2019)	21	0.0186	0.75	29.22	2.25	1.22	No	No
Fig. 3b	21	0.0174	0.75	16.22	3.75	1.05	No	No
Fig. 5b	33	0.03	1.25	19.01	5	2.85	No	Yes
Fig. 6b	39	0.035	1.25	22.66	5	3.96	Yes	Yes

Table 4 Comparison of the proposed counters with previous related designs in QCA technology

Reference	Counting number	Cell number	Area (μm^2)	Latency ($\times 10^{-12}$ s)	Cost	New Cost	Type of sensitivity	Latch type
Bhavani and Alinvinisha (2015)	0–7	244	0.33	4.25	–	–	Level	T
Angizi et al. (2015)	0–7	238	0.36	2.25	–	–	Falling	T
Amirzadeh and Gholami (2019)	0–7	174	0.20	3	81	2825.9	Falling	D
Majeed et al. (2019)	0–7	140	0.16	2	24	1209.6	Falling	T
Fig. 8	0–7	137	0.16	2	36	1130.5	Falling	T
Amirzadeh and Gholami (2019)	0–15	258	0.25	4	144	6801.4	Falling	D
Majeed et al. (2019)	0–15	196	0.24	2	32	3295.6	Falling	T
Fig. 10	0–15	195	0.23	2	46	3080.1	Falling	T
Zoka and Gholami (2018)	0–5	546	0.69	3	84	–	Rising	D
Fig. 12	0–5	287	0.34	2.5	42.5	–	Falling	T
Fig. 14	2–5	295	0.37	2.5	40	3821.3	Falling	T

$$E_{\text{diss}} = \frac{h}{2}\int_{-L}^{L} \boldsymbol{\Gamma}\cdot\frac{\mathrm{d}\boldsymbol{\lambda}}{\mathrm{d}t}\,\mathrm{d}t = \frac{h}{2}\left([\,\boldsymbol{\Gamma}\cdot\boldsymbol{\lambda}\,]_{-L}^{L} - \int_{-L}^{L}\boldsymbol{\lambda}\cdot\frac{\mathrm{d}\boldsymbol{\Gamma}}{\mathrm{d}t}\,\mathrm{d}t\right), \quad (3)$$

$$\boldsymbol{\Gamma} = \frac{1}{h}\,[-2\gamma, 0, \mathrm{Ek}\,(C_{j-1} + C_{j+1})\,], \quad (4)$$

where $\boldsymbol{\lambda}$ is the three-dimensional (3D) coherence vector, h is Planck's constant, and $\boldsymbol{\Gamma}$ is a 3D Hamiltonian vector. $\boldsymbol{\Gamma}$ is the vector for the atmosphere energy of the QCA cell together with the neighboring cell effects and is given in Eq. (4).

Figs. 21 and 22 illustrate the energy dissipation of the proposed T-latch structure and the proposed selective counter (which counts from 2 to 5) at the 0.5Ek level, respectively. In these figures, the darker points represent the cells at higher loss. Also, Table 5 shows the comparison between leakage, switching, and total energy loss of all the proposed designs with other related works. The method for analyzing and reporting energy dissipation in Table 5 is inspired from Sheikhfaal et al. (2015).

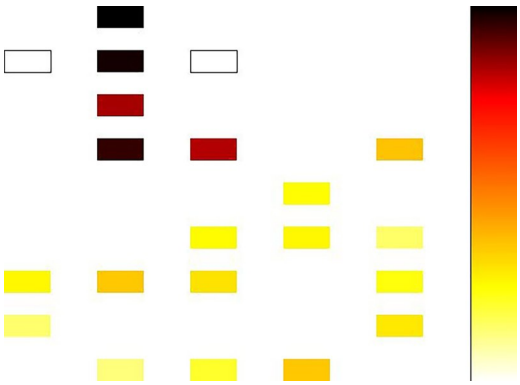

Fig. 21 Energy diagram of the proposed T-latch

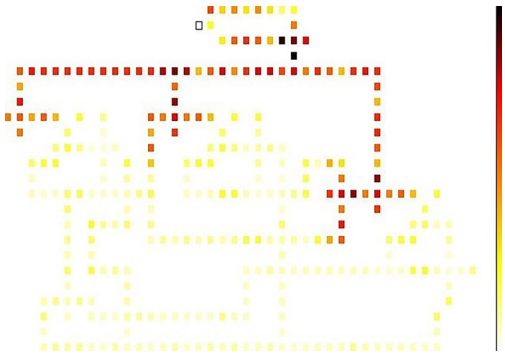

Fig. 22 The energy dissipation map of the proposed selective counter which counts from 2 to 5

Table 5 Leakage, switching, and total energy dissipation comparison

Circuit	Average leakage energy dissipation (meV)			Average switching energy dissipation (meV)			Total energy dissipation (meV)		
	0.5Ek	1.0Ek	1.5Ek	0.5Ek	1.0Ek	1.5Ek	0.5Ek	1.0Ek	1.5Ek
Fig. 3b	8.36	22.16	36.89	7.86	6.60	5.42	16.22	28.76	42.31
Fig. 5b	11.82	31.73	53.34	7.19	5.94	4.88	19.01	37.67	58.22
Fig. 6b	13.43	36.07	60.68	9.23	7.62	6.35	22.66	43.69	67.03
Fig. 8	48.05	136.57	235.27	148.22	128.31	109.67	196.27	264.88	344.94
Fig. 10	69.93	194.35	336.63	221.19	191.76	162.93	291.12	386.11	499.56
Fig. 14	96.86	281.29	497.09	161.34	138.73	119.26	258.20	420.02	616.35

6 Conclusions

In this research, we have discussed the principles of quantum cell design. Also, simple and useful designs of T-latches, T-latches with reset input, and T-latches with set and reset inputs have been presented. In addition, a level-to-edge converter has been used for clock of T-latches which leads to TFF topologies. We have also designed, with the help of the suggested flip-flops, a 3-bit counter, a 4-bit counter, a 0–5 selective counter, and a 2–5 intermediate selective counter. All the designs have been simulated using QCADesigner and QCAPro to validate their performance. The designs have also been compared in terms of number of cells, occupied area, delay, and energy dissipation.

Contributors

Mohammad GHOLAMI designed the research. Zaman AMIRZADEH processed the data and drafted the paper. Mohammad GHOLAMI revised and finalized the paper.

Compliance with ethics guidelines

Mohammad GHOLAMI and Zaman AMIRZADEH declare that they have no conflict of interest.

Data availability

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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