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Digital-to-analog converter free architecture for digital reconfigurable intelligent surface*

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Abstract: This research investigates the digital-to-analog converter (DAC) free architecture for the digital reconfigurable intelligent surface (RIS) system, where the transmission lines are implemented for reflection coefficient (RC) control to reduce power consumption. In the proposed architecture, the radio frequency (RF) switch based phase shifter is considered. By using a single-pole four-throw (SP4T) switch to simultaneously control the RCs of a group of elements, a 2-bit phase shifter is realized for passive beam steering. A novel modulation scheme is developed to explore the cost effectiveness, which approaches the performance of traditional quadrature amplitude modulation (QAM). Specifically, to overcome the limitation of the phase shift bits, joint frequency-shift and phase-rotation operations are applied to the constellation points. The simulation and experimental results demonstrate that the proposed architecture is capable of providing an ideal transmission performance. Moreover, 64- and 256-QAM modulation schemes could be implemented by expanding the elements and phase bits.

Key words: Reconfigurable intelligent surface; Hardware implementation; High-order modulation
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1 Introduction

A reconfigurable intelligent surface (RIS) employs numerous passive elements to reflect or transmit the incident signal, and is capable of regulating the channel and significantly increasing the achievable rate in complex electromagnetic environments (Liu YW et al., 2021; Yuan et al., 2021). Typically, bias voltage and varactor diodes are used to form the reflection coefficients (RCs) dispersing with signal-generating components. Moreover, metamaterials (Cui et al., 2017; Varamini et al., 2018) or metal materials are used as constituents for the reflective structure to regulate the direction of incident signals. Owing to the potential benefits of multiple paths generated by the large-scale elements, RIS structure tends to exhibit considerable potentiality in wide-area coverage (Zeng et al., 2021) and terahertz communication (Wan et al., 2021). Hence, it has been widely recognized as a hinge technology in next-generation wireless communication. Given that it is an emerging technology and has several unique characteristics that enable to save costs, theoretical background underlying the formulation and implementation of RIS systems has recently been

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attracting widespread interest, as has their hardware implementation (Hu et al., 2018; Basar, 2019; Taha et al., 2021). Specifically, in Sanchez et al. (2019), Luo et al. (2021), and Nguyen et al. (2021), the advantages of RIS systems have been demonstrated in terms of spectral efficiency improvement, anti-eavesdropping, and interference elimination. Hybrid beamforming algorithms were conceived for RIS communications to provide high-performance gains (Di et al., 2020; Ying et al., 2020). Furthermore, cascaded channel estimation methods were developed in Kundu and Mckay (2021) and Chen J et al. (2023), exhibiting low computational complexity. Simultaneously, RIS systems have appealing advantages in hardware implementation, and are thus worth investigating.

The most popular hardware architectures include metamaterial-based RIS and digital RIS. The metamaterial-based RIS technique was first explicitly advocated in Minatti et al. (2015) and Du et al. (2021), where the radiation patterns of the incident signal were modified by optimizing the RC of the elements. To further improve the compactness of the miniaturized array, some variants of constructions were studied, including lens (Lou and Chen, 2021), metal (Chen DX et al., 2022), and liquid metal (Sanusi et al., 2022). In particular, a decoupling method based dual-band patch antenna was studied in Liu F et al. (2020), significantly enhancing the multi-band isolation of multi-frequency RIS systems. As a further development, varactor diodes based RIS has been incorporated in reconfigurable circuit design, which implements the electromagnetic response control of the RIS structure. Based on this, the polarization characteristics (Gao et al., 2018; Zheng et al., 2018) and channel characteristics (ElMossallamy et al., 2020) of RIS were explored. However, the electromagnetic response control of metamaterial-based RIS elements is eminently complex, which will introduce excessive computational complexity when the number of RIS elements increases.

As a parallel trend, digital RIS, which employs a field programmable gate array (FPGA) to simplify the beam design, has been advocated as a novel RIS architecture. Specifically, in digital RIS structure (Zhang L et al., 2018; Dai et al., 2021; Rajabalipanah et al., 2021), the FPGA outputs information to a digital-to-analog converter (DAC) to control the bias voltage, thereby encoding the RCs of RIS elements. It is digital RIS that enables RIS communications to exploit a high transmission rate, and the reasons were highlighted in Tang et al. (2019) for channelizing attention and resources toward this area of technology as being its advantages over simplified modulation mechanism, frequency shift keying (FSK) (Zhang XG et al., 2022), quadrature phase shift keying (QPSK) (Dai et al., 2019), and 8-phase shift keying (8-PSK). In Chen MZ et al. (2022), the 256-quadrature amplitude modulation (QAM) scheme was studied by controlling the duty cycle and delay, which can significantly increase the capacity and transmitting rate. The aforementioned digital RIS structures are designed mainly upon PIN diodes, where continuous phase shifting could be achieved by adjusting the bias voltage.

Nevertheless, the control circuits of metamaterial RIS and digital RIS, which constitute the main power consumption of the circuit, both include the combination of DAC and varactor diode. Furthermore, the power consumption of a single RIS element reaches the mW-level, with the result that the power consumption of a RIS structure reaches the W-level after the integration of hundreds of elements, a phenomenon that runs contrary to the original intention underlying passive communication. Moreover, due to the discrete signal detection scheme at the receiver, continuous phase regulation is impossible in practice. The use of a voltage grading method is the currently prevailing state-of-the-art technical recommendation for the division of different constellation points. However, the voltage regulation range is limited, resulting in a small RC distance and a high bit error rate (BER) at the receiver.

Against the above backgrounds, a novel DAC-free architecture for digital RIS is proposed. First, a low-power RC control circuit is adopted to reduce the power consumption of individual elements to the μW-level, significantly reducing the cost and energy. Furthermore, a modulation method based on discrete RCs is proposed, which simultaneously enhances the resolution of the RCs and ensures the transmission rate. However, with the raising of the frequency band, the impedance characteristics of capacitors and inductors become unstable. As a result, precise RC design remains a challenge. Addressing of the abovementioned issues constitutes the main contributions made by the present research, and these contributions are summarized as follows:

1. We propose a DAC-free architecture for digital RIS, where passive radio frequency (RF) switches are implemented to toggle between different transmission lines given the prevalence of absence of bias voltage. Consequently, the proposed architecture is capable of attaining ultra-low power consumption and hardware cost compared with traditional diode-based RIS architectures.

2. We design a novel modulation method to address the limitation of discrete phase modulation that characterizes passive RF switches, where the constellation points are multiplied through joint frequency-shift and phase-rotation operations. As a result, the same modulation order as traditional digital RIS is acquired even if the number of RCs is limited.

3. Single-pole four-throw (SP4T) switches are implemented to control a group of RIS elements with the aims of improving signal gain and reducing link costs.

4. The performance of the proposed DAC-free architecture for digital RIS as well as the modulation scheme is studied, and the results of the study verify the feasibility of the proposed system. Specifically, the BER performance of the proposed modulation method is observed to approach those of traditional QAM schemes. In practice, the proposed architecture has the ability to realize battery-free communication.

2 DAC-free digital RIS architecture

In this section, DAC-free digital RIS architecture is first introduced to reduce the hardware cost and power consumption of traditional digital RIS architectures. The design of the transmission line based passive phase shifter is characterized. A near-standard QAM scheme is portrayed to cope with the limitation of RF switches.

2.1 System structure

Fig. 1a portrays a traditional system structure of digital RIS, where the host computer generates and radiates a carrier signal to the RIS structure via universal software radio peripheral (USRP). To enhance the transmitted signal, high-gain and high-directional horn antennas are applied for both the transmitter and receiver. As a further advancement, a controller and antenna array are incorporated within the RIS structure's composition, where the FPGA supports a power module. The FPGA controls a DAC module to alter the bias voltage, thereby changing the resistor of PIN diodes and regulating the RCs.

Fig. 1b illustrates a novel DAC-free architecture, and the present researchers aim to illustrate how the digital RIS operating under this system is characterized by reduced power consumption and hardware cost compared with a traditional digital RIS. First, passive RF switches are developed for RC control. As a further advancement, the RF switches are directly controlled by the FPGA to turn on/off, eliminating the need for bias voltage. Second, each group of RIS elements is managed jointly by an RF switch, which reduces the number of RF switches required. By designing a single-pole multi-throw switch and the impedance matching networks, multi-bit RCs can easily be implemented.

To illustrate the progressiveness of the proposed architecture, the power consumption levels of active RIS, traditional digital RIS, and the proposed DAC-free RIS architecture are listed in Table 1. Specifically, active RIS refers to RIS architectures that include high-power devices such as reflectional amplifiers. Both traditional digital RIS and the proposed RIS architecture belong to passive RIS, whose power consumption is negligible compared to that of active RIS. From Table 1, we see that the power consumption of a single element of an active RIS reaches W-level, while that of traditional digital RIS is at mW-level. The proposed architecture reduces power consumption to μW-level at the expense of phase shift bits. Even as the number of RIS elements increases, the proposed architecture maintains power consumption at a low level, which indicates that subsequent to the integration of energy harvesting modules, we might expect to achieve intelligent communication in the absence of a power supply.

To further elaborate on the proposed architecture, the situation wherein the transmitter sends a single carrier is first considered. Supposing that the RIS structure contains A rows and B columns, and that the element at the a^{th} row and b^{th} column is represented by $N_{a,b}$, the coefficient of $N_{a,b}$ could then be expressed in the following form:

$$\mathit{\Gamma}_{a,b} = \gamma_{a,b}\mathrm{e}^{\mathrm{j}\theta_{a,b}}, \tag{1}$$

where $\gamma_{a,b}$ and $\theta_{a,b}$ represent the amplitude and

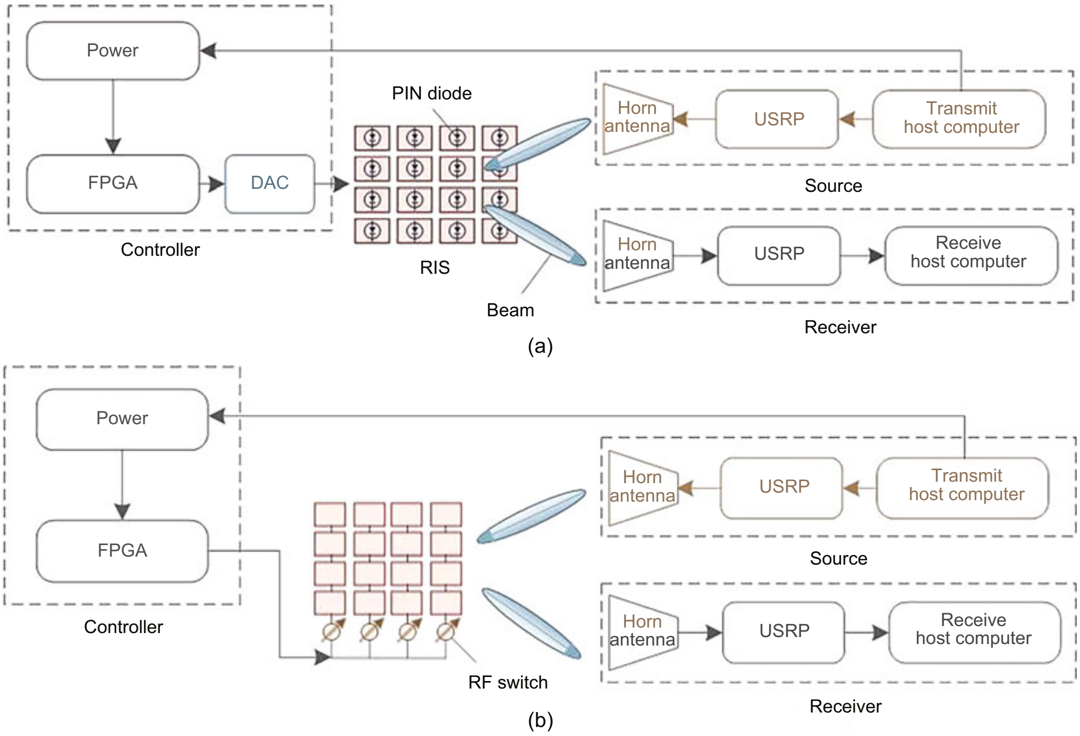


Fig. 1 System structure: (a) a traditional system structure of digital RIS; (b) the proposed DAC-free system structure of digital RIS

Table 1 Power comparison among an active RIS, a traditional passive RIS, and the proposed RIS structure

Core component	Power		
	Active	Traditional	Proposed
Patch/Metamaterial	0	0	0
DAC	1 mW	1 mW	
PIN diode	250 mW	250 mW	
RF switch			1 μW
Amplifier	1.2 W		
FPGA	300 μW	300 μW	300 μW

phase of $\mathit{\Gamma}_{a,b}$, respectively. By modifying the capacity and sensory resistance of the impedance network, the RCs could be designed properly. Commonly, the phase matrix of the RIS structure is assumed to be a diagonal matrix $\boldsymbol{\Theta} \in \mathbb{C}^{AB\times AB}$, where the dialogue elements are the RCs of each RIS element. Supposing the deployment of a transmitter with N_t antennas and a receiver with N_r antennas, the received signal at the k^th antenna would then be expressed as

$$\boldsymbol{y}^k = \boldsymbol{g}\boldsymbol{\Theta}\boldsymbol{h}\boldsymbol{x} + \boldsymbol{n}, \tag{2}$$

where $\boldsymbol{x} \in \mathbb{C}^{N_\mathrm{t}\times 1}$ represents the transmitted signal from the transmitter, $\boldsymbol{h} \in \mathbb{C}^{AB\times N_\mathrm{t}}$ represents the channel from the transmitter to the RIS structure, $\boldsymbol{g} \in \mathbb{C}^{N_\mathrm{r}\times AB}$ represents the channel from the RIS structure to the receiver, and $\boldsymbol{n} \in \mathbb{C}^{N_\mathrm{r}\times 1}$ represents the set of noise. The digital RIS architecture proposed serves as the transmitter. At this point, the transmitter sends a single carrier, where the elements of $\boldsymbol{x}$ are represented by 1.

2.2 Transmission line based precise phase shifter

Given that the objective is to control the RCs of RIS elements, it is foreseeable that the phase shifter structure, including RF switches and an impedance matching network, would be required. Specifically, an SP4T RF switch is selected to demonstrate the design of the phase shifter. Considering the parasitic impedance generated by available capacitors and resistors under high frequency, micro-band transmission lines are chosen as the impedance matching network for the proposed phase shifter. According to the transmission line theory, the relationship between the phase and the transmission line length could be written as

$$\Delta\phi = \frac{2\pi}{\lambda_\mathrm{g}}\left(l_1 - l_2\right), \tag{3}$$

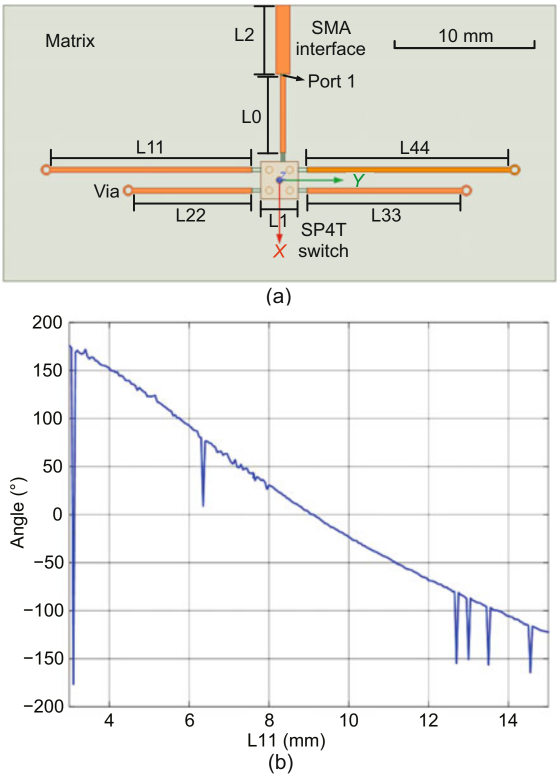
where $\Delta\phi$ is the phase shift value, $\lambda_g = \lambda/\sqrt{\varepsilon_r}$ is the medium wavelength, and ε_r is the dielectric constant. $l_1 - l_2$ denotes the segment between the electrical lengths of two transmission lines. Since the incident signal is reflected to the receiver through the transmission lines, the length difference of transmission lines with a phase difference of $\pi/2$ should be $\lambda/8$.

Fig. 2a depicts the High Frequency Structure Simulator (HFSS) model of the proposed 2-bit phase shifter. First, the SP4T switch model is established, including a pad, five vias, an input port, and four output ports, where all ports are bound with S-parameters. Next, the impendence matching network is designed according to Eq. (3), where each output port is connected to a transmission line. To avoid end radiation that would be caused by the open transmission line, the other end of the transmission line is connected to a via hole. Moreover, the center frequency of the system is set at 5.6 GHz to avoid interference caused by electromagnetic waves in the Wi-Fi band. The medium is flame retardant 4 (FR4, $\varepsilon_r = 4.4$), and the thickness of the board is 1.2 mm. TXLINE is employed to calculate the width and length of the 50-Ω matching line, and the specific parameter settings are provided in Table 2.

Table 2 Parameter settings

Parameter	Value	Description
T	35 μm	Thickness of the immersion gold
H	0.203 mm	Media thickness
W50	0.359 mm	Width of the 50-Ω transmission line
L1	2.7 mm	Pad length of the SP4T switch
L2	5 mm	Pad length of the SMA interface
R1	10 mil	Inner diameter of the via
R2	15 mil	Outer diameter of the via
L11	5.2 mm	Simulation results of the lengths of the transmission lines
L22	11.3 mm	
L33	8.7 mm	
L44	14.65 mm	

Due to the effects of materials and space radiation, the theoretical length of the transmission line usually needs to be revised. Next, the length of transmission lines is scanned to obtain the proper parameters. The phase shift of port 1 associated with L11 is presented in Fig. 2b. The phase shift performances of L22, L33, and L44 are similar to that of L11. With the length of the transmission line increasing, the phase shift between the incident signal and the echo signal at port 1 shows an approximately linear change. In contrast with the general impedance network, the RCs move on the circle of the Smith chart with a modification in the length of the transmission line, which results in phase movement of $\Gamma_{a,b}$. To maintain a phase shift of $\pi/2$ between the four ports of the RF switch, it is necessary to determine the values of L11, L22, L33, and L44. On the other hand, the callback loss of port 1 (S_{11}) remains above −4 dB, indicating that the reflected energy is much greater than the absorbed energy. Consequently, the incident signal is modulated and reflected to the receiver. Finally, the four selected transmission lines are the ones whose lengths are represented as L11, L22, L33, and L44, as indicated in Table 2, and the corresponding phases are $-2\pi/3$, $-\pi/3$, 0, and $2\pi/3$; the reason underlying the choice of these four RCs is explained in Section 2.3.



(a)

(b)

Fig. 2 HFSS model of the 2-bit phase shifter: (a) HFSS model of the SP4T switch and phase shifter; (b) simulation results of the phase angle

2.3 High-order modulation scheme

In this subsection, a high-order modulation scheme based on the proposed phase shifter is presented. Due to the finite RCs, frequency shift and phase rotation are used simultaneously to create the constellation points. First, Fig. 3 explains the principle of the proposed modulation scheme. The transmitter's carrier frequency is set as f_0, while the transmission frequency of the RIS structure is Δf. When the RF switches handoff between two RCs, RC1 and RC2, a frequency shift to the carrier signal f_0 is realized. Furthermore, the characteristics of the frequency shift signal are changed by arranging and combining different RC pairs. On the other hand, phase rotation is obtained by applying additional time delays to the clock of FPGA. Specifically, when the clock controls an internal signal phase shift of 2π, the new signal will overlap with the original signal. By evenly dividing the 2π phase, phase rotations of different bits can be obtained. As illustrated in Fig. 4a, when the phase is rotated by $\pi/2$ each time, the standard QPSK signal is obtained. Correspondingly, the four constellation points are represented as 00, 01, 10, and 11.

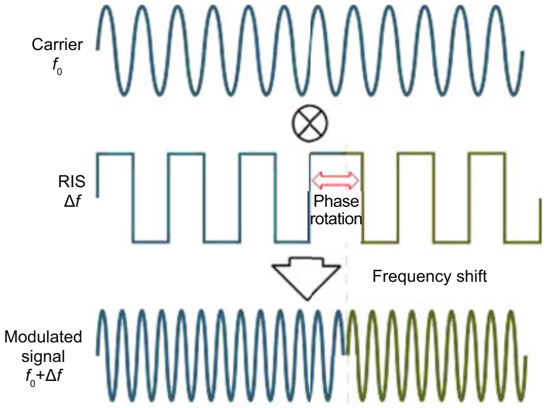


Fig. 3 Modulation principle

Furthermore, Fig. 4b shows the standard 16-QAM scheme, where four RCs are selected to create four frequency offsets. Since we are aiming at retaining the coordinates of the four constellation points of 1+i, 2+i, 1+2i, and 2+2i, the angle between RC3, RC1, and RC2 should be maintained at $\pi/4$, and the angle between RC3, RC4, and RC2 is maintained at $\pi/2$. To accurately control the position of the RC points moving inward in the circular graph, it is necessary to set the parameters of the ideal capacitance and inductance. However, in practice, ideal capacitors and inductors do not exist, and high-frequency characteristics can be illustrated as

$$Z_C = \mathrm{j}\omega L_\mathrm{e} + R_\mathrm{s} + \frac{1}{G_\mathrm{e} + \mathrm{j}\omega C}, \tag{4}$$

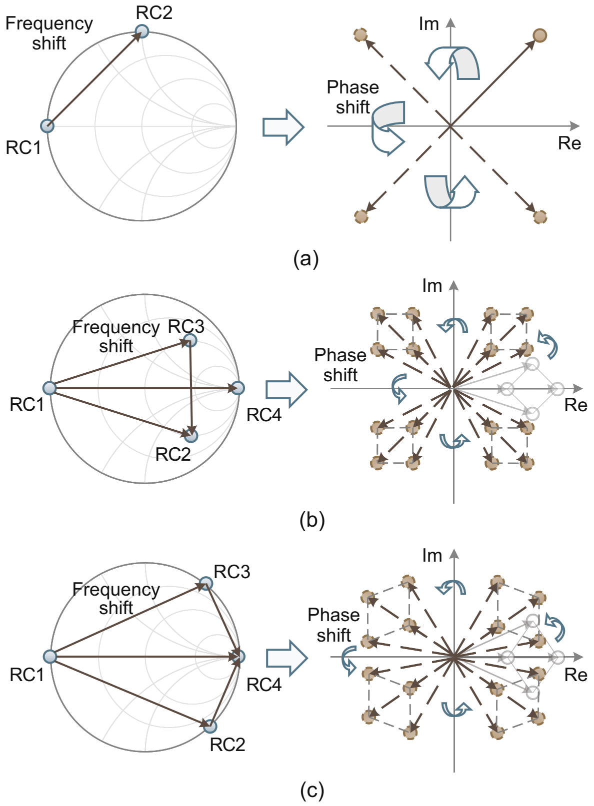


Fig. 4 High-order modulation scheme: (a) QPSK; (b) standard 16-QAM; (c) near-standard 16-QAM

$$Z_L = \mathrm{j}\omega L_\mathrm{e} + \frac{1}{\mathrm{j}\omega C_\mathrm{a} + 1/R_\mathrm{s}}, \tag{5}$$

where L_e represents the lead impedance, C represents the inter-board capacitance, R_s represents the characteristic impedance, C_a represents the parasitic capacitance, $G_\mathrm{e} = \omega C \tan \varDelta$ represents the conduction, and $\varDelta$ represents the loss angle. According to Eqs. (4) and (5), the parameters vary with the circuit and spatial electromagnetic field, which makes it difficult to control the capacitance and inductance characteristics in practice. Consequently, an impedance adjustment scheme based on the microstrip line length is proposed. Specifically, the impedance calculation of the microstrip is given by

$$Z_\mathrm{O} = \frac{87}{\sqrt{\varepsilon_\mathrm{r} + 1.41}} \ln\left(\frac{5.98H}{0.8W + T}\right), \tag{6}$$

where ε_r denotes the dielectric constant, H represents the height of the medium, W represents the width of the microstrip, and T represents the copper coating thickness. When the process and substrate material are given, the impedance parameters of the microstrip are related only to W. The RC phase can be modified by adjusting the length of the microstrip. However, the RCs provided by the microstrip impedance move only around the circular graph's circumference, making it impossible to obtain orthogonal constellation points. Consequently, a near-standard QAM scheme is illustrated based on the proposed transmission line phase shifter.

As demonstrated in Fig. 4c, four RCs lie on the circumference of the Smith chart. The angle between RC3, RC1, and RC2 is set to $\pi/3$, while that between RC3, RC4, and RC2 is set to $2\pi/3$. To ensure the formation of a regular rhombus, the RCs are mapped to constellation points within the coordinate system. Naturally, the near-standard 16-QAM is obtained as a result of phase rotation performed thrice.

3 Simulation results

In this section, the BER performance of the proposed near-standard modulation scheme is analyzed to verify the feasibility of the system. The Rayleigh channel with perfect channel state information is assumed in all the simulation results. First, the transmitter sends the carrier signal to the RIS structure. After passive modulation of RIS, the receiver demodulates the reflected signal. At the receiver, the signal is demodulated using a maximum likelihood (ML) detector, which is written as

$$\hat{\Theta} = \arg\min \|\boldsymbol{y} - \boldsymbol{g}\boldsymbol{\Theta}\boldsymbol{h}\boldsymbol{x}\|^2, \tag{7}$$

where $\hat{\Theta}$ indicates the estimated signal. In this research, a single antenna transmitter that continuously sends a single carrier is considered, where the elements of $\boldsymbol{x}$ are denoted as 1. In this paper, $\|\cdot\|$ denotes the Frobenious norm of a matrix. The ML detector is further written as

$$\hat{\Theta} = \arg\min \|\boldsymbol{y} - \boldsymbol{g}\boldsymbol{\Theta}\|^2, \tag{8}$$

and a blind channel estimation method is applied for signal demodulation. Table 3 discusses the mapping of transmitting symbols and constellation points, which have been carried out in adherence with the near-standard QAM scheme proposed in Section 2.3. The symbol c equals $\sqrt{2}/2$. The simulation parameters are presented in Table 4. Rayleigh quasi-static fading is considered contemporaneously with the perfect channel state information being known at the receiver. Simulation results are illustrated in Figs. 5 and 6.

Table 3 Simulation mapping table of the proposed scheme

Symbol	Bits	Constellation	Amplitude
0	0000	$0+3\mathrm{i}$	3
1	0001	$-c+2\mathrm{i}$	$\sqrt{19}/4$
2	0010	$-2-c\cdot 1\mathrm{i}$	$\sqrt{19}/4$
3	0011	$-3+0\mathrm{i}$	3
4	0100	$c+2\mathrm{i}$	$\sqrt{19}/4$
5	0101	$0+1\mathrm{i}$	1
6	0110	$-1+0\mathrm{i}$	1
7	0111	$-2+c\cdot 1\mathrm{i}$	$\sqrt{19}/4$
8	1000	$3+0\mathrm{i}$	3
9	1001	$2-c\cdot 1\mathrm{i}$	$\sqrt{19}/4$
10	1010	$0-3\mathrm{i}$	3
11	1011	$c-2\mathrm{i}$	$\sqrt{19}/4$
12	1100	$2+c\cdot 1\mathrm{i}$	$\sqrt{19}/4$
13	1101	$1+0\mathrm{i}$	1
14	1110	$-c-2\mathrm{i}$	$\sqrt{19}/4$
15	1111	$0-1\mathrm{i}$	1

Table 4 Parameter setting of the simulations

Parameter	Value	Parameter	Value
N_t	1	B	4
N_r	1	d_ts	1 m
A	4	d_sr	1 m

A is the number of rows of RIS elements, B is the number of columns of RIS elements, d_ts indicates the distance between the transmitter and the RIS structure, and d_sr denotes the distance between the RIS structure and the receiver

Fig. 5 elucidates the received constellation points of the digital RIS system with a near-standard QAM scheme. Compared to standard QAM structures, the constellation points can be clearly distinguished despite the sacrifice of isolation.

In Fig. 6, the performance results of the proposed digital RIS system, in association with different modulation schemes, are presented and compared. We observe from Fig. 6 that the BER and sample error rate (SER) performances of the proposed modulation method approach those of the traditional QAM, which implies the possibility of applying this method in practical signal transmission. The proposed digital RIS system using near-standard 16-QAM reaches a BER of 10^{-5} at a signal-to-noise ratio (SNR) of 20 dB.

The BERs of different modulation methods are compared in Fig. 7. When the number of RIS elements is the same, the BPSK scheme achieves 10^{-7} at SNR=16 dB, which appears to be the optimal BER performance. Consequently, the proposed near-standard QAM modulation scheme achieves a high transmission rate while ensuring high BER performance. In addition, due to the limitations of demodulation performance at the receiver, a 4-bit discrete phase shifter achieves a performance similar to that of a continuous phase shifter.

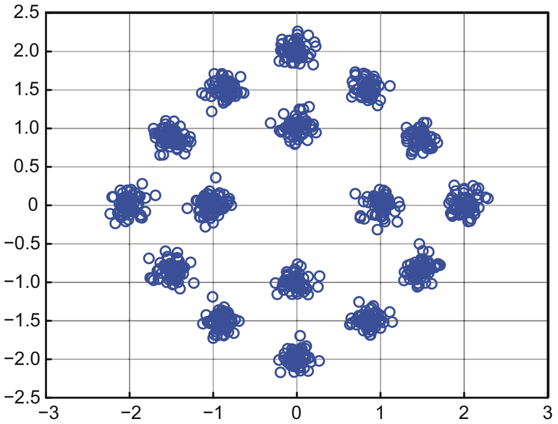


Fig. 5 Simulation results of the received constellation points

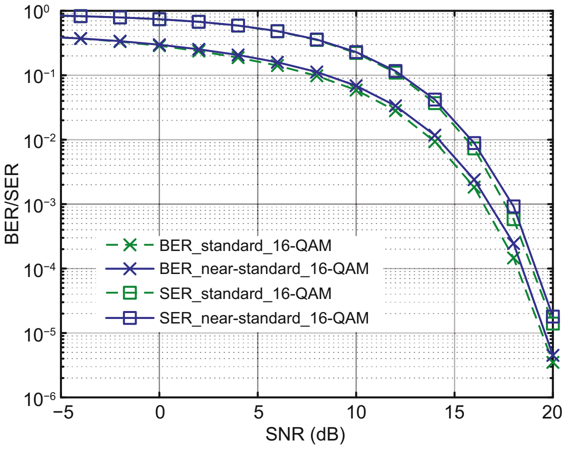


Fig. 6 BER and SER performances of the proposed modulation method

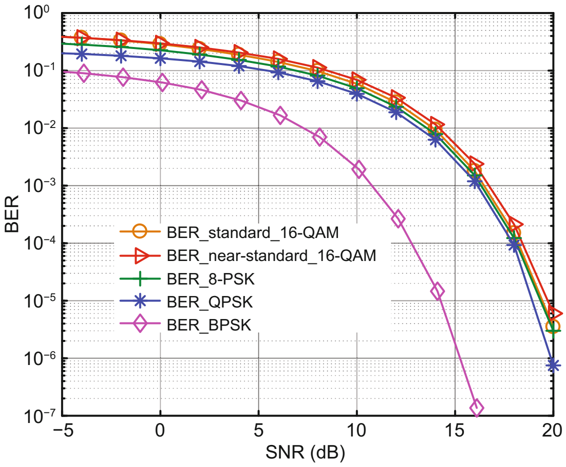


Fig. 7 Comparison of the proposed scheme and traditional schemes

4 Experimental results

In this section, experimental results of the proposed architecture are presented, including the hardware implementation and evaluation.

4.1 Hardware implementation

In this subsection, the prototype of the proposed DAC-free digital RIS architecture, which operates at 5.6 GHz, is illustrated. Fig. 8a shows the circuit of the proposed RIS structure, which is implemented on a printed circuit board (PCB). The design includes 4×4 RIS elements, four RF switches, and a microcontroller. The RIS elements are composed of small microstrip patches, and every group of four elements is connected to a phase shifter. Fig. 8b shows the S_{11} parameter of a set of RIS elements tested by the network analyzer (Libre VNA, ZEENKO, China), which suffers from superior return loss at −30 dB. The RF switch ADRF5040 is chosen because of its sound isolation, high response speed, and low power consumption at high frequencies. Each RF switch is connected to a group of elements and four transmission lines, whose conduction state is controlled by the microcontroller. To enable the selection of the RCs, ultra-low power FPGA (AGLN060V2, Microchip Technology, USA) is used for the microcontroller. The envelope detector (LTC5536ES6, ADI, USA) is also implemented for carrier signal detection, and the high-precision active crystal oscillator (3225 OSC, Genuway, China) is applied for 20 MHz clock generation.

The network analyzer is applied toward explicit testing of the RCs of each group of RIS elements, and the results are given in Table 5. The phase shift between “10” and “00” is close to π/3, while that between “10” and “11” is close to π. The experimental results are consistent with those of the near-standard QAM scheme proposed in Section 2.3.

A host and a USRP 2943R are employed to transmit carrier signals and receive a reflected signal. The transmitter and receiver are equipped with a high-directional double-ridged horn antenna for signal enhancement. During signal transmission, the USRP controls the horn antenna to send a single-carrier signal. Each data packet contains a preamble for the RIS structure, which is implemented for channel estimation at the receiver.

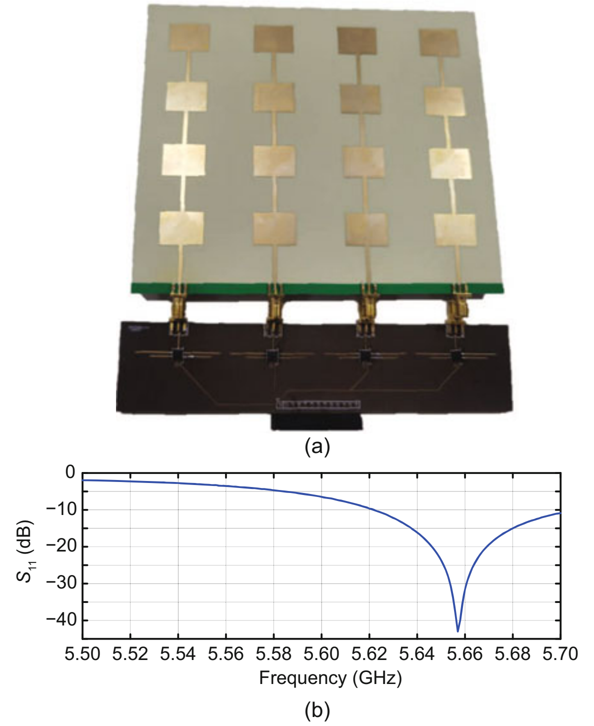


Fig. 8 Prototype of the proposed RIS structure (a) and S_{11} of RIS elements (b)

Table 5 Test results of reflection coefficients

Group	Angle (°)			
	00	01	10	11
1	152	−83	83	30
2	150	−87	88	32
3	145	−89	92	33
4	151	−79	85	27

4.2 Evaluation

In this subsection, we describe the experimental evaluation of the proposed DAC-free digital RIS system. As Fig. 9 illustrates, a pair of double-spine horn antennas are used, each variously connected to the transmitter and receiver. The RIS structure is powered by the host, where 16-QAM signals are transmitted. The transmitter sends packets with a pilot, which is implemented for synchronizing the signal at the RIS structure and the receiver. LabVIEW is applied for controlling the generation of signals for transmission as well as for the processing of the received signals, and Matlab is used for offline demodulation.

Fig. 10 explains the decoding constellation points of the proposed near-standard 16-QAM modulation scheme for the digital RIS structure. An indoor environment encompassing interference from Wi-Fi signals is determined as the condition compatible for the experiments. The distance between the RIS structure and the transmitting and receiving horn antenna is 1 m. According to the test results of the network analyzer, the operating frequency is set to 5.7 GHz, and the sampling frequency is set to 20 MHz. As Fig. 10 shows, the transmission constellation symbols can be accurately restored after demodulating the received time-domain signal. The data rate of the proposed scheme reaches 800 kb/s after ignoring the synchronization and pilot overhead. The power consumption of the control circuit and RIS elements is at mW-level. By increasing the numbers of RIS elements and transmitting links, the system's data rate could be further improved, against the prevalent backdrop of the need to ensure limited power consumption.

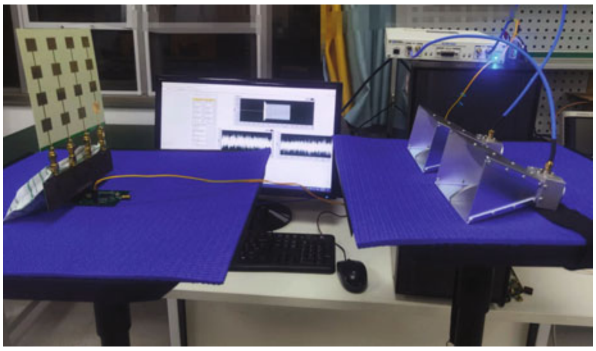


Fig. 9 Test scenario

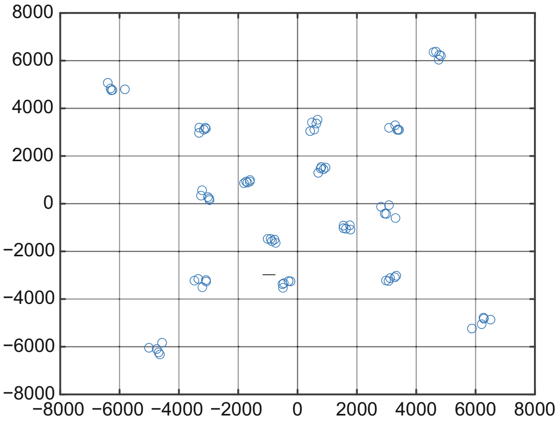


Fig. 10 Demodulation results

5 Conclusions

In the present research, a DAC-free architecture is proposed for digital RIS structure, and high-precision phase shifters and novel high-order modulation schemes are analyzed for the proposed architecture. Simulation and experimental results confirm the feasibility of the proposed algorithm. Compared with the traditional digital RIS architecture, the proposed architecture and modulation method can effectively reduce power consumption and hardware cost.

Contributors

Miaoran PENG designed the research. Miaoran PENG and Jinhao KAN processed the data. Miaoran PENG drafted the paper. Lixia XIAO, Guanghua LIU, and Jinhao KAN helped organize the paper. Miaoran PENG, Lixia XIAO, Guanghua LIU, and Tao JIANG revised and finalized the paper.

Compliance with ethics guidelines

Miaoran PENG, Jinhao KAN, Lixia XIAO, Guanghua LIU, and Tao JIANG declare that they have no conflict of interest.

Data availability

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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