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Design and verification of an FPGA programmable logic element based on Sense-Switch pFLASH*

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Abstract: This paper proposes a kind of programmable logic element (PLE) based on Sense-Switch pFLASH technology. By programming Sense-Switch pFLASH, all three-bit look-up table (LUT3) functions, partial four-bit look-up table (LUT4) functions, latch functions, and d flip flop (DFF) with enable and reset functions can be realized. Because PLE uses a choice of operational logic (COOL) approach for the operation of logic functions, it allows any logic circuit to be implemented at any ratio of combinatorial logic to register. This intrinsic property makes it close to the basic application specific integrated circuit (ASIC) cell in terms of fine granularity, thus allowing ASIC-like cell-based mappers to apply all their optimization potential. By measuring Sense-Switch pFLASH and PLE circuits, the results show that the "on" state driving current of the Sense-Switch pFLASH is about 245.52 μA, and that the "off" state leakage current is about 0.1 pA. The programmable function of PLE works normally. The delay of the typical combinatorial logic operation AND3 is 0.69 ns, and the delay of the sequential logic operation DFF is 0.65 ns, both of which meet the requirements of the design technical index.

Key words: Field programmable gate array (FPGA); Programmable logic element (PLE); Boolean logic operation; Look-up table; Sense-Switch pFLASH; Threshold voltage

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1 Introduction

Field programmable gate arrays (FPGAs) are widely used in signal processing, fifth-generation (5G) communication, industrial control, artificial intelligence, and other fields due to their high density, rich logic resources, and flexible programmability (Nadal and Baghdadi, 2021). From the realization of FPGA process classification, it includes three types, i.e., static random access memory (SRAM) based FPGA (Zhang et al., 2022), anti-fuse-based FPGA (Liu MQ et al., 2022), and Flash-based FPGA (Wulf et al., 2022).

The advantages of SRAM-based FPGA are its large scale and high computing power, which can realize user logic of more than 100 million equivalent system gates and meet the requirements of high-performance computing. The disadvantage is that data in configuration SRAM are lost after power-off, so non-volatile memory (Desnoyers and Kandiraju, 2016) needs to be configured on the periphery, and the bitstream data will be loaded again during each power-on. The advantages of anti-fuse-based FPGA include non-loss of data after power-off and excellent anti-radiation performance, so it is used as the core control logic circuit in satellites and space stations. The disadvantage is that the anti-fuse layout area used for programmable wiring switches is large, so the

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equivalent number of system gates achieved by this type of FPGA is smaller than six million. Flash-based FPGA balances the advantages and disadvantages of the first two kinds of FPGAs, and uses Flash technology to realize programmable wiring switches, which not only meets the needs of large-scale logic resources, but also does not require peripheral configuration memory. Meanwhile, the radiation resistance performance of Flash cell is obviously better than that of SRAM cell. Therefore, Flash-based FPGA has the characteristics of high startup speed, simple peripheral circuit, high resource density, and good anti-radiation performance, and is especially suitable for aerospace applications such as image processing and data transmission.

The programmable logic element (PLE) is the core logic in FPGA; it is the most basic module that realizes user programmable logic functions and has the largest logic resources. The PLE can be implemented in two ways; one is using look-up table (LUT) technology (Suzuki and Hanyu, 2023), and the other is using choice of operational logic (COOL) technology. The former is suitable for applications in SRAM-based FPGA, such as Xilinx company's SRAM-based FPGA (Xilinx Inc., 2009), while the latter is suitable for applications in Flash-based FPGA, such as ACTEL company's Flash-based FPGA (Microchip Technology Inc., 2022). Due to the high technical barriers of Flash-based FPGA, there are few companies designing Flash-based FPGA. Currently, Flash-based FPGA research and product development institutions include mainly ACTEL Corporation in the United States and No. 58 Research Institute of China Electronics Technology Group Corporation in China (Cao et al., 2022a, 2022b; Shan et al., 2022). ACTEL company uses n-channel Flash as a signal switch and uses 32 nFLASH switches to design a PLE that can realize any three-input logic function operation. The domestic research on Flash-based FPGA, Sense-Switch pFLASH (SSPF) (Liu GZ et al., 2019; Song et al., 2021; Cao et al., 2023; Jiang et al., 2023), was conducted from the p-channel Flash technology as the signal switch in PLE.

In this paper, a novel PLE based on SSPF and using COOL technology is proposed for Flash-based FPGA, and the PLE array of the whole chip is constructed. Extensive tests are carried out to evaluate the performance of the proposed PLE and compare it with other PLEs used in FPGA.

2 Structure and principle of Flash-based FPGA

Flash-based FPGA is composed mainly of PLE, digital signal processor (DSP) (Eddla and Pappu, 2022), block random access memory (BRAM) (Tian et al., 2023), input/output block (IOB) (Swift et al., 2004), switch box (SB), programmable interconnect point (PIP) (Zhang et al., 2020), and phase-locked loop (PLL) (Jin et al., 2023). The resource structure and principle of Flash-based FPGA are shown in Fig. 1.

Flash-based FPGA implements different digital logic functions, which are realized mainly by PLE and SB. Both PLE and SB contain SSPF, and different signal paths are selected by programming SSPF, so as to realize programmable logic functions. Fig. 1a shows the overall resource structure of the Flash-based FPGA; in Fig. 1b, the SB is a universal programmable SB, which realizes the interconnection of signals in four directions; the PLE in Fig. 1c is a basic module equivalent to any three-input look-up table, which can implement basic logic functions such as AND, OR, or XOR; Fig. 1d shows the circuit diagram of the SSPF, which is the structure of a shared floating gate (FG). Its physical device structure is shown in Fig. 1e.

3 Programmable logic element and programming circuit design

3.1 Sense-Switch pFLASH design

SSPF is the most critical core technology for designing Flash-based FPGA. The performances of the SSPF (Liu GZ et al., 2020, 2023; Song et al., 2022), such as the consistency of the programmed threshold voltage, driving current, and turn-off current, determine the maximum operating frequency and static power consumption of the Flash-based FPGA. SSPF is composed of two p-type FG metal oxide semiconductor (MOS) transistors that share an FG and a control gate (CG). T1 and T2 are a programming/erase transistor (Sense) and a switch transistor (Switch) for signal transmission control, respectively, as shown in Fig. 2. A scanning electron microscope (SEM) photo of the SSPF structure based on the 90 nm Flash process is shown in Fig. 3. The charge in the shared FG is changed by programming and erasing

T1, which then controls the working state of the T2 switch. Its programming method adopts band-to-band tunneling induced hot electron (BTBTIHE) (Takahiro et al., 1999) to charge the FG as shown in Fig. 4a, namely, the "on" state. The erase mode adopts full-channel uniform Fowler–Nordheim (FN) (Chan and Liu, 1999) tunneling mode to remove FG charge, as shown in Fig. 4b, namely the "off" state. D and S represent the drain port and the source port of the transistor, respectively.

3.2 PLE logic circuit design

In this study, PLE is designed based on SSPF. In the COOL way, any three-input logic function (equivalent to LUT3), partial four-input logic function (equivalent to LUT4), latch function, and d flip flop (DFF) with enable and reset functions can be realized through MUX2_1, NOR2, NOT, and SSPF. The PLE allows arbitrary logic circuit designs to be implemented at any ratio of combinatorial logic to register. This intrinsic property makes it close to the basic application specific integrated circuit (ASIC) cell in terms of fine granularity, thus allowing ASIC-like cell-based mappers to apply all their optimization potential.

In a Boolean logic operation, all logic operations can be realized by the three most basic logic operations, i.e., two-input AND, OR, and NOT (Tan, 2006), and there are eight kinds of logic functions for any two-input logic operation after simplification. In COOL technology, MUX2_1 is taken as the basic unit to replace the above three kinds of logic gate circuits. In addition to realizing any two-input logic operation,

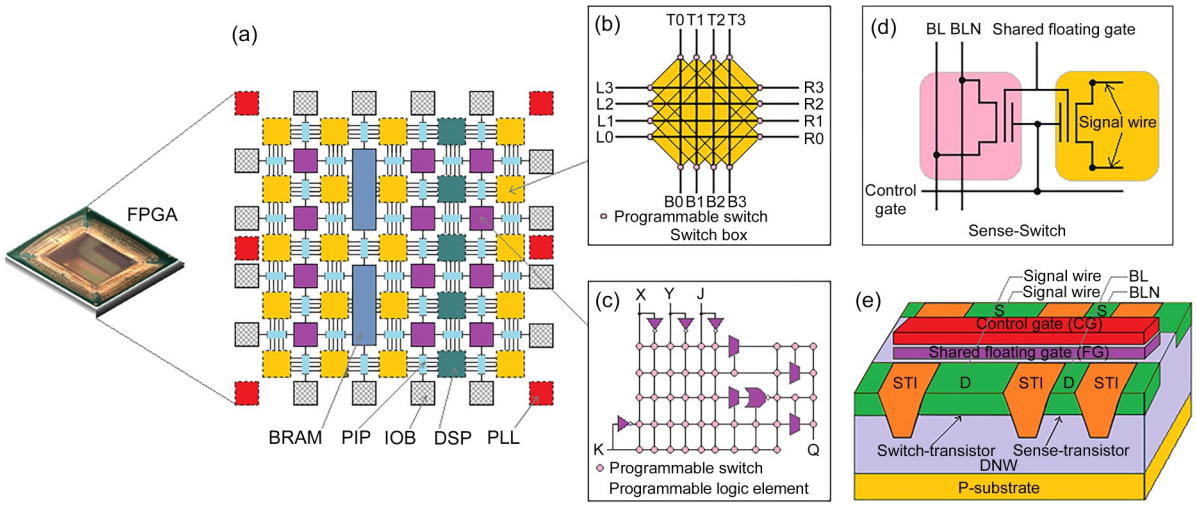

Fig. 1 Structure and principle of Flash-based FPGA: (a) overall resource structure of Flash-based FPGA; (b) a universal SB; (c) a PLE; (d) circuit of the SSPF; (e) physical device structure of the SSPF (FPGA: field programmable gate array; SB: switch box; PLE: programmable logic element; SSPF: Sense-Switch pFLASH; BRAM: block random access memory; PIP: programmable interconnect point; IOB: input/output block; DSP: digital signal processor; PLL: phase-locked loop; BL: bit line; BLN: bit line NOT; DNW: deep N-well; STI: shallow trench isolation)

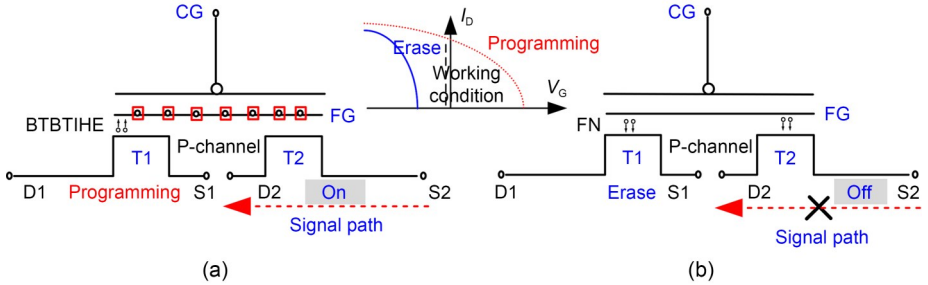

Fig. 2 Schematic diagram of the SSPF working mode: (a) "on" state (programming state); (b) "off" state (erase state) (SSPF: Sense-Switch pFLASH; CG: control gate; FG: floating gate; FN: Fowler–Nordheim; BTBTIHE: band-to-band tunneling induced hot electron)

MUX2_1 can realize two kinds of logic functions with the output fixed as “0” (when A0=A1=S=0) and “1” (when A0=A1=S=1). So, MUX2_1 can implement 10 kinds of logic functions. The logic operations of any two-input AND connection method of replacing AND, OR, and NOT with a single MUX2_1 are shown in Fig. 5.

The programmable combination of four MUX2_1 implementations via SSPF enables the implementation of arbitrary three-input logic functions and DFF functions. Fig. 6 shows the circuit diagram of the PLE designed in this study, which contains 4 MUX2_1, 36 SSPFs, 1 NOR2, and 13 NOT. The circuit design uses 90 nm Flash technology.

In the sequential circuit, DFF is the most frequently used register and the core unit of the circuit. Therefore, DFF with enable and reset functions will be taken as an example to describe its implementation in PLE. In Fig. 6, X is used as the data input port D of the DFF, and the pink line is the data input path of the DFF. Y is used as the clock input port CK of the

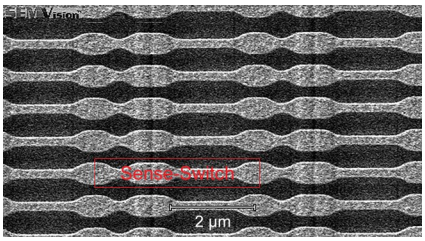

Fig. 3 An SEM photo of the SSPF device (SEM: scanning electron microscope; SSPF: Sense-Switch pFLASH)

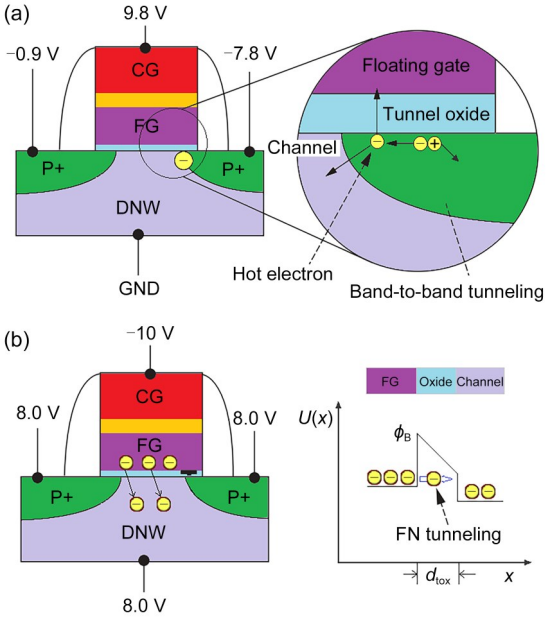

Fig. 4 SSPF erase and programming: (a) BTBTIHE tunneling mode programming; (b) FN tunneling mode erase (SSPF: Sense-Switch pFLASH; BTBTIHE: band-to-band tunneling induced hot electron; FN: Fowler–Nordheim; CG: control gate; FG: floating gate; DNW: deep N-well)

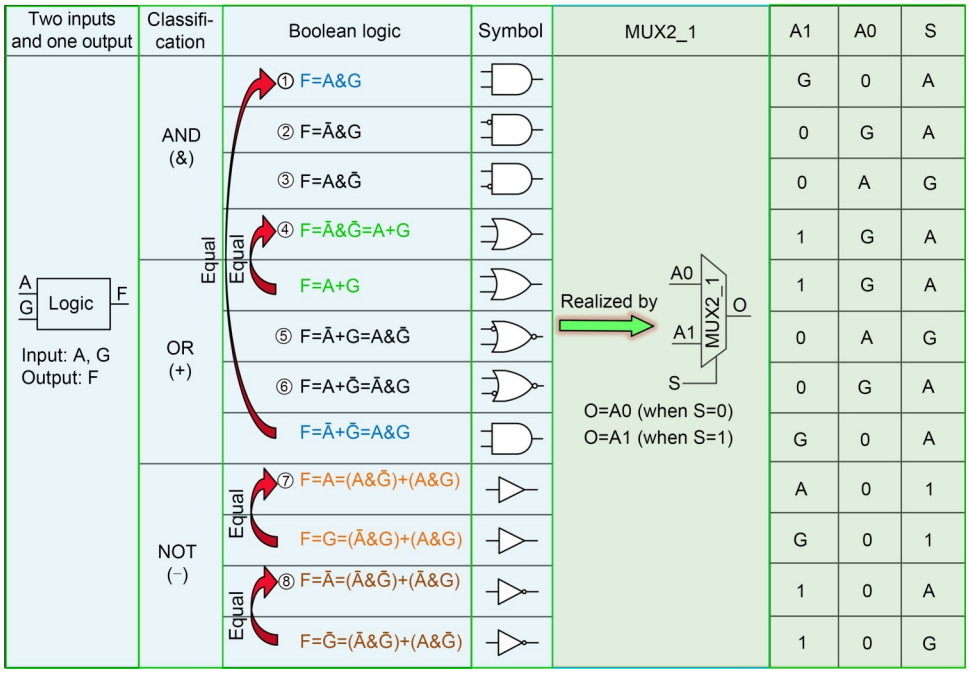

Fig. 5 Logic operations of any two-input AND connection method with a single MUX2_1 of replacing AND, OR, and NOT

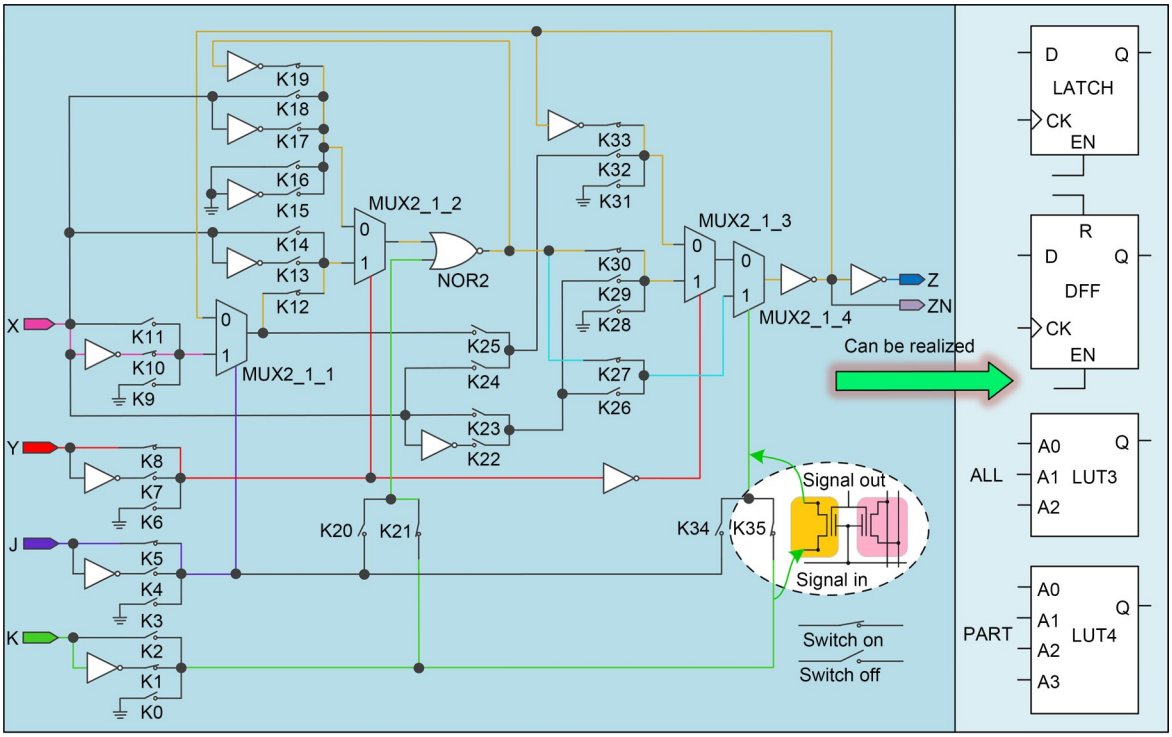

Fig. 6 Circuit diagram of the PLE designed in this study and the principle of implementing a DFF with enable and reset functions (PLE: programmable logic element; DFF: d flip flop)

DFF, and the red line is the clock path of the DFF. J is used as the enable input port EN of the DFF, and the purple line is the enable path of the DFF. K is used as the data reset port R of the DFF, and the green line is the reset path of the DFF. Z is used as the data output port Q of the DFF, and the yellow line is the signal feedback path inside the DFF to realize the data latch. In Fig. 6, a total of 11 SSPFs labeled K10, K12, K8, K5, K1, K21, K35, K19, K27, K30, and K33 are in the "on" state after programming, while the rest are completely in the "off" state. The simulation waveform of the DFF at 25 ℃ is shown in Fig. 7.

Another important functional module in the sequential circuit is LATCH. The implementation of enabled LATCH in PLE is shown in Fig. 8. X, Y, and J ports are used as LATCH data input port D, clock input port CK, and enable input port EN, respectively.

There is also a register with a special function in the sequential circuit, called the clock trigger register CDFF, which is often used in timers to output fixed logic signals triggered by the clock. The realization method is to connect the input port of DFF to "power" or "ground." In this design, the input port is connected to the ground, and the output is the logic signal "1."

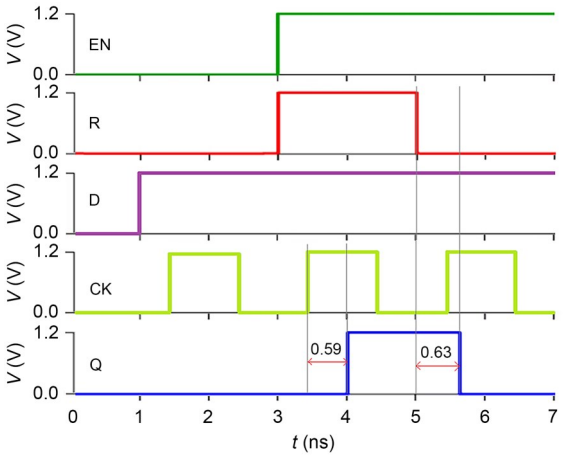

Fig. 7 Simulation waveform of the d flip flop (DFF) at 25 ℃

Table 1 shows the SSPF statistics of LATCH, DFF, and CDFF in PLE in the above sequential circuit.

In combinatorial logic operations, INV, two-input AND2, NOR, and three-input AND3, NOR3 are the most basic logic operation units. In PLE, they are all realized through different connection modes of MUX2_1. The implementation of AND3 in PLE is shown in Fig. 9, and the implementation of NOR3 in PLE is shown in Fig. 10.

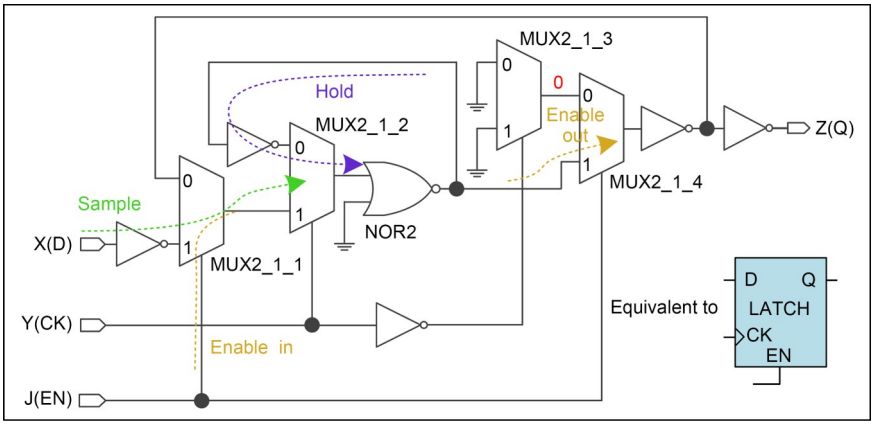

Fig. 8 Simplified circuit diagram of the enabled LATCH implemented in the programmable logic element (PLE)

Table 1 Statistics of the SSPF used for LATCH, DFF, and CDFF implemented in the PLE

Function	Symbol	Used input port	Used Sense-Switch pFLASH
LATCH	D Q LATCH CK EN	X, Y, J	K10, K12, K8, K5, K34, K0, K21, K19, K27, K28, K31
DFF	D R Q DFF CK EN	X, Y, J, K	K10, K12, K8, K5, K1, K21, K35, K19, K27, K30, K33
CDFF	D R Q CDFF CK EN	Y, J, K	K9, K12, K8, K5, K1, K21, K35, K19, K27, K30, K33

SSPF: Sense-Switch pFLASH; DFF: d flip flop; PLE: programmable logic element

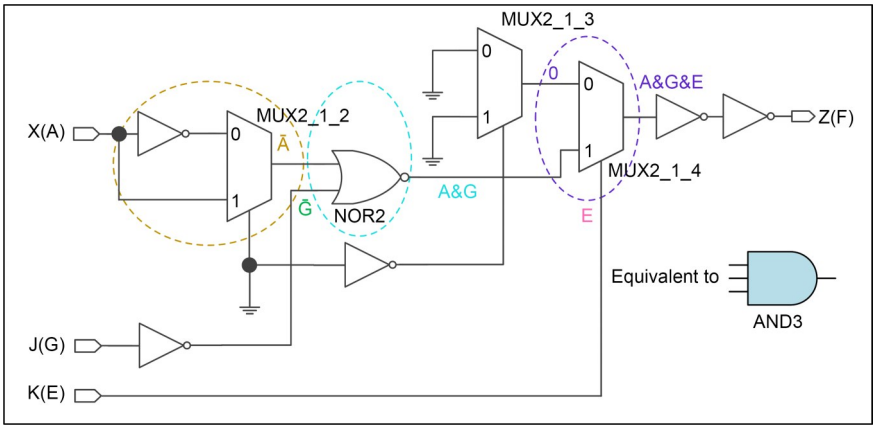

Fig. 9 Simplified circuit diagram of the AND3 implemented in the programmable logic element (PLE)

The XOR gate is also widely used in combinational logic operations; it can be used to realize parity generators, controllable inverters, XOR check, etc. In particular, the application of a three-input XOR3 gate in the adder can generate the summing signal of a one-bit full adder (Anjaneyulu and Reddy, 2023). The operation logic of the three-input XOR3 gate is shown as follows:

$$F=A\oplus G\oplus E, \tag{1}$$

where A, G, and E are three input signals and F is the output signal.

Eq. (1) is converted and expressed in the form of MUX2_1. The conversion process is as follows:

$$\begin{aligned} F&=A\oplus G\oplus E\\ &=(\bar{A}\&G+A\&\bar{G})\oplus E\\ &=(\overline{\bar{A}\&G+A\&\bar{G}})\&E+(\bar{A}\&G+A\&\bar{G})\&\bar{E}\\ &=(A\&G+\bar{A}\&\bar{G})\&E+(\bar{A}\&G+A\&\bar{G})\&\bar{E}. \end{aligned} \tag{2}$$

Based on Eq. (2), three-input XOR3 is implemented in PLE. The circuit is shown in Fig. 11. The three inputs A, G, and E of XOR3 correspond to input ports X, Y, and J of PLE, respectively.

The carry signal C_O of the one-bit full adder is expressed by three inputs A, G, and E, where A and G are two additions and E is the carry of the upper level. The expression is shown as follows:

$$C_O=A\&G+A\&E+G\&E. \tag{3}$$

Eq. (3) is converted and expressed in the form of MUX2_1. The conversion process is as follows:

$$\begin{aligned} C_O&=A\&G+A\&E+G\&E\\ &=(\bar{E}+E)(A\&G)+A\&E+G\&E\\ &=\bar{E}\&(A\&G)+E\&(A\&G+A+G)\\ &=\bar{E}\&(A\&G)+E\&(A+G). \end{aligned} \tag{4}$$

The carry signal of the full adder is realized in PLE based on Eq. (4). The circuit is shown in Fig. 12. The three inputs A, G, and E of the full adder correspond to the X, Y, and K input ports of PLE, respectively.

Table 2 shows the statistics of SSPF applied to the implementation of the main basic logic operation gates in PLE for achieving equivalent LUT3.

The above describes the three-input logic gate. By selecting different SSPF implementation modes in PLE, more input logic operations can be decomposed into

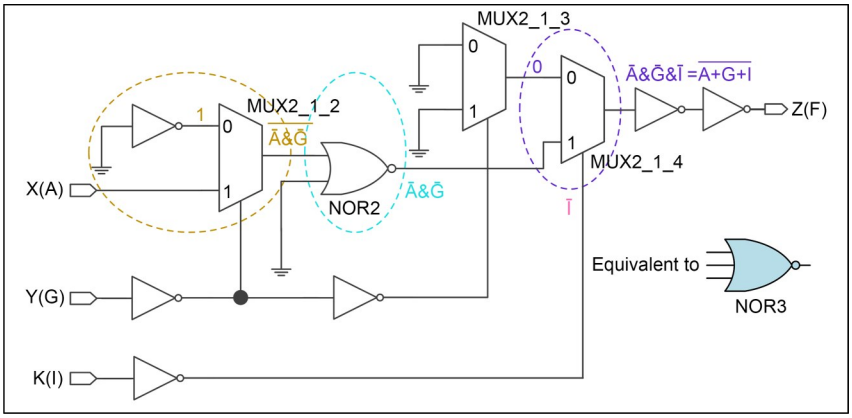

Fig. 10 Simplified circuit diagram of the NOR3 implemented in the programmable logic element (PLE)

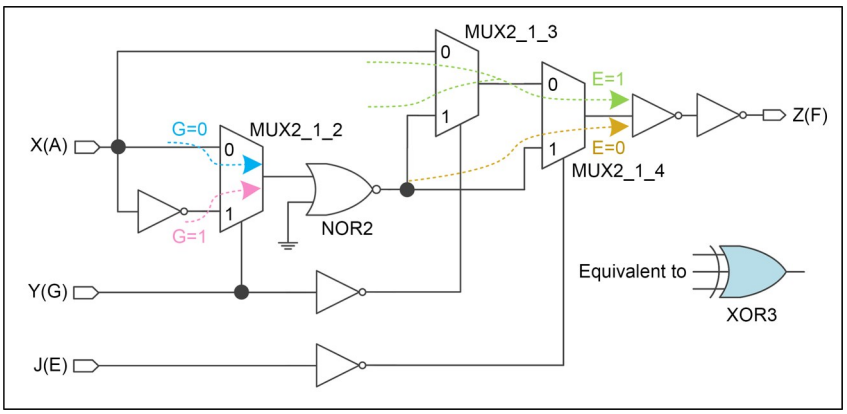

Fig. 11 Simplified circuit diagram of the XOR3 implemented in the programmable logic element (PLE)

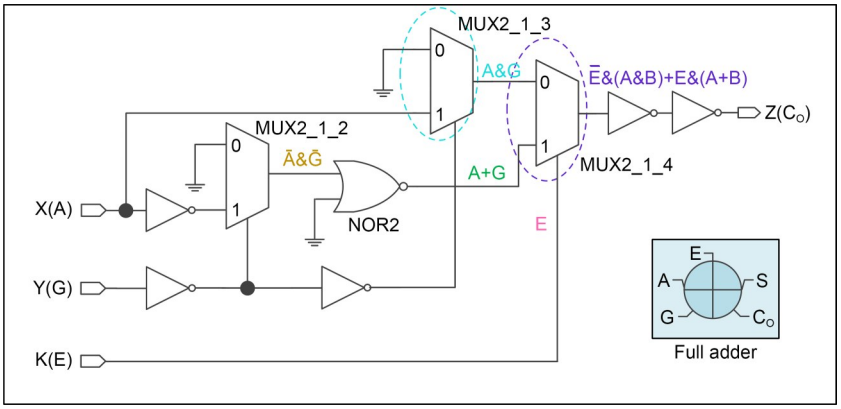

Fig. 12 Simplified circuit diagram of the full adder carry signal implemented in the programmable logic element (PLE)

Table 2 Statistics of the SSPF used for the main basic logic operation gates implemented in the PLE

Function	Symbol	Used input port	Used Sense-Switch pFLASH
INV		X	K22, K29, K6, K31, K3, K34
AND2		X, Y	K23, K29, K7, K31, K3, K34
NOR2		X, Y	K22, K29, K8, K31, K3, K34
XOR2		X, Y	K24, K32, K22, K29, K7, K3, K34
AND3		X, J, K	K14, K17, K6, K4, K20, K28, K31, K2, K35, K27
NOR3		X, Y, K	K14, K15, K7, K3, K20, K28, K31, K1, K35, K27
XOR3		X, Y, J	K13, K18, K24, K32, K8, K0, K21, K5, K34, K30, K27

SSPF: Sense-Switch pFLASH; PLE: programmable logic element

logic operations with no more than three inputs. The designed PLE in this study can realize not only any three-input logic operation, but also partial four-input logic operation, in which all four input ports of the PLE are used. The four-input AND4 and NOR4 are often used in address decoding circuits and digital timing detection. The logic operation AND4 is converted according to MUX2_1, as shown in Eq. (5); the logic operation NOR4 is also converted according to MUX2_1, as shown in Eq. (6):

$$\begin{aligned} F&=A\&G\&E\&I \\ &=((\overline{\overline{\overline{A\&G)\&E}}})\&I \\ &=((\overline{\overline{A\&G}}+\bar{E})\&I, \end{aligned} \tag{5}$$

$$\begin{aligned} F&=\overline{A+G+E+I} \\ &=\bar{A}\&\bar{G}\&\bar{E}\&\bar{I} \\ &=((\overline{\overline{\bar{A}\&\bar{G}}}+E)\&\bar{I}. \end{aligned} \tag{6}$$

AND4 is implemented in PLE as shown in Fig. 13, and NOR4 is implemented in PLE as shown in Fig. 14. The main four-input AND4, AND4A, AND4B, AND4C, NOR4, NOR4A, NOR4B, and NOR4C implementations in PLE using SSPF statistics are shown in Table 3. AND4A means that there is one reversal in the four inputs, AND4B means that there are two reversals, AND4C means that there are three reversals, and the same is true for NOR4A, NOR4B, and NOR4C.

Based on the single PLE mentioned above, the PLE matrix of a certain scale is constructed by expanding it in X and Y directions in the Flash-based FPGA. Taking millions of gate-level Flash-based FPGAs as an example, the PLE matrix includes 32 banks in total, and the size of the PLE matrix in each bank is 12×16, as shown in Fig. 15. Fig. 15a shows two adjacent banks, Fig. 15b shows two bank-to-bank PLEs and an interconnected SB in BANK, Fig. 15c

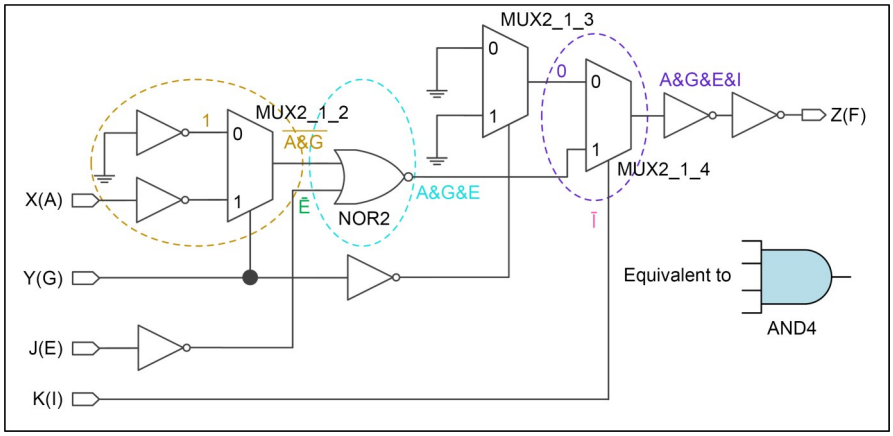

Fig. 13 Simplified circuit diagram of the AND4 implemented in the programmable logic element (PLE)

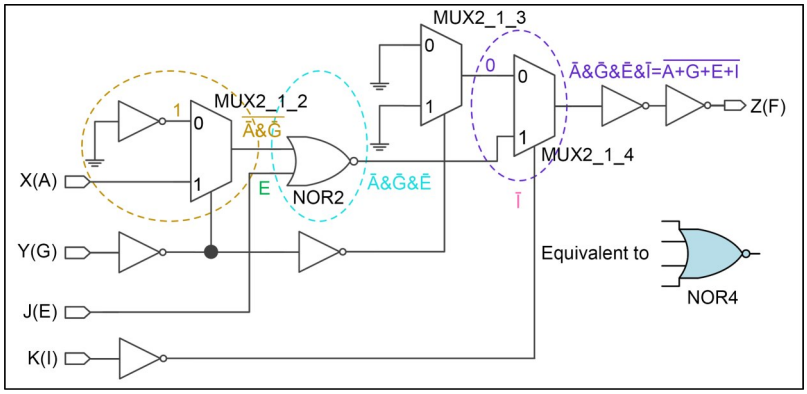

Fig. 14 Simplified circuit diagram of the NOR4 implemented in the programmable logic element (PLE)

Table 3 Statistics of the SSPF used for four-input logic gates implemented in the PLE

Function	Symbol	Used input port	Used Sense-Switch pFLASH
AND4		X, Y, J, K	K13, K15, K8, K4, K20, K2, K35, K28, K31, K27
AND4A		X, Y, J, K	K14, K15, K8, K4, K20, K2, K35, K28, K31, K27
AND4B		X, Y, J, K	K14, K15, K7, K4, K20, K2, K35, K28, K31, K27
AND4C		X, Y, J, K	K14, K15, K7, K5, K20, K2, K35, K28, K31, K27
NOR4		X, Y, J, K	K14, K15, K7, K5, K20, K1, K35, K28, K31, K27
NOR4A		X, Y, J, K	K13, K15, K7, K5, K20, K1, K35, K28, K31, K27
NOR4B		X, Y, J, K	K13, K15, K7, K5, K20, K2, K35, K28, K31, K27
NOR4C		X, Y, J, K	K13, K15, K8, K5, K20, K2, K35, K28, K31, K27

SSPF: Sense-Switch pFLASH; PLE: programmable logic element

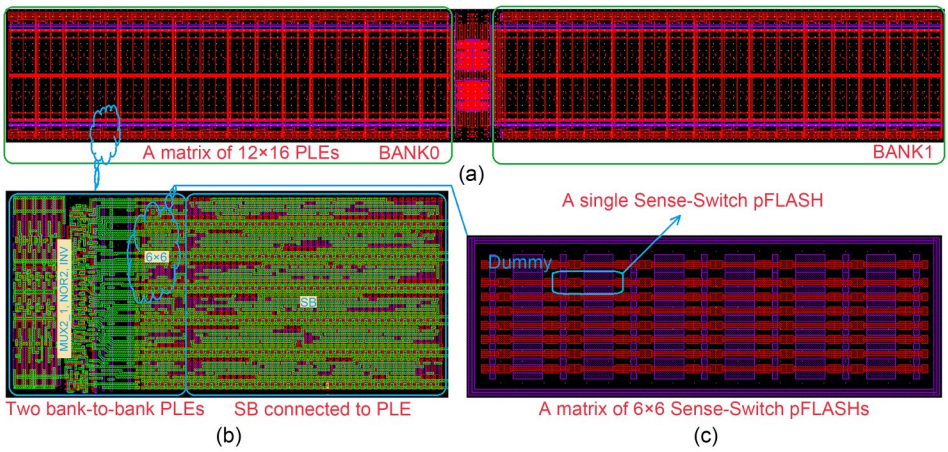

Fig. 15 PLE matrix in the Flash-based FPGA: (a) two adjacent banks; (b) two bank-to-bank PLEs and an interconnected SB; (c) 36 SSPFs of 6×6 in PLE (PLE: programmable logic element; FPGA: field programmable gate array; SB: switch box; SSPF: Sense-Switch pFLASH)

shows 36 SSPFs of 6×6 in PLE, corresponding to K0–K35 in Fig. 6. It is worth noting that, in the layout design of PLE, the layouts of MUX2_1, NOR2, NOT, and SSPF are not placed together as in the logic diagram in Fig. 6. Instead, a separate layout is adopted, as shown in the annotations in Figs. 15b and 15c. The dummy SSPF designed around the SSPF array is isolated for protection (Chou et al., 2021), thus improving the reliability of the internal SSPF.

Each input signal in the PLE is selected mainly through MUX6_1, which consists of six SSPFs, two INVs, and one NMOS, as shown in Fig. 16a. INVs are used to drive the signal output, and NMOS is used to set the global "0" of the signal during the power-on process of the FPGA. The symbol of MUX6_1 is shown in Fig. 16b, and the SB composed of MUX6_1 is shown in Fig. 16c.

3.3 Programming method and circuit

Due to the programmability of Flash-based FPGA, sign-off static timing analysis (Shah et al., 2020) is performed on the user's code after synthesis, technology mapping, place, and route, so as to ensure that the delay on the critical signal path meets the set-time and hold-time of sequential circuits. The delay on the critical signal path consists of three parts: the delay on the logic cell, the delay on the signal line, and the delay on the SSPF. A very important parameter with which to determine the delay is the threshold voltage of the device. The processor of the chip can manufacture PMOS and NMOS devices with the accuracy of the

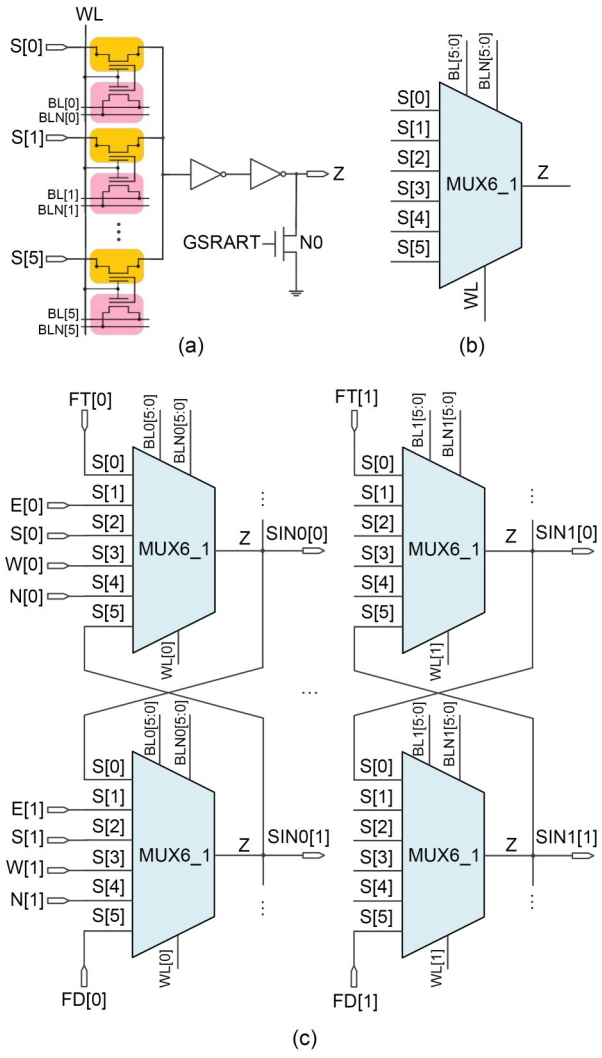

Fig. 16 Schematic of the switch box (SB): (a) schematic of MUX6_1; (b) symbol of MUX6_1; (c) SB array

threshold voltage. The resistance and capacitance of the signal line can also be calculated accurately, so the delay on the logic cell and the delay on the signal line can be obtained accurately. However, the threshold voltage of SSPF has an important relationship with programming voltage, programming time, and programming method, and even programming disturbance (Cai and Huang, 2014) between Flash arrays during programming will have a significant impact on the threshold voltage of SSPF. Therefore, there are strict requirements for the programming of the Flash array in PLE. The purpose is to make the threshold voltage after SSPF programming more accurate and have a better distribution consistency, so as to ensure the superior programmability of Flash-based FPGA.

Based on the features and technical requirements of SSPF in the Flash-based FPGA, the driving capability of the programmed SSPF is controlled within the range of 220–260 μA, and the leakage current after SSPF erasure is controlled below 1 pA to reduce the static power consumption of PLE. The correspondence between threshold voltage distribution and current magnitude of SSPF is shown in Fig. 17. To accurately control the threshold voltage after SSPF programming, the multistep programming method (Cao et al., 2021) is adopted, and the threshold voltage is adjusted to the preset range after several programming sessions. The multistep programming method is shown in Fig. 18.

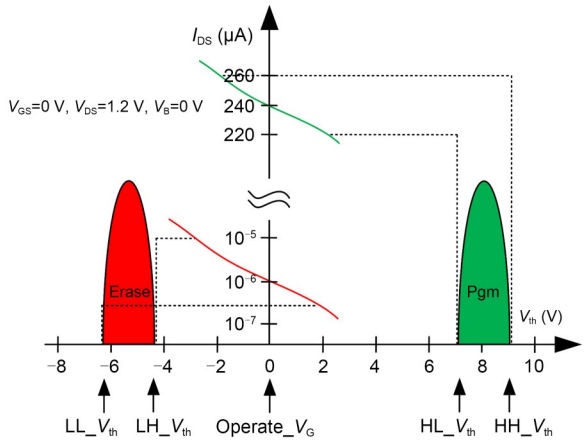

Fig. 17 Correspondence between threshold voltage distribution and current magnitude of SSPF (SSPF: Sense-Switch pFLASH; Pgm: programming)

The programming circuit for SSPF is shown in Fig. 19, which is composed mainly of a positive high voltage charge pump, a negative high voltage charge pump, a reading circuit, line decoding (word line), column decoding (bit line), and an erase–programming control circuit. Both positive and negative high voltage charge pumps use four sets of sub-charge pump circuits with a 90° phase difference of clock signals to work in parallel, which improves the driving capacity of the charge pump and reduces its ripple. Before programming Flash, all SSPFs should be erased to prevent over-programming (Park et al., 2023). In the multistep programming process, the threshold voltage is determined by comparing the SSPF read-back current I_{read} with the reference current I_{ref}, and the programming voltage and time are adjusted in time to improve the accuracy of the threshold voltage after the SSPF programming. A typical programming waveform is shown in Fig. 20.

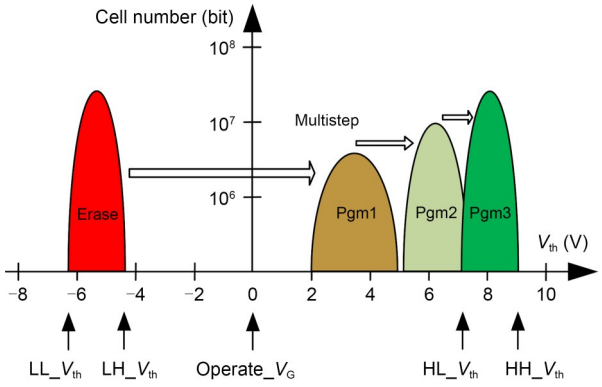

Fig. 18 Multistep programming (Pgm) approach

4 Experimental results and analysis

The test of this study consists of two parts. One is to test the erase and programming characteristics of SSPF. The probe test of SSPF was conducted using an Agilent B1500 semiconductor parameter analyzer and a Summit-12000B low leakage current semi-automatic high- and low-temperature probe station. The other is to test the function and performance of the soft-packaging PLE with the application evaluation board (Fig. 21).

The results of the SSPF test are as follows: 45 groups of arrays (each group of arrays collected one sample point) were investigated. The cumulative distribution of the threshold voltage of the programming/erase state, threshold window, and “on/off” state of the

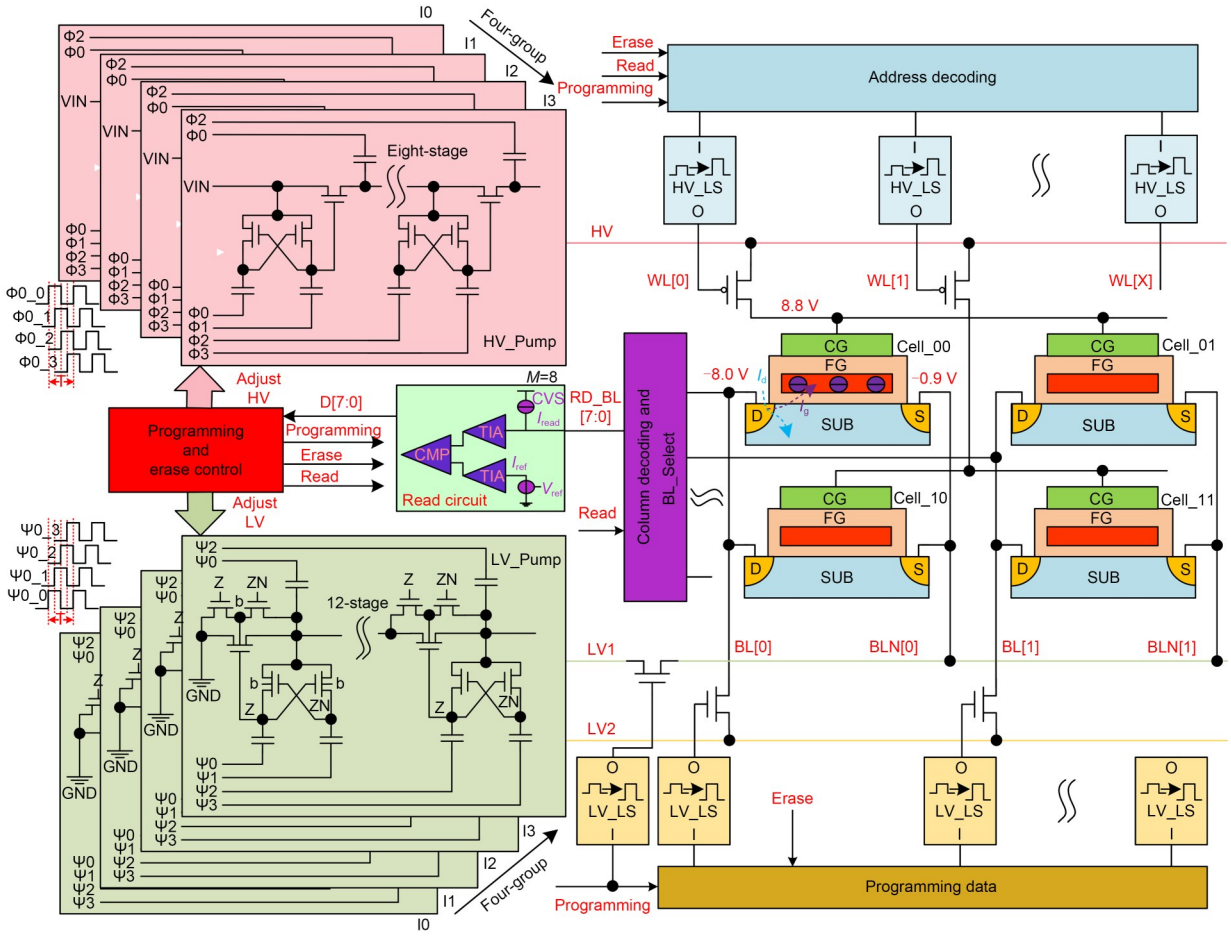

Fig. 19 Programming circuit for SSPF (SSPF: Sense-Switch pFLASH; CG: control gate; FG: floating gate; CMP: comparator; TIA: trans-impedance amplifier; SUB: substrate; BL: bit line; BLN: bit line NOT)

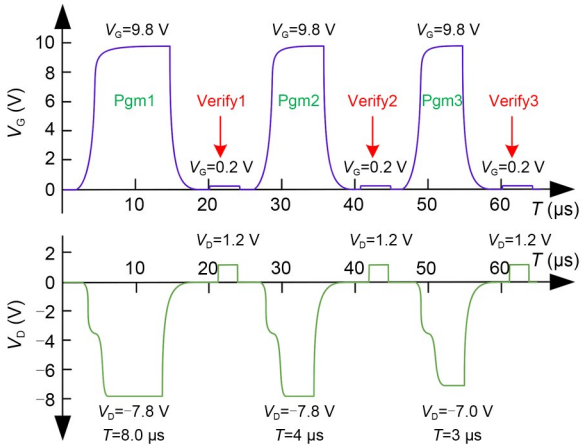

Fig. 20 A typical programming (Pgm) waveform

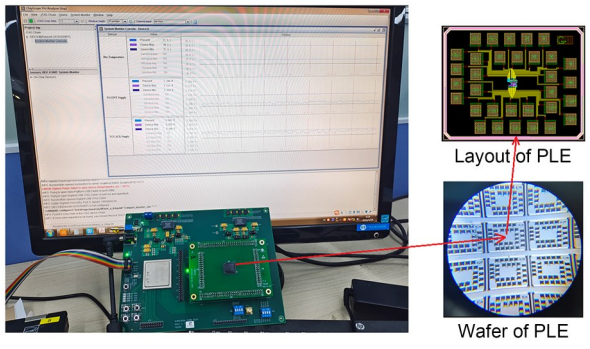

Fig. 21 Silicon wafer and test evaluation board of the programmable logic element (PLE)

transistor T2 are shown in Fig. 22, which showed good consistency. The threshold windows of transistors T1 and T2 were about 13.72 and 13.64 V respectively (uniformity was less than 2.1%), the driving current of the "on" state was about 245.52 μA (normalization: 180.5 μA/μm; uniformity: 5.52%), and the leakage current of the "off" state was about 0.1 pA.

For the test of PLE, the PLE was programmed with different logic functions, and the operating temperature of the PLE was adjusted to −55, 25, and 125 °C,

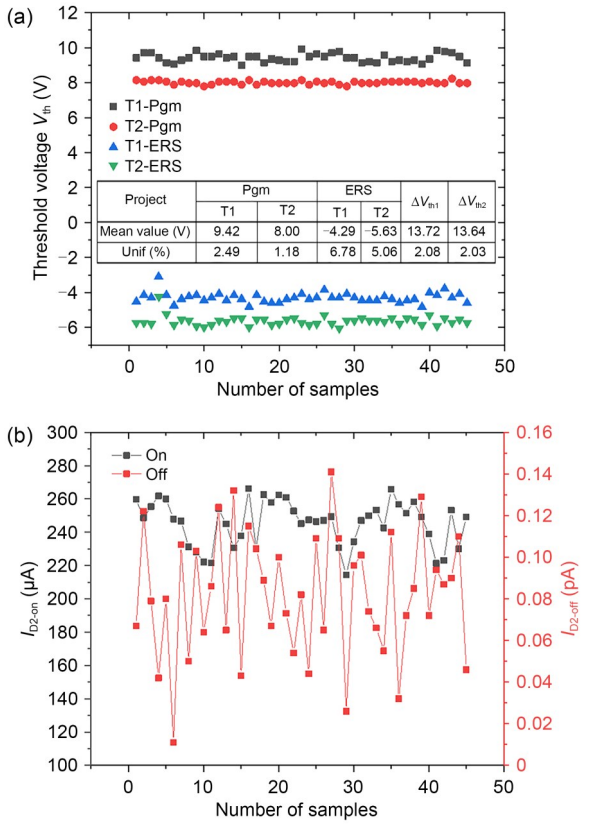

Fig. 22 Characteristics of the SSPF: (a) T1 and T2 threshold voltage accumulation statistics; (b) cumulative statistics of the "on/off" states of the transistor T2 (SSPF: Sense-Switch pFLASH; Pgm: programming; ERS: erase; Unif: uniformity)

separately, by an ATS-730 high- and low-temperature impact testing machine, and the results are shown in Table 4.

The performance of the designed PLE in this study was compared with that of the PLE in ProASIC3 of ACTEL and the PLE in Virtex-4 of Xilinx, and the results are shown in Table 5.

It can be seen from Table 5 that the PLE in this work had more functions of LUT4 than the PLE in ProASIC3 in a comparable area because the PLE in this work used the 90 nm process, and the operating speed was slightly superior.

The PLE in Virtex-4 can realize all LUT4 functions. One LUT4 is equal to two LUT3; thus, converted to LUT3, it was about 25 μm×25 μm, and its area was the largest among the three, because it needs an additional address decoding circuit. Of course, the PLE in SRAM-based FPGA operated faster compared to the Flash-based FPGA, where the SSPF caused too much delay.

Table 4 Test results of PLE at three temperatures

Function	Symbol	Delay (ns)		
		−55 ℃	25 ℃	125 ℃
INV		0.44	0.47	0.51
AND2		0.52	0.56	0.59
NOR2		0.53	0.57	0.62
AND3		0.66	0.69	0.73
NOR3		0.72	0.77	0.83
XOR3		0.88	0.91	0.98
AND4		0.85	0.88	0.95
NOR4		0.85	0.89	0.96
LATCH	D Q LATCH CK EN	0.96	1.01	1.08
DFF	D R Q DFF CK EN	0.59	0.65	0.71

PLE: programmable logic element; DFF: d flip flop

Table 5 Performance comparison of the designed PLE with ProASIC3 and Virtex-4

Technical index	Virtex-4	ProASIC3	This work
Process (nm)	90	110	90
Type	Volatile	Non-volatile	Non-volatile
Function	LUT4	LUT3 (equivalent)	LUT3+partial LUT4 (equivalent)
Static current (μA)	0.29	0.13	0.11
Delay of DFF (ns)	0.20	0.74	0.65
Delay of AND3 (ns)	0.36	0.75	0.69
Area (μm×μm)	25×50	19×20	18×22

PLE: programmable logic element; DFF: d flip flop; LUT3: three-bit look-up table; LUT4: four-bit look-up table

5 Conclusions

In this paper, a PLE for the Flash-based FPGA has been designed based on SSPF, which can realize

all LUT3 functions, partial LUT4 functions, latch functions, and DFF with enable and reset functions. The LUT4 function of PLE can meet the requirements of the address decoding circuit and digital timing detection, thus improving the utilization of PLE and reducing the overhead of other logic resources. The multifunctional DFF satisfies most of the register requirements of sequential circuits. The die tests of SSPF and PLE show that the "on" state driving current and the "off" state leakage current meet the requirements. The programmable function of PLE is normal, and the delays of both combinatorial logic operations and sequential logic DFF meet the requirements of the design technical specifications.

Contributors

Zhengzhou CAO designed the research. Zhengzhou CAO, Guozhu LIU, and Yanfei ZHANG processed the data. Zhengzhou CAO drafted the paper. Yueer SHAN and Yuting XU helped organize the paper. Zhengzhou CAO, Guozhu LIU, and Yanfei ZHANG revised and finalized the paper.

Conflict of interest

All the authors declare that they have no conflict of interest.

Data availability

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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