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Research on electromagnetic interference resistance performance of three kinds of CMOS inverters

Fangjun LIU, Jiaming SHEN, Jizhong SHEN‡

College of Information Science and Electronic Engineering, Zhejiang University, Hangzhou 310027, China

E-mail: 22231034@zju.edu.cn; 22131029@zju.edu.cn; jzshen@zju.edu.cn

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Abstract: The performance of complementary metal oxide semiconductor (CMOS) circuits is affected by electromagnetic interference (EMI), and the study of the circuit's ability to resist EMI will facilitate the design of circuits with better performance. Current-mode CMOS circuits have been continuously developed in recent years due to their advantages of high speed and low power consumption over conventional circuits under the deep submicron process; their EMI resistance performance deserves further study. This paper introduces three kinds of NOT gate circuits: conventional voltage-mode CMOS, MOS current-mode logic (MCML) with voltage signal of input and output, and current-mode CMOS with current signal of input and output. The effects of EMI on three NOT gate circuits are investigated using Cadence Virtuoso software simulation, and a disturbance level factor is defined to compare the effects of different interference terminals, interference signals' waveforms, and interference signals' frequencies on the circuits in the 65 nm process. The relationship between input resistance and circuit EMI resistance performance is investigated by varying the value of cascade resistance at the input of the current-mode CMOS circuits. Simulation results show that the current-mode CMOS circuits have better resistance performance to EMI at high operating frequencies, and the higher the operating frequency of the current-mode CMOS circuits, the better the resistance performance of the circuits to EMI. Additionally, the effects of different temperatures and different processes on the resistance performance of three circuits are also studied. In the temperature range of −40 ℃ to 125 ℃, the higher the temperature, the weaker the resistance ability of voltage-mode CMOS and MCML circuits, and the stronger the resistance ability of current-mode CMOS circuits. In the 28 nm process, the current-mode CMOS circuit interference resistance ability is relatively stronger than that of the other two kinds of circuits. The relative interference resistance ability of voltage-mode CMOS and MCML circuits in the 28 nm process is similar to that of the 65 nm process, while the relative interference resistance ability of current-mode CMOS circuits in the 28 nm process is stronger than that of the 65 nm process. This study provides a basis for the design of current-mode CMOS circuits against EMI.

Key words: Voltage-mode complementary metal oxide semiconductor (CMOS); MOS current-mode logic (MCML); Current-mode CMOS; Electromagnetic interference (EMI); Inverter

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1 Introduction

Electronic products in the economy, social life, and national defense have a wide range of field applications, and current updates to electronic products cannot be separated from the design of internal circuits. With the continuous development of technology and product demand, the development of low-voltage and low-power integrated circuits (ICs) is a market trend, and the technology scaling of circuits induces a reduction in power supply voltage and noise margin (Kim and Iliadis, 2007a; Richelli, 2012). Electromagnetic interference (EMI), including conducted, coupled, and radiated disturbances, can lead to distortion phenomena, direct current shift, and other effects, hindering electronic circuits and devices from functioning properly (Zupan

‡ Corresponding author
ORCID: Fangjun LIU, https://orcid.org/0009-0004-5624-559X; Jizhong SHEN, https://orcid.org/0000-0002-9031-2379

and Deutschmann, 2020). In military applications, weapons' failure due to EMI (Backstrom and Lovstrand, 2004; Hu et al., 2023) can determine victory or defeat in a war. In the civilian field, EMI in the medical, communication, and aircraft manufacturing fields (Richelli et al., 2003; Albertson et al., 2006) has created many inconveniences; thus the EMI resistance ability of electronic equipment needs to be improved, and it is necessary to study circuit EMI resistance performance. The current main EMI resistance technology aims to protect electromagnetic equipment, and most EMI resistance design is from the distance and shielding (Radasky et al., 2004), which is not suitable for submicron technologies due to increased volume and cost (Choudhary et al., 2021). There is a lack of circuit design at the level of circuit structure for EMI resistance. Based on the EMI resistance performance of the circuit structure, the designed circuit has practical application value. The main part of the current electronic system is the digital circuit, which has the advantages of a simple structure, easy integration, and large noise margin. In digital circuits, most ICs use a metal oxide semiconductor field effect transistor (MOSFET), which can be designed with different structures of gate circuits. Different gate structures have different EMI resistance performances with respect to electromagnetic radiation. NOT gates are the most important and basic digital units, also known as inverters, so the study of EMI resistance performance of inverters is of great significance to the study of EMI resistance performance in digital systems (Wang HY et al., 2008). Currently, the most widely used inverter is the voltage-mode complementary metal oxide semiconductor (CMOS) NOT gate, and MOS current-mode logic (MCML) with voltage signals of input and output is an important current-mode CMOS circuit with high-speed, low-noise characteristics (Liang et al., 2012). Current-mode CMOS with current signals of input and output (Yao and Sun, 2019) also has high-speed, low-noise characteristics, and has low-power characteristics in the deep submicron process (Gupta et al., 2021). The effect of power and pulse width of the injected electromagnetic pulse on the performance of voltage-mode inverters has been investigated in the literature (Lin et al., 2021), and the latch-up of voltage-mode inverters induced by electromagnetic pulses has also been investigated (Wang HY et al., 2017). These studies compare the performance of EMI-resistant MCML circuits and propose a source-buffered differential pair with high EMI immunity (Redouté and Steyaert, 2010). However, there is a lack of research on the EMI resistance performance of current-mode CMOS circuits. Therefore, three circuits are selected to study their EMI resistance performance. In the EMI environment, electromagnetic waves are often coupled into the circuits through the "front door" or "back door" paths (Wang HY et al., 2008), and EMI signals coupled to the internal circuits are generally formed by the interference pulse voltage (Kim and Iliadis, 2007b). Most of the EMI signals are sine waves and rectangular waves (Wunsch and Bell, 1968; Singh, 2017), so we study the effect of the direct injection of sine waves and rectangular waves into the circuits. In this paper, circuit simulations are carried out by Cadence Virtuoso simulation software to study and compare the effect of applied interference on the circuits by directly injecting the interference voltage signals into three different CMOS NOT gate circuits. In addition, current-mode CMOS circuits use current as a signal, and have the advantages of high speed, low power consumption, and high EMI resistance performance over voltage-mode CMOS circuits under the deep submicron process. EMI signals are generally voltage pulses, so it can be expected that the current-mode CMOS circuits will have a better EMI resistance performance compared to the other two kinds of CMOS circuits.

2 Three circuit structures

In digital circuit design, the NOT gate (including NAND gate and NOR gate) is an indispensable basic and important unit, so it is selected for EMI resistance performance research. In this paper, three different principles of NOT gates are selected for investigation, and the three circuit structures are described below.

Voltage-mode CMOS NOT gate requires fewer MOS transistors and has a simple structure (Powell et al., 2018) as shown in Fig. 1, and its output is inverted with its input.

MCML is a current-mode circuit; its input and output signals are differential voltages, and internally the current signals are used as logic signals, which consist of a constant-current source, a pull-down switching network, and a pull-up load resistor (Yamashina and

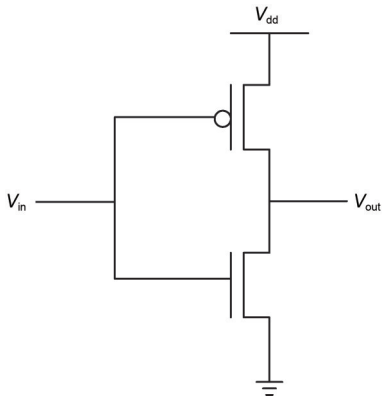

Fig. 1 Voltage-mode complementary metal oxide semiconductor (CMOS) NOT gate

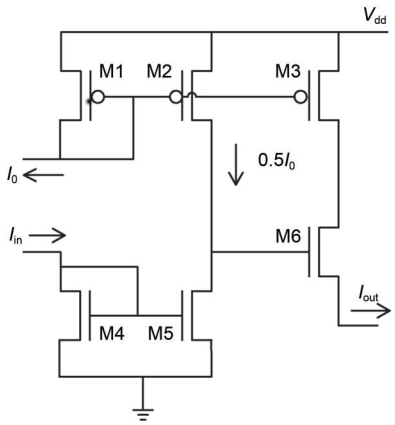

Fig. 3 Current-mode CMOS NOT gate

Yamada, 1992; Hassan et al., 2005). The signals are inputted to the circuit in differential voltages, and the pull-down switching network controls the circuit so that one side of the path is on and the other side of the pathway is off, and the constant current is only outputted through one side of the pathway. The structure of the MCML NOT gate is shown in Fig. 2. When the input voltage V_{in} is high, positive channel metal oxide semiconductor (PMOS) transistor M1 is cut off, N-metal oxide semiconductor (NMOS) transistor M3 is on, and the output voltage V_{out} is low; when the input voltage V_{in} is low, PMOS transistor M1 is on, NMOS transistor M3 is cut off, and the output voltage V_{out} is high.

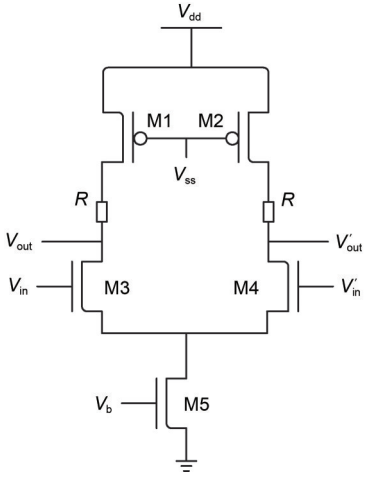

Fig. 2 MOS current-mode logic (MCML) NOT gate

Current-mode CMOS circuits use current signals as input and output signals and therefore have significant advantages in designing circuits with arithmetic functions (Yao and Sun, 2019). The structure of the NOT gate is shown in Fig. 3. The threshold current I_0 is inputted into the circuit through the PMOS current mirror, and the input current signal I_{in} is copied by the NMOS current mirror and compared with $0.5I_0$. When I_{in} is 0, the current comparator consisting of M1, M2, M4, and M5 outputs a high level, the NMOS transistor M6 is on, and the output current signal I_{out} equals I_0; when I_{in} equals I_0, the current comparator outputs a low level, the NMOS transistor M6 is cut off, and the output current signal I_{out} is 0.

3 Definition of the disturbance level

To compare the EMI resistance performance of circuits, a disturbance level factor λ is defined. It is assumed that the logic value 1 and logic value 0 of the output of the circuit correspond to voltage or current values whose difference is α when the circuit is not disturbed, and the difference between the actual output voltage or current value and the theoretical value is β after the circuit is disturbed. Define $\lambda=\beta/\alpha$, and when the value of λ is larger, this means that the circuit is subject to a deeper degree of EMI, and the circuit has a weaker EMI resistance ability. Since the output has two possibilities of logic value 1 or logic value 0, the circuit has two corresponding values of λ, and we scientifically take the larger value as the circuit's λ. λ can be calculated from both voltage and current values, which is conducive to comparing the EMI resistance performance of voltage-mode and current-mode circuits.

In the practical application of digital circuits, usually the high (low) level of the allowable input and output of the gate circuit is a range. By consulting datasheets from leading companies in the industry, the allowable high (low) level input range of logic gates for most of the currently used standard CMOS processes is around 25%. Accordingly, λ is divided into three intervals depending on the magnitude of the effect of the interference on the output. λ<0.25 means that the interference is small, and the output value is in the interval of the permissible output, which can drive the next circuit properly, and it is considered that the circuit logic correctness is not affected by the EMI; 0.25≤λ≤0.75 means that the interference is large, the output value is not in the permissible output interval, the output logic is uncertain, and the circuit is affected by the EMI; λ>0.75 means that the interference is large, the output value exceeds the permissible output interval, and the output logic flips to the opposite logic, that is, a logic error.

4 Effect of EMI signal injection terminal on the circuits

EMI can easily affect the whole system through the "front door" (signal receiving antenna) and "back door" (power lines, signal transmission lines, etc.) of electronic devices. Electromagnetic attacks will lead to EMI waves at the pins of the IC. IC pins can usually be subdivided into power, input, and output terminals, which means that interfering signals can generally penetrate the circuits from either the power pin or the input/output pins (Redouté and Richelli, 2015). The following simulations are carried out by direct injection interference signals from different terminals to simulate the impact of EMI on the circuits and compare the EMI's effect on the outputs.

Circuits are designed in Taiwan semiconductor manufacturing company limited (TSMC)'s 65 nm CMOS technology in Cadence Virtuoso. Simulation parameters are set as follows: the simulation temperature is set at 27 ℃, the width-to-length ratio (W/L) of the PMOS transistor is set to 600 nm/300 nm, W/L of the NMOS transistor is set to 400 nm/300 nm, and the power supply is set to 2 V, while the simulation results prove that the logic function of the three kinds of NOT gates are correct. The interfering signal is a sine signal (Richelli et al., 2003) with a frequency of 100 MHz, which is injected into the circuits from the power supply, the signal input, and the output, respectively. For input signals with both high and low levels, the outputs are subjected to different levels of interference, the higher level of interference will be recorded, and the subsequent simulation is the same.

4.1 Voltage-mode CMOS NOT gate

According to Fig. 1, the simulation parameters are set as follows: the input voltage V_{in} is a square wave with an amplitude of 2 V and a period of 40 ns, and the amplitude of the interference signal varies from 0.2 to 1.6 V.

The variation of the disturbance level factor λ with the injection terminal and amplitude of the interference signal is shown in Table 1, and the corresponding line graph is plotted in Fig. 4. The simulated output transient

Table 1 Variation of λ of voltage-mode CMOS NOT gate with injection terminal and amplitude of sine wave interference signal

Interference amplitude (V)	λ		
	Power pin	Signal input pin	Output pin
0.2	0.100	0.000	0.100
0.4	0.200	0.000	0.200
0.5	0.250	0.000	0.250
0.6	0.300	0.000	0.300
0.8	0.400	0.030	0.400
1.0	0.500	0.885	0.500
1.2	0.600	0.985	0.600
1.4	0.700	0.995	0.700
1.5	0.750	0.996	0.750
1.6	0.800	1.000	0.800

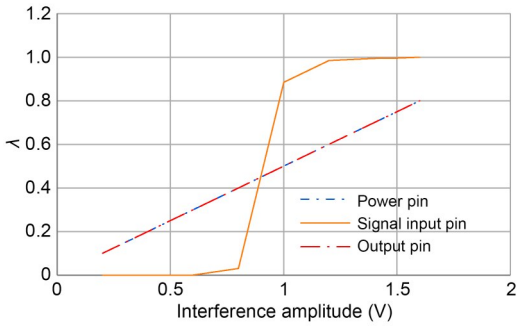

Fig. 4 Variation of λ of voltage-mode CMOS NOT gate with injection terminal and amplitude of sine wave interference signal

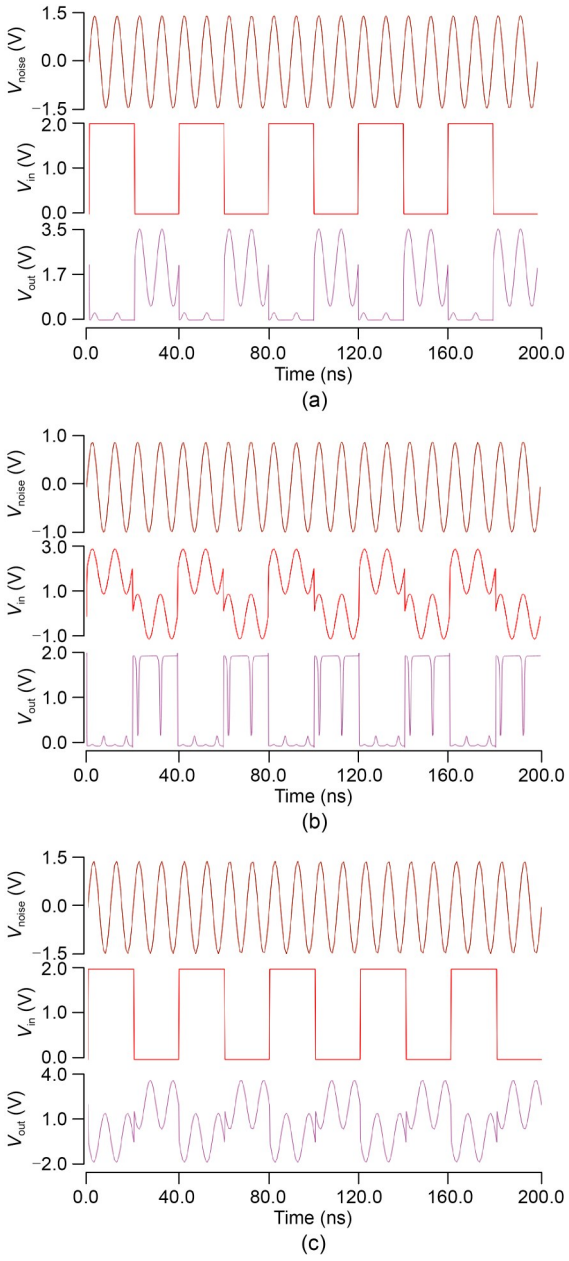

Fig. 5 Simulated output transient waveforms of a voltage-mode CMOS NOT gate when a logic error occurs due to a sine interference signal: (a) interference injected from the power supply pin; (b) interference injected from the signal input; (c) interference injected from the output

waveform of the circuit, when a logic error occurs due to the interference of a sine signal, is shown in Fig. 5, and the waveforms are the interference signal, the input signal, and the output signal, in order from the top to the bottom. The waveforms of circuits in the following simulated output transient waveforms figures are in the same order.

Conclusions can be drawn from Table 1 as follows:

(1) In the case where the interference signal is injected from the power supply pin, when the amplitude of the interference signal is greater than 0.5 V and λ>0.25, the circuit is interfered with; when the amplitude of the interference signal is greater than 1.5 V and λ>0.75, the circuit output logic is erroneous.

(2) In the case where the interference signal is injected from the signal input, when the amplitude of the interference signal is greater than 1 V and λ>0.75, the circuit output logic is erroneous.

(3) In the case that the interference signal is injected from the output, the circuit is disturbed when the amplitude of the interference signal is greater than 0.5 V and λ>0.25; when the amplitude of the interference signal is greater than 1.5 V and λ>0.75, the circuit output logic is erroneous.

(4) Comparing the three kinds of circuits, for voltage-mode CMOS NOT gate, the interference signal is injected from the input pin to have a greater impact on the circuit, and when the amplitude of the interference signal is incremented to about 1 V, the output result is disturbed by the rapid change. Because the signal is injected from the output without using the logic function of the circuit, the disturbance level of the circuit changes linearly with the increase in the amplitude of the interference signal.

4.2 MCML NOT gate

According to Fig. 2, the simulation parameters are set so that the circuit operates in the right state with a resistor R of 800 kΩ, the input voltage V_{in} is a square wave with an amplitude of 2 V and a period of 40 ns, and the amplitude of the interference signal varies from 0.2 to 1.6 V.

The variation of the disturbance level factor λ with the injection terminal and amplitude of the interference signal is shown in Table 2, and the corresponding line graph is plotted in Fig. 6. The simulated output transient waveforms of the circuit when a logic error occurs due to the interference of a sine signal is shown in Fig. 7.

Conclusions can be drawn from Table 2 as follows:

(1) In the case where the interference signal is injected from the power supply pin, when the amplitude of the interference signal is greater than 0.5 V and λ>0.25, the circuit is disturbed; when the amplitude

Table 2 Variation of λ of MCML NOT gate with injection terminal and amplitude of sine wave interference signal

Interference amplitude (V)	λ		
	Power pin	Signal input pin	Output pin
0.2	0.100	0.000	0.100
0.4	0.200	0.000	0.200
0.5	0.250	0.000	0.250
0.6	0.300	0.105	0.300
0.7	0.350	0.430	0.350
0.8	0.400	0.935	0.400
1.0	0.500	0.965	0.500
1.2	0.600	0.970	0.600
1.4	0.700	0.975	0.700
1.5	0.750	0.975	0.750
1.6	0.800	0.975	0.800

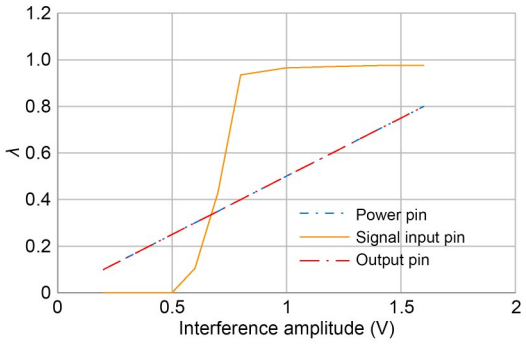

Fig. 6 Variation of λ of MCML NOT gate with injection terminal and amplitude of sine wave interference signal

of the interference signal is greater than 1.5 V and λ> 0.75, the circuit output logic is erroneous.

(2) In the case where the interference signal is injected from the signal input, when the amplitude of the interference signal is greater than 0.7 V and λ>0.25, the circuit is disturbed; when the amplitude of the interference signal is greater than 0.8 V and λ>0.75, the circuit output logic is erroneous.

(3) In the case where the interference signal is injected from the output, when the amplitude of the interference signal is greater than 0.5 V and λ>0.25, the circuit is disturbed; when the amplitude of the interference signal is greater than 1.5 V and λ>0.75, the circuit output logic is erroneous.

(4) Comparing the above three cases, for the MCML NOT gate, the interference signal injected from the input has a greater impact on the circuit, and the output result is erroneous when the amplitude of the interference signal is incremented to 0.8 V.

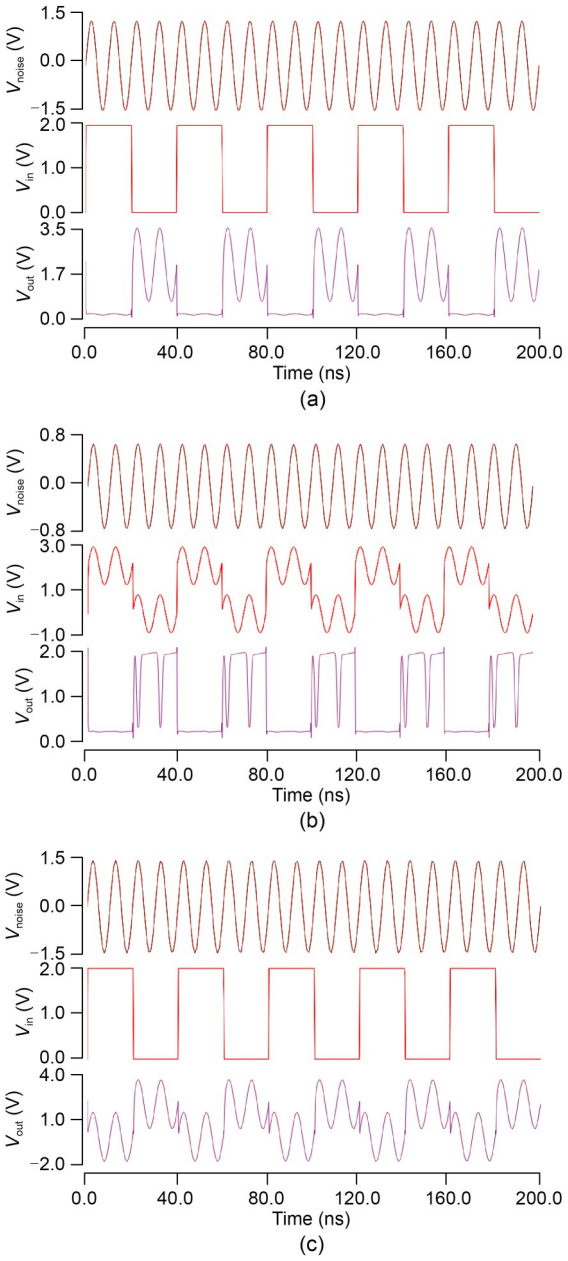

Fig. 7 Simulated output transient waveforms of an MCML NOT gate when a logic error occurs due to a sine interference signal: (a) interference injected in the power supply pin; (b) interference injected in the signal input; (c) interference injected in the output

4.3 Current-mode CMOS NOT gate

According to Fig. 3, the threshold current I_0 is set to 20 μA and the input current I_{in} is a square wave

with an amplitude of 20 μA and a period of 40 ns. The interfering signal is used as a voltage source with an amplitude varying from 0.2 to 2.4 V, and an equivalent input resistor R_1 of a current-mode CMOS NOT gate is connected in series so that the circuit is fed with the interfering current. According to theoretical calculations and simulation results (Razavi, 2008), the input impedance of the 65 nm process current-mode CMOS NOT gate is about 150 kΩ when the interfering signal is a sine wave of 100 MHz, so we connect the interfering source in series with a 150 kΩ resistor so that the interfering signal power is maximally input into the circuit. Subsequently, we will investigate different resistors in series for different frequencies of interfering signals in Section 6.

The variation of the disturbance level factor λ with the injection terminal and amplitude of the interference signal is shown in Table 3, and the corresponding line graph is plotted in Fig. 8. The simulated output transient waveform of the circuit when a logic error occurs due to the interference of a sine signal is shown in Fig. 9.

Conclusions can be drawn from Table 3 as follows:

(1) In the case where the interference signal is injected from the power supply pin, when the amplitude of the interference signal is greater than 1.1 V and λ>0.25, the circuit is disturbed; when the amplitude of the interference signal is greater than 1.2 V and λ>0.75, the output logic of the circuit is erroneous.

(2) In the case where the interference signal is injected from the signal input, when the amplitude of the interference signal is greater than 0.6 V and λ>0.25, the circuit is disturbed; when the amplitude of the interference signal is greater than 0.7 V and λ>0.75, the output logic of the circuit is erroneous.

(3) In the case where the interference signal is injected from the output, when the amplitude of the interference signal is greater than 0.8 V and λ>0.25, the circuit is disturbed; when the amplitude of the interference signal is greater than 2.3 V and λ>0.75, the output logic of the circuit is erroneous.

(4) In the case where the interference signal is injected from the threshold current input pin, the circuit is interfered with when the amplitude of the interference signal is greater than 1.1 V and λ>0.25; when the amplitude of the interference signal is greater than 2.2 V and λ>0.75, the output logic of the circuit is erroneous.

(5) For the current-mode CMOS NOT gate, the interference signal injected from the signal input has a greater degree of influence on the circuit, and when the amplitude of the interference signal is incremented to 0.7 V, the output result is erroneous.

Table 4 lists the voltage amplitude required by the three circuits to have logic errors at different interference signal injection terminals.

Conclusions can be obtained from Table 4 as follows:

Table 3 Variation of λ of current-mode CMOS NOT gate with injection terminal and amplitude of sine wave interference signal

Interference amplitude (V)	λ			
	Power pin	Signal input pin	Output pin	Threshold current input pin
0.2	0.000	0.000	0.064	0.073
0.4	0.000	0.012	0.134	0.117
0.6	0.000	0.443	0.195	0.167
0.7	0.000	1.210	0.220	0.187
0.8	0.000	1.340	0.260	0.207
1.0	0.075	1.475	0.320	0.243
1.1	0.495	1.500	0.360	0.257
1.2	0.765	1.540	0.385	0.283
1.4	1.000	1.600	0.450	0.330
1.6	1.000	1.660	0.518	0.410
1.8	1.000	1.718	0.584	0.427
2.0	1.000	1.750	0.650	0.460
2.2	1.000	1.775	0.730	0.837
2.3	1.000	1.800	0.783	1.125
2.4	1.000	1.800	0.784	1.365

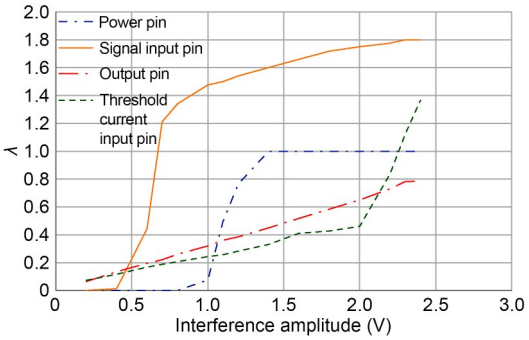

Fig. 8 Variation of λ of current-mode CMOS NOT gate with injection terminal and amplitude of sine wave interference signal

(1) When a sine interference with 100 MHz is injected into the circuits, the injection from the signal input has the strongest interference effect on the circuits, and the circuits have the weakest resistance ability to interference.

(2) When a sine interference with 100 MHz is injected from the signal input, the voltage-mode CMOS NOT gate has the strongest resistance ability to interference; when a sine interference with 100 MHz is injected from the signal output, the current-mode CMOS NOT gate has the strongest resistance ability to interference.

(3) When a sine interference with 100 MHz is injected into the circuits from the power supply pin, the resistance performance of the three circuits is similar.

Table 4 Voltage amplitude required by the three circuits to have logic errors at different interference signal injection terminals

Injection terminal	Voltage (V)		
	Voltage-mode	MCML	Current-mode
Power supply pin	1.5	1.5	1.2
Signal input pin	1.0	0.8	0.7
Output pin	1.5	1.5	2.3

5 Effects of EMI waveforms on circuits

Common interference styles include pseudorandom signal, monotone, and narrow-band interference (Mu and Jia, 2021), and the EMI signal emitted by the jammer can be simplified and approximated as a sine wave or a rectangular wave; so on the basis of the study of sine interference signals, it is necessary to study the EMI effects of rectangular wave signals on

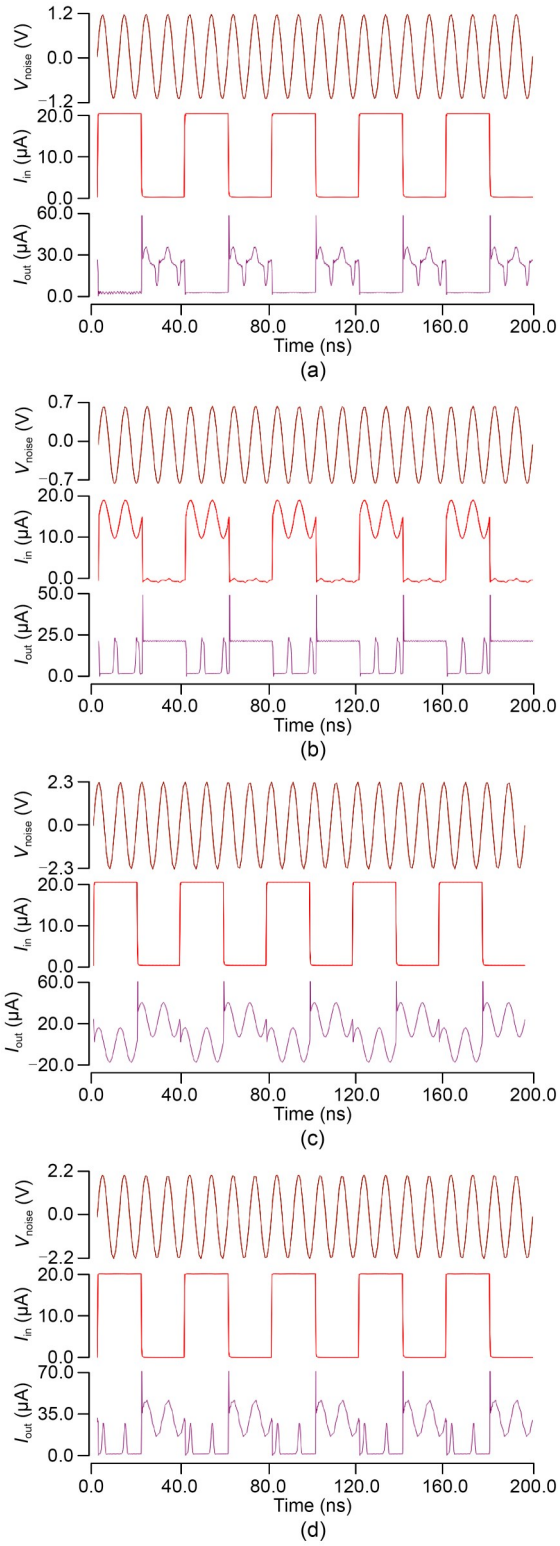

Fig. 9 Simulated output transient waveforms of a current-mode CMOS NOT gate when a logic error occurs due to a sine interference signal: (a) interference injected from the power supply pin; (b) interference injected from the signal input; (c) interference injected from the output; (d) interference injected from the threshold current input

the circuits. Sine wave is characterized by a gradual change in signal amplitude, and the constantly changing sine interference signal has a continuous effect on the circuit, while the rectangular wave is characterized by a short rise time, a wide frequency distribution, and many high-frequency components (Wang GJ et al., 2022). The following is a comparison of the EMI effects of sine and rectangular wave signals on the circuits in each of the three circuits. According to the previous simulation results, since the interference signal injected at the input has a relatively large effect on the circuits, here we just study the effect of different interference signal waveforms on the circuits when they are injected from the input.

The interference signal is selected as a square wave signal without loss of generality (Deutschmann and Winkler, 2023), which has a frequency of 100 MHz and an amplitude varying from 0.2 to 2.5 V, and the rest of the simulation parameters are the same as those in Section 4. Combined with the simulation results of sine wave interference in Section 3, the variation of λ of the three NOT gates with the waveform and amplitude of the interference signal is shown in Table 5, and the corresponding line graphs are plotted as in Fig. 10. The simulated output transient waveforms of the circuit when a logic error occurs due to interference of a square wave signal are shown in Fig. 11.

Conclusions can be drawn from Table 5 as follows:

(1) For the voltage-mode CMOS inverter, the two interference waves have a similar trend of influence on the circuit, and both of them cause the circuit to output a logic error when the amplitude of the interference signal is 1 V.

(2) For the MCML inverter, the two interference waves have a similar trend of influence on the circuit, and both of them cause the circuit to output a logic error when the amplitude of the interference signal is 0.8 V.

(3) For the current-mode CMOS inverter, the sine interference has a greater impact on the circuit, and the output logic of the circuit is error when the amplitude of the sine interference signal is 0.7 V, while the output logic of the circuit is erroneous when the amplitude of the square wave interference signal is 2.5 V.

(4) In the sine wave interference, the voltage-mode CMOS circuit interference resistance ability is stronger; in the square wave interference, the current-mode CMOS circuit interference resistance ability is significantly stronger than that of the other two kinds of circuits. Due to the current-mode CMOS NOT gate being more complex, the intrinsic capacitance of the circuit is larger, and it filters the high-frequency component of the square wave much more strongly, and the circuit is less disturbed.

6 Effects of EMI frequencies on circuits

Using simulations, it is found that the circuits are disturbed to different degrees with different frequencies

Table 5 Variation of λ of the three NOT gates with the waveform and amplitude of the interference signal

Interference amplitude (V)	λ of voltage-mode		λ of MCML		λ of current-mode	
	Square wave	Sine wave	Square wave	Sine wave	Square wave	Sine wave
0.2	0.020	0.000	0.000	0.000	0.000	0.000
0.4	0.035	0.000	0.025	0.000	0.000	0.012
0.6	0.050	0.000	0.050	0.105	0.000	0.443
0.7	0.070	0.000	0.455	0.430	0.000	1.210
0.8	0.100	0.030	0.935	0.935	0.000	1.340
1.0	0.885	0.885	0.965	0.965	0.000	1.475
1.2	1.000	0.985	0.970	0.970	0.000	1.540
1.4	1.000	0.995	0.975	0.975	0.000	1.600
1.6	1.000	1.000	0.975	0.975	0.000	1.660
1.8	–	–	–	–	0.000	1.718
2.0	–	–	–	–	0.000	1.750
2.2	–	–	–	–	0.000	1.775
2.4	–	–	–	–	0.256	1.800
2.5	–	–	–	–	0.944	1.854

"–" represents no data

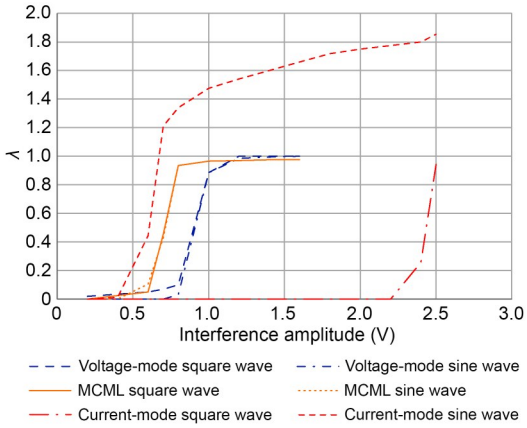

Fig. 10 Variation of λ of the three NOT gates with the waveform and amplitude of the interference signal

of the EMI sources, due to equivalent intrinsic capacitors in the circuits, and the capacitors have different filtering abilities for high-frequency and low-frequency EMI. For this reason, we compare the EMI effects of the interference sources on the three circuits at frequencies of 1 GHz and 100 MHz. According to the previous simulation results, since the interference signal injected from the input has a relatively large effect on the circuits, we study the interference signal injected from the input, and since the sine interference signal interferes more greatly with the circuits, here we only study the effect of different frequencies' sine interference signals on the circuits.

The three circuits are simulated separately, with the interference frequency of 1 GHz and the amplitude varying from 0.2 to 1.6 V, and the rest of the simulation parameters are the same as those in Section 4. Combined with the simulation results of the 100 MHz frequency interference in Section 3, the variation of λ of three kinds of NOT gates with the frequency and amplitude of the sine interference signal is shown in Table 6, and the corresponding line graph is plotted as in Fig. 12. The simulated output transient waveforms of the circuit when a logic error occurs due to the interference of the 1 GHz signal are shown in Fig. 13.

Conclusions can be drawn from Table 6 as follows:

(1) In the three kinds of NOT gates, when the interference frequency is increased from 100 MHz to 1 GHz, λ becomes smaller, the degree of interference in the circuits is weakened, and the disturbance voltage levels that invert output logic of voltage-mode CMOS,

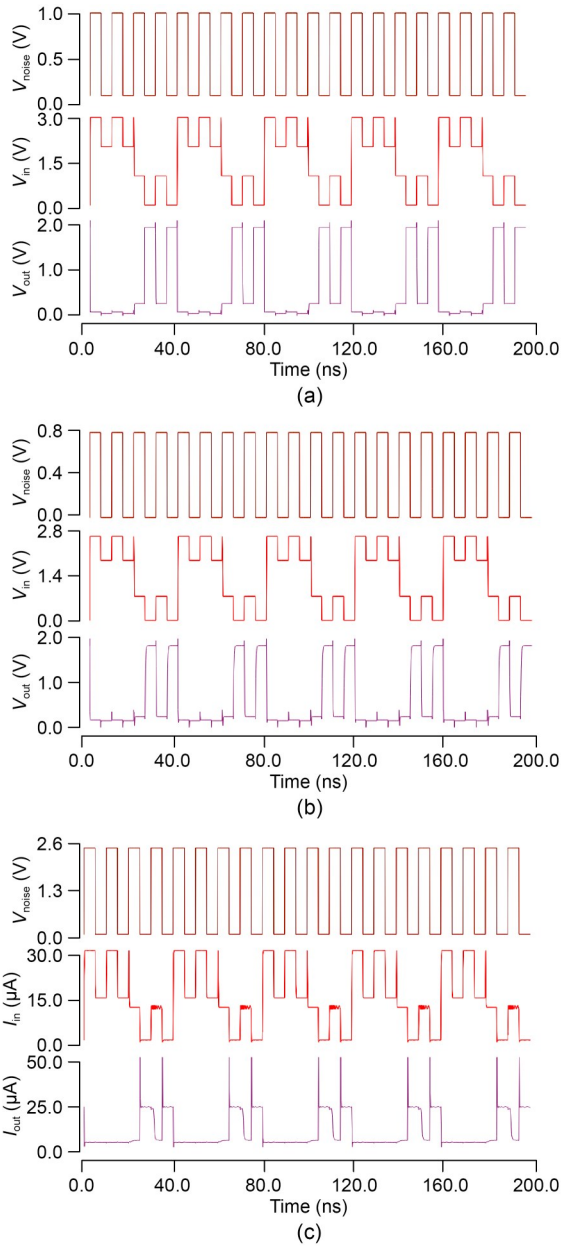

Fig. 11 Simulated output transient waveforms of three NOT gate circuits when a logic error occurs due to a square wave interference signal: (a) voltage-mode; (b) MCML; (c) current-mode

MCML, and current-mode CMOS NOT gates become larger, changing from 1 V, 0.8 V, and 0.7 V, to 1.1 V, 0.9 V, and 1.2 V, respectively.

(2) When injecting interference from the signal input, due to the intrinsic capacitance in the circuit for high-frequency interference to provide a much stronger coupling to the ground path, suppressing part of the interference, the higher the frequency of the

Table 6 Variation of λ of three kinds of NOT gates with the frequency and amplitude of the sine wave interference signal

Interference amplitude (V)	λ of voltage-mode		λ of MCML		λ of current-mode	
	f=1 GHz	f=100 MHz	f=1 GHz	f=100 MHz	f=1 GHz	f=100 MHz
0.2	0.000	0.000	0.020	0.000	0.000	0.000
0.4	0.005	0.000	0.040	0.000	0.000	0.012
0.6	0.010	0.000	0.070	0.105	0.060	0.443
0.7	0.010	0.000	0.190	0.430	0.070	1.210
0.8	0.025	0.030	0.580	0.935	0.080	1.340
0.9	0.079	0.090	0.965	0.960	0.155	1.400
1.0	0.425	0.885	0.990	0.965	0.310	1.475
1.1	0.955	0.960	0.990	0.970	0.560	1.513
1.2	0.985	0.985	0.990	0.970	0.950	1.540
1.4	1.000	0.995	0.990	0.975	1.590	1.600
1.6	1.000	1.000	0.990	0.975	1.970	1.660

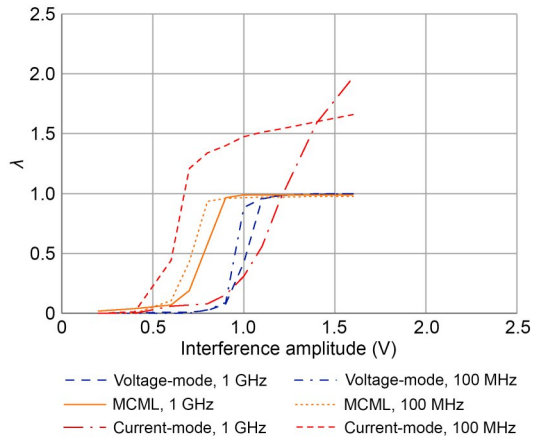

Fig. 12 Variation of λ of three kinds of NOT gates with the frequency and amplitude of the sine wave interference signal

interference signal, the stronger the circuit inhibition of the interference signal, and the higher the amplitude of the interference voltage required for the output logic to occur error, the stronger the circuit's ability to resist interference.

(3) In the 100 MHz interference frequency, the voltage-mode CMOS circuits are more resistant to interference; in the 1 GHz interference frequency, the current-mode CMOS circuits have significantly better interference resistance performance. The working frequency of modern digital ICs is getting higher and higher. Compared with the other two kinds of circuits, the current-mode CMOS circuits are more capable of resisting high-frequency interference and will satisfy more resistance applications.

7 Effects of temperatures and processes on circuits

MOSFET devices exhibit different performances at different temperatures and processes, and the threshold voltage V_{TH} and mobility μ_n of MOSFETs are both affected by temperature (Razavi, 2000). Thus, the effect of different temperatures and processes on the resistance performance of three kinds of circuits is investigated. According to the previous simulation results, since the interference signal injected from the input has a relatively large effect on the circuits, we study the interference signal injected from the input. Since the sine interference signal interferes more greatly with the circuits, here we study the effect of sine interference signals on the circuits, which have a frequency of 100 MHz and an amplitude varying from 0.2 to 1.0 V.

7.1 Simulation at different temperatures

The three circuits are designed in TSMC's 65 nm CMOS technology in Cadence Virtuoso. This subsection simulates the experiments of three circuits to resist interference at the lowest (−40 ℃) and highest (125 ℃) temperatures in the operating temperature range of a general electronic system and at two intermediate temperatures (0 ℃, 50 ℃), and compares the results of the experiments with the original experiments under a temperature of 27 ℃. The rest of the simulation parameters are the same as those in Section 4. The variation of λ of three kinds of NOT

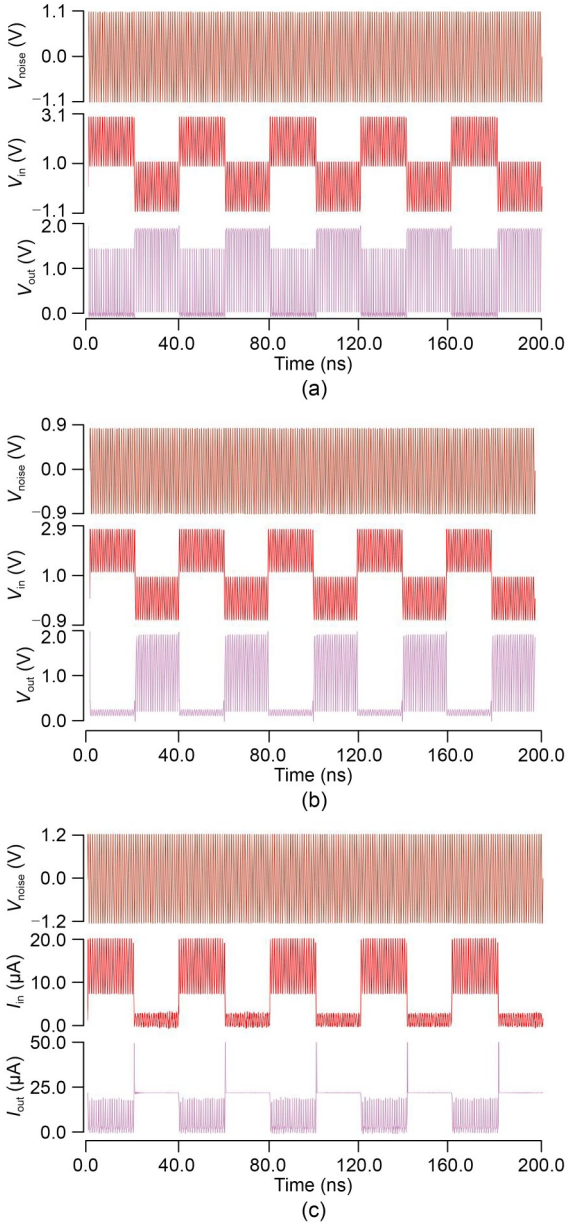

Fig. 13 Simulated output transient waveforms of three NOT gates when a logic error occurs due to a 1 GHz sine interference signal: (a) voltage-mode; (b) MCML; (c) current-mode

gates with temperatures and amplitudes of the sine interference signal is shown in Table 7, and the corresponding line graph is plotted as in Fig. 14.

Conclusions can be drawn from Table 7 as follows:

(1) The interference signal amplitude is within a certain range for voltage-mode CMOS and MCML circuits; the higher the temperature, the larger the degree of output voltage offsets, the larger the degree of disturbance to the circuit, and the weaker the circuit's ability to resist interference. The main reason for this is that the resistance between the drain and the source of the MOSFET is approximated as $R_{on}=\frac{1}{\mu_n C_{OX}\left(\frac{W}{L}\right)(V_{GS}-V_{TH})}$ (Razavi, 2000), where C_{OX} is the gate oxide capacitance per unit area. As the temperature rises, the lower the carrier mobility μ_n, the higher the value of the drain-source resistance, the higher the drain-source voltage drop, and the larger the degree of output voltage offset.

(2) For current-mode CMOS circuits, the higher the temperature, the smaller the degree of output current offsets, the smaller the degree of interference with the circuit, and the stronger the circuit's ability to resist interference. The main reason for this is that the saturation drain-source current of the MOSFET is expressed as $I_D=\frac{1}{2}\mu_n C_{OX}\left(\frac{W}{L}\right)(V_{GS}-V_{TH})^2$. The higher the temperature, the lower the carrier mobility μ_n (Razavi, 2000), and the smaller the current offset.

7.2 Simulation in 28 nm process

To compare the impact of different processes, the three circuits are simulated again in TSMC's 28 nm process. The setting of the simulation parameters is as follows: the simulation temperature is set at 27 ℃, for the voltage-mode CMOS and MCML NOT gate, *W*/*L* of the PMOS transistor is set to 100 nm/30 nm, *W*/*L* of the NMOS transistor is set to 100 nm/30 nm, and the power supply is set to 1 V. The input voltage V_{in} is a square wave with an amplitude of 1 V and a period of 40 ns. For the current-mode CMOS NOT gate, the threshold current I_0 is set to 10 μA, and the input current I_{in} is a square wave with an amplitude of 10 μA and a period of 40 ns. For the circuit to perform properly and output a 10 μA current, *W*/*L* of the NMOS transistor is set to 100 nm/30 nm, while *W*/*L* of the PMOS transistors M1, M2, and M3 is set to 300 nm/30 nm, 180 nm/30 nm, and 170 nm/30 nm, respectively.

Due to the fact that circuits manufactured in different processes use different supply voltages, to compare the resistance of circuits in different processes fairly, we define a relative interference resistance parameter η, which is the ratio of the interference voltage V_{noise}, which is just enough to make the circuit's output logic errors to the power supply voltage. A larger η indicates

Table 7 Variation of λ of three kinds of NOT gates with different temperatures and amplitudes of the sine wave interference signal

NOT gate	Temperature (°C)	λ						
		Amplitude=0.2 V	0.4 V	0.6 V	0.7 V	0.8 V	0.9 V	1.0 V
Voltage-mode	−40	0.000	0.000	0.000	0.000	0.020	0.060	0.885
	0	0.000	0.000	0.000	0.000	0.025	0.075	0.885
	27	0.000	0.000	0.000	0.000	0.030	0.090	0.885
	50	0.000	0.000	0.000	0.000	0.035	0.100	0.885
	125	0.000	0.000	0.000	0.000	0.050	0.125	0.885
MCML	−40	0.000	0.000	0.075	0.210	0.790	0.960	0.965
	0	0.000	0.000	0.075	0.340	0.920	0.960	0.965
	27	0.000	0.000	0.105	0.430	0.935	0.960	0.965
	50	0.000	0.005	0.155	0.510	0.940	0.960	0.965
	125	0.000	0.015	0.310	0.755	0.940	0.960	0.965
Current-mode	−40	0.000	0.017	0.630	1.275	1.400	1.460	1.515
	0	0.000	0.012	0.505	1.245	1.365	1.430	1.485
	27	0.000	0.012	0.443	1.210	1.340	1.410	1.475
	50	0.000	0.003	0.415	1.195	1.330	1.390	1.455
	125	0.000	0.000	0.315	1.070	1.285	1.355	1.405

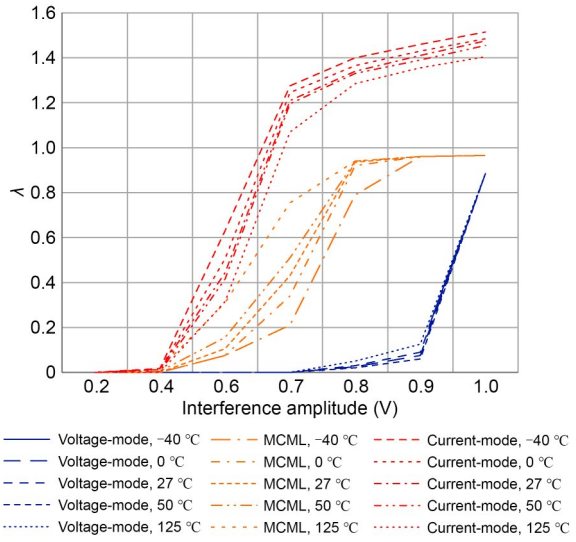

Fig. 14 Variation of λ of three kinds of NOT gates with temperatures and amplitude of the sine wave interference signal

Table 8 Voltage amplitude required by the three circuits to have logic errors and η values in different processes

NOT gate	V_{noise} (V)		η	
	28 nm	65 nm	28 nm	65 nm
Voltage-mode	0.50	1.00	0.50	0.50
MCML	0.40	0.80	0.40	0.40
Current-mode	0.80	0.70	0.80	0.35

a stronger ability of the circuit to resist interference. Table 8 lists the voltage amplitude required by the three circuits to have logic errors and η values in different processes.

Conclusions can be drawn from Table 8 as follows:

(1) In the 28 nm process, the interference voltages that cause errors in the output logic of the three types of circuits, voltage-mode CMOS, MCML, and current-mode CMOS circuits, are 0.5, 0.4, and 0.8 V, respectively. The current-mode CMOS circuit interference resistance ability is relatively stronger than that of the other two kinds of circuits. With the development of the process, the current-mode CMOS circuit with a relatively stronger immunity to interference will have a wider range of applications.

(2) The relative interference resistance ability of voltage-mode CMOS and MCML circuits in the 28 nm process is similar to that of the 65 nm process, while the relative interference resistance ability of current-mode CMOS circuits in the 28 nm process is stronger than that of the 65 nm process. According to the drain current of the MOS transistor formula, $I_D = \frac{1}{2}\mu_n C_{OX}\left(\frac{W}{L}\right)(V_{GS} - V_{TH})^2$, the larger the W/L value, the greater the impact on I_D. This results in better current robustness and stronger immunity of the current-mode CMOS

circuits to interference. In our simulations, the minimum transistor is set to $(W/L)_1$=100 nm/30 nm in the 28 nm process, and the maximum transistor is set to $(W/L)_2$=600 nm/300 nm in the 65 nm process. Obviously, $(W/L)_1>(W/L)_2$, so the relative interference resistance ability of current-mode CMOS circuits in the 28 nm process is stronger than that of the 65 nm process. Thus, the continuous progress of the process will better improve the interference resistance of current-mode CMOS circuits.

8 Effect of resistance values on current-mode CMOS circuits

Due to the existence of the intrinsic capacitance (gate and drain equivalent capacitance) of the circuit, the equivalent input impedance of the circuit is different when the circuit is fed with signals of different frequencies. In addition, parameters, such as the channel width and length of the MOS transistor in the circuit, have an effect on the input impedance; for this reason, it is necessary to study the interference effect of a cascade resistor with different values. Since only current-mode CMOS circuits have input interference source with cascade resistors, we study the effect of cascade resistance values on current-mode CMOS circuits.

To simplify the study without a loss of generality, the parameters set for the circuit simulation are the same as those in Section 4, the interference signal is a sine wave voltage source with a frequency of 100 MHz and an amplitude varying from 0.5 to 2 V, injected from the input, and the series resistor R_1 is connected with a median value of 150 kΩ and varies by 100 kΩ each at a larger and a smaller scale. The variation of λ of the current-mode CMOS circuit with the amplitude of a sine interference signal and a resistance value is shown in Table 9, and the corresponding line graph is plotted in Fig. 15.

Conclusions can be drawn as follows:

In the same interference signal amplitude, the larger the resistance value of R_1, the smaller the interference current, the smaller the degree of interference in the circuit, and the stronger the interference resistance ability of the circuit. As modern processes become more advanced, the internal capacitance of the circuit becomes smaller, the input impedance of the circuit becomes larger, and the resistance performance of the circuit will become better.

9 Conclusions

In this paper, the effect of EMI on three kinds of gates is investigated, and the three kinds of NOT gates are simulated and compared with respect to the three aspects of the injection terminal of the interference source, the interference waveform, and the interference frequency. It is found that the EMI has a greater effect on the circuits if it is injected from the input of the signals from the simulation results. For high-frequency EMI, the current-mode CMOS circuits have a better resistance performance than the other two kinds of circuits due to the presence of more intrinsic capacitance inside, which suppresses the high-frequency EMI. Additionally, the same amplitude square wave has more high-frequency components than a sine wave, and the current-mode CMOS circuits can better filter high-frequency EMI, so it is less sensitive to square wave EMI than the other two kinds of circuits, and the ability to resist square wave EMI is stronger. There are some variations regarding the resistance of the circuits to interference at different temperatures and in different processes. In the temperature range of

Table 9 Variation of λ of current-mode CMOS circuit with amplitude of sine interference signal and resistance value

Interference amplitude (V)	λ				
	Resistance=50 kΩ	100 kΩ	150 kΩ	200 kΩ	250 kΩ
0.5	1.540	1.455	0.000	0.000	0.000
1.0	1.859	1.659	1.474	0.059	0.000
1.5	2.044	1.791	1.631	1.440	0.081
2.0	2.135	1.921	1.745	1.619	1.411

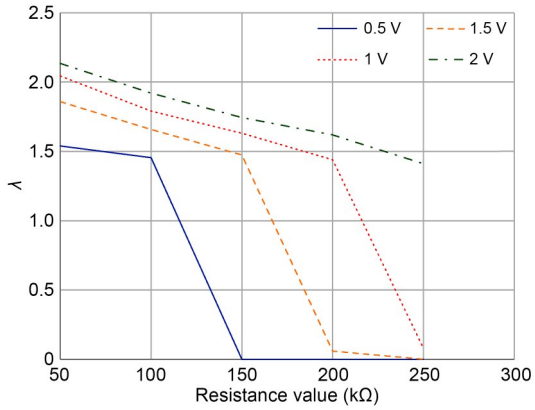

Fig. 15 Variation of λ of current-mode CMOS circuit with amplitude of sine interference signal and resistance value

−40 to 125 ℃, the higher the temperature, the weaker the immunity of voltage-mode CMOS and MCML circuits, and the stronger the immunity of current-mode CMOS circuits. In the 28 nm process, the immunity of the current-mode CMOS circuit is relatively stronger than that of the other two kinds of circuits. The relative immunity of voltage-mode CMOS and MCML circuits in the 28 nm process is similar to that of the 65 nm process, while the relative immunity of current-mode CMOS circuits in the 28 nm process is stronger than that in the 65 nm process.

Based on the aforementioned conclusions, we would like to point out that, with technology scaling, the internal capacitance of the circuits becomes smaller and smaller, the equivalent input impedance of the circuits is large in the high-frequency state, and the interference immunity of the current-mode CMOS circuits will be further enhanced. Therefore, the current-mode CMOS circuits have the advantages of high speed and low power consumption in the deep submicron process, as well as strong EMI resistance ability. With the development of ICs, the need for high-speed and EMI resistance performance becomes more urgent, and the current-mode CMOS circuits will have better application prospects.

Contributors

Fangjun LIU conducted the investigation, experimental validation, data organization, and drafted the original manuscript. Jiaming SHEN assisted with investigation and validation. Jizhong SHEN provided experimental guidance, supervision, paper review, and editing.

Conflict of interest

All the authors declare that they have no conflict of interest.

Data availability

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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